PRODUCT SUMMARY

Si82900/10/11/13 Isolated Safety Gate Drivers Product Summary

Applications

- Electric vehicle traction inverters
- Full hybrid vehicle traction inverters
- Plug-in hybrid traction inverters

Features

- Programmable variable current drive (ProVCD™)
  - Current-mode controlled output
  - Three phases of turn-on and turn-off waveform control
  - 15 A sink/source continuous output
  - 15 A integrated Miller clamp
  - Current settings adjustable from 0 to 15 A
- Suitable for high-side or low-side use
- Functional safety support
  - Developed according to ISO 26262
  - Extensive diagnostics with latent fault detection
  - Power-on and on-demand built-in self tests
  - Configurable fault pins
  - Fault-triggered soft shutdown
  - Forced safe states for outputs
  - Suitable for use in systems up to ASIL D
- SPI interface
  - Programmable configuration
  - CS, ENUM, and daisy-chain addressing modes
  - SPI communication integrity checks
- Complementary switching control inputs
  - Overlap protection
  - Programmable dead-time
  - Deglitch options for noise filtering
  - Control input to gate signal integrity check
- Fast overcurrent protection
  - DESAT detection
  - Current mirror short-circuit protection
- ADC-based measurement system
  - Four channels for temperature, voltage, or current
  - PTC, NTC, or diode temperature sensor support
  - Gate voltage monitoring pin
  - Two back-channels to PWM data to host MCU
  - V_{th} measurement for FET health monitoring
- On-chip and external Miller clamp capability
- VDDO 18 V to 30 V
  - On-chip regulated positive gate voltage
  - On-chip generated negative gate voltage
  - Output shutdown clamp for unpowered condition
- VDDI 3.3 V or 5 V
  - CMOS inputs for noise immunity
- Transient immunity (CMTI): 125 kV/µs
- Reliable isolation technology
  - Up to 6 kV_{RMS} isolation for one minute
  - Up to 1500 V_{RMS} working voltage
  - Up to 10 kV peak bipolar surge
  - Barrier lifetime > 20 years per IEC 60747-17
- Wide operating range
  - –40 to +125 °C
- RoHS-compliant package
- Multiple package options
- AEC-Q100 qualified
- Automotive-grade manufacturing

Safety and Regulatory Approvals (Pending)

- UL recognized
  - 1577 (6000 V_{RMS} for one minute)
- CSA certification conformity
  - 62368-1 (reinforced insulation)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

1. Description

The Si829x isolated safety gate driver with extensive configuration, feedback, and diagnostics is ideal for traction inverter applications. Featuring complementary input controls, this single-driver device can be placed in high-side or low-side locations to form half- or full-bridge switching power supplies. Programmable variable current drive (ProVCD™) coupled with on-the-fly, cycle-by-cycle parametric update capability and high constant gate current assures minimum switching losses when driving discrete or modular FET gate loads. The chip operates with a flexible input voltage (VDDI) and a maximum output-side supply voltage (VDDO_PWR) of 30 V. It includes a programmable on-chip regulator for the positive gate voltage, and the negative gate voltage is generated as a function of the output supply voltage and the programmed positive gate voltage.

The Si829x is well-suited for driving IGBTs and silicon carbide FETs in traction inverter applications. These drivers utilize Skyworks proprietary silicon isolation technology, supporting up to 6 kV_{RMS} for one-minute isolation rating and 10 kV peak bipolar surge voltage tolerance. This technology enables high common-mode transient immunity (125 kV/µs), low propagation delays, minimal variation with temperature and age, and tight part-to-part skew matching.

The Si829x also offers over-current and over-temperature protection, under-voltage and over-voltage fault detection, dead-time programmability, overlap protection, and fail-safe operation with the gate drive output default low in case of power loss. In addition, the SPI interface facilitates rich programmability of configurations, fault and error handling, autonomous or report-to-host fault reactions, and diagnostic feedback to the power supply control ASIC or MCU.

The Si829x was designed in full compliance with ISO 26262 and is suitable for ASIL D-rated applications.

2. Device Pinouts

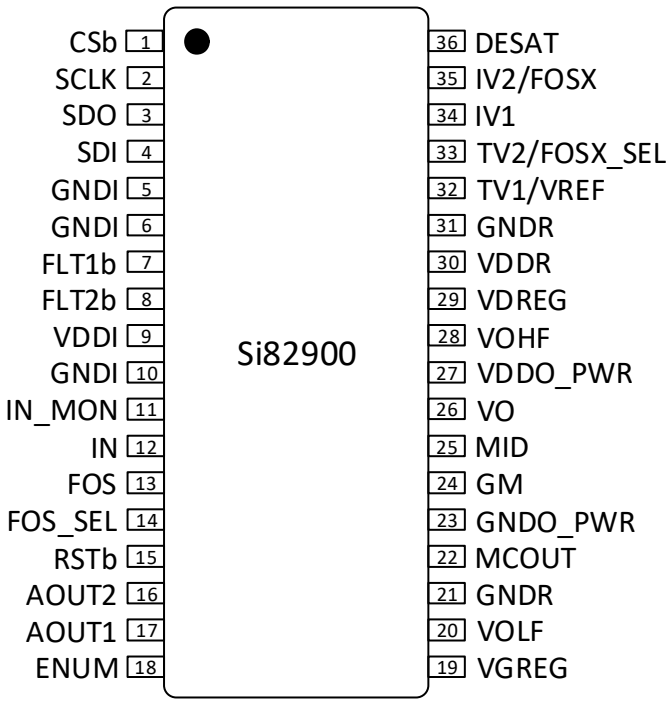

Figure 1. Si82900 36-Pin WB SSOP

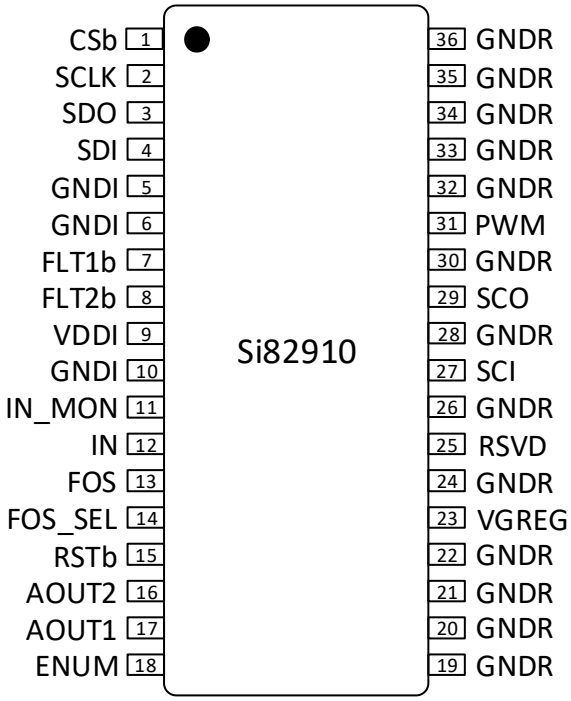

Figure 2. Si82910 36-Pin WB SSOP

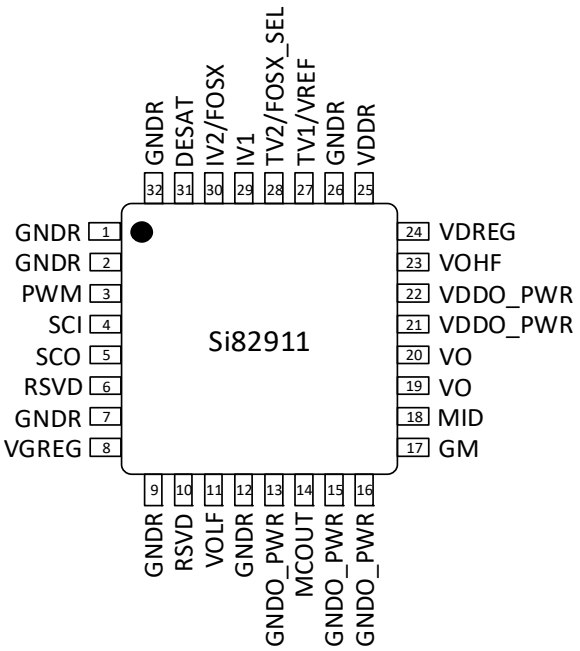

Figure 3. Si82911 5x5 32-Pin QFN

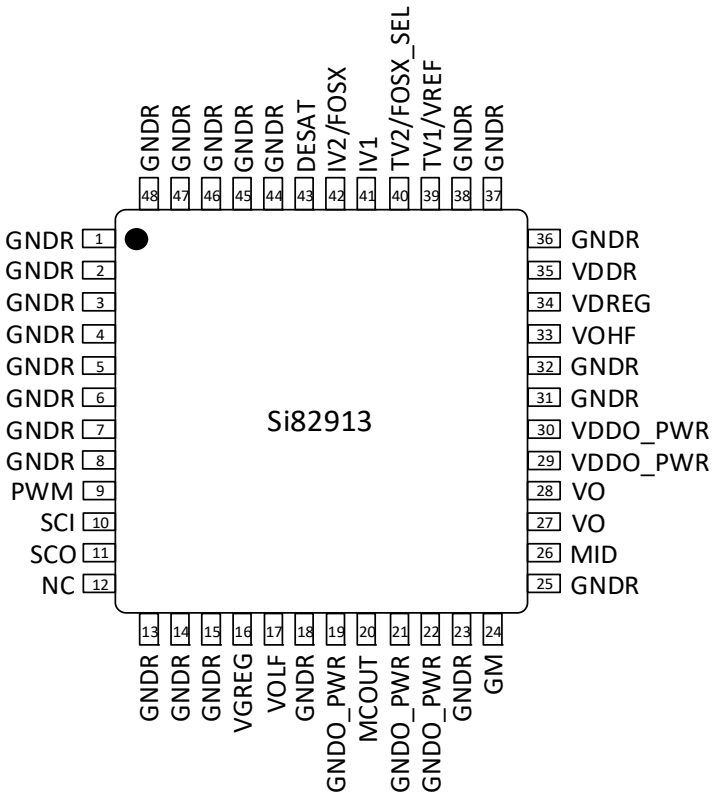

Figure 4. Si82913 7x7 48-Pin QFN

2.1. Pin Details

Table 1. Input Side (Si89200 or Si89210)

Pin	I/O	PU/PD[1]	Description
VDDI	Supply	—	Supply input side.
IN	In	PD	Gate driver control.
IN_MON	In	PD	Gate driver monitoring input (connect to complementary driver control input).
RSTb	In	PD	Reset (active low). This pin has a weak pull-down to assure the part is held in reset if not purposefully driven high. To disable the hardware-based reset capability, tie this pin to VDDI.
FOS	In	PD	Force output state (active high).
FOS_SEL	In	PD	Forced output state polarity selection pin (0: output low; 1: output high).
FLT1b	Out	PD	Fault alert pin 1 (active low). Open drain output pin requires external 10 kΩ pull-up resistor.
FLT2b	Out	PD	Fault alert pin 2 (active low). Open drain output pin requires external 10 kΩ pull-up resistor.
AOUT1	Out	PD	Analog measurement channel 1.
AOUT2	Out	PD	Analog measurement channel 2.
ENUM	In	PD	Resistor pin for part identification in enumeration mode.
SDI	In	PD	SPI bus data from host.
SDO	Out	PD	SPI bus data to host.
SCLK	In	PD	SPI bus clock from host.
CSb	In	PU	SPI bus chip selection (active low).
GNDI	Supply	—	Ground input side.

1. PU/PD indicates whether the pin has a weak pull-up or pull-down included.

Table 2. Package-to-Package Interface Pins (Si82910 to Si82911 or Si82913)

Pin	I/O	PU/PD[1]	Description (with Respect to Si82910)
VGREG	In analog	—	5 V regulator input referenced to GNDR. Connect VGREG pin between Si82910 and Si82911 (Option 2) or Si82913 (Option 3).
PWM	Out	—	Gate driver control signal.
SCO	Out	—	Data out, chip-to-chip communication channel.
SCI	In	—	Data in, chip-to-chip communication channel.
GNDR	Supply	—	Ground path connection.
RSVD	RSVD	—	Reserved pin; tie to GNDR net.

1. PU/PD indicates whether the pin has a weak pull-up or pull-down included.

Table 3. Output Side (Si82900, Si82911, or Si82913)

Pin	I/O	PU/PD[1]	Description
VDDO_PWR	Supply	—	Supply output side.
VDDR	Out analog	—	Decoupling capacitor return pin (pairs with VDREG and VOHF). Do not short VDDR to VDDO_PWR on the PCB.
VDREG	Out analog	—	Connection for decoupling capacitor for 5 V regulator referenced to VDDR.
DESAT	In analog	—	Desaturation detection connection referenced to MID.
VOHF	Out analog	—	Connection for reservoir capacitor for the pull-up current referenced to VDDR.
VO	Out analog	PD	Gate drive output. Note: The Si82911 and Si82913 QFN packages have two adjacent VO pins with identical functionality. The two VO pins must be shorted together on the customer PCB design. A single trace can be run from this shorted node to the gate of the switch.
VOLF	Out analog	—	Connection for reservoir capacitor for the pull-down current referenced to GNDR.
GM	In analog	PD	Gate voltage waveform monitoring pin.
MCOUT	Out analog	PD	Control gate voltage for optional external Miller Clamp. Drives voltage high to turn on external clamping FET; supports use of either NPN bipolar or NMOS FET external clamp devices.
MID	Out analog/supply	—	Midpoint reference between high-side and low-side FETs in half-bridge when using on-chip VPOS regulator or supply pin when using external voltage supplies.
IV1	In analog	—	Voltage measurement path that monitors current levels via resistor to MID for current output mirror switches, overcurrent protection, and short-circuit protection.
TV1/VREF	In analog	—	Voltage measurement path for external temperature sensor; includes on-chip programmable current source to bias temperature sensor. Can alternatively be configured as an input to receive an external voltage reference for the on-chip measurement ADC.
IV2/FOSX	In analog or in digital	PD (FOSX only)	Voltage measurement path that monitors current levels via resistor to MID for current output mirror switches, providing over-current protection and short-circuit protection. Can alternatively be configured for output-side force output state control.
TV2/FOSX_SEL	In analog or in digital	PD (FOSX_SEL only)	Voltage measurement path for external temperature sensor; includes on-chip programmable current source to bias temperature sensor. Can, alternatively, be configured for output-side force output state polarity selection.
VGREG	Out analog	—	Connection for decoupling capacitor for 5 V regulator referenced to GNDR.
GNDR	Out analog	—	Decoupling capacitor return pin (pairs with VGREG and VOLF) for internal analog ground return. Do not short GNDR to GNDO_PWR on the PCB.
GNDO_PWR	Supply	—	Ground output side.
RSVD	RSVD	—	Reserved pin; tie to GNDR net.

1. PU/PD indicates whether the pin has a weak pull-up or pull-down included.

Table 4. Si82911 or Si82913 Only

Pin	I/O	PU/PD[1]	Description
ePad	Supply	—	Thermal relief pad located on bottom side of device; tie to GNDR net.

1. PU/PD indicates whether the pin has a weak pull-up or pull-down included.

3. Functional Block Diagrams

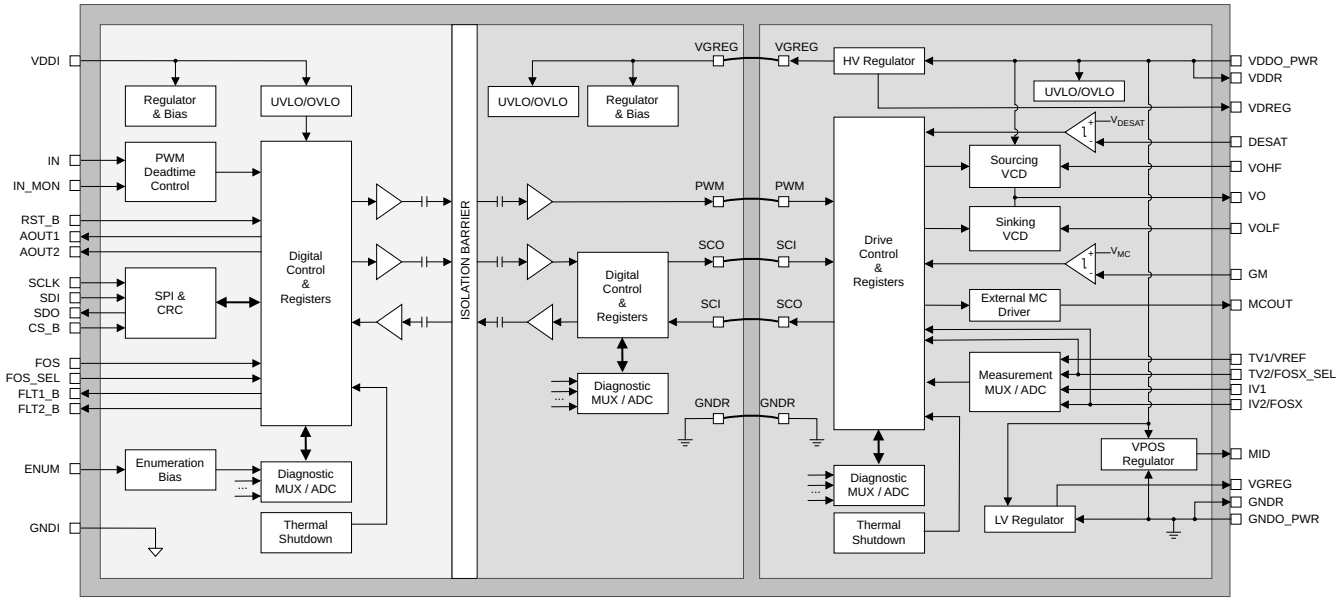

Figure 5. Si82900 Functional Block Diagram

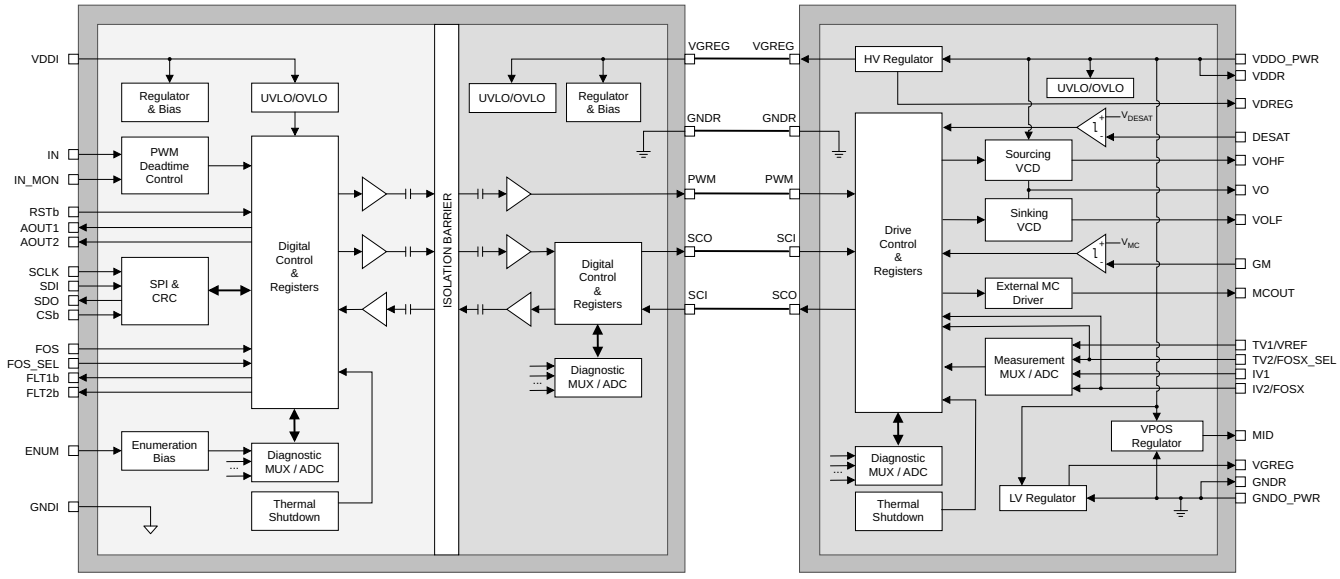

Figure 6. Si82910 with Si82911 or Si82913 Functional Block Diagram

4. Functional Safety

Functional safety considerations are a key aspect of the development of the Si829x Isolated Safety Gate Driver. The Si829x is developed according to ISO 26262.

Extensive safety analysis of Si829x results in a robust product suitable for ASIL D applications. ASIL management removes the necessity for redundant safety components, ensuring predictable fault reactions for deterministic safe states. Si829x offers complete diagnostic coverage of the power switch gate drive. Additionally, automated latent fault checks minimize processor overhead during boot-up.

Figure 7 illustrates key safety features of the Si829x.

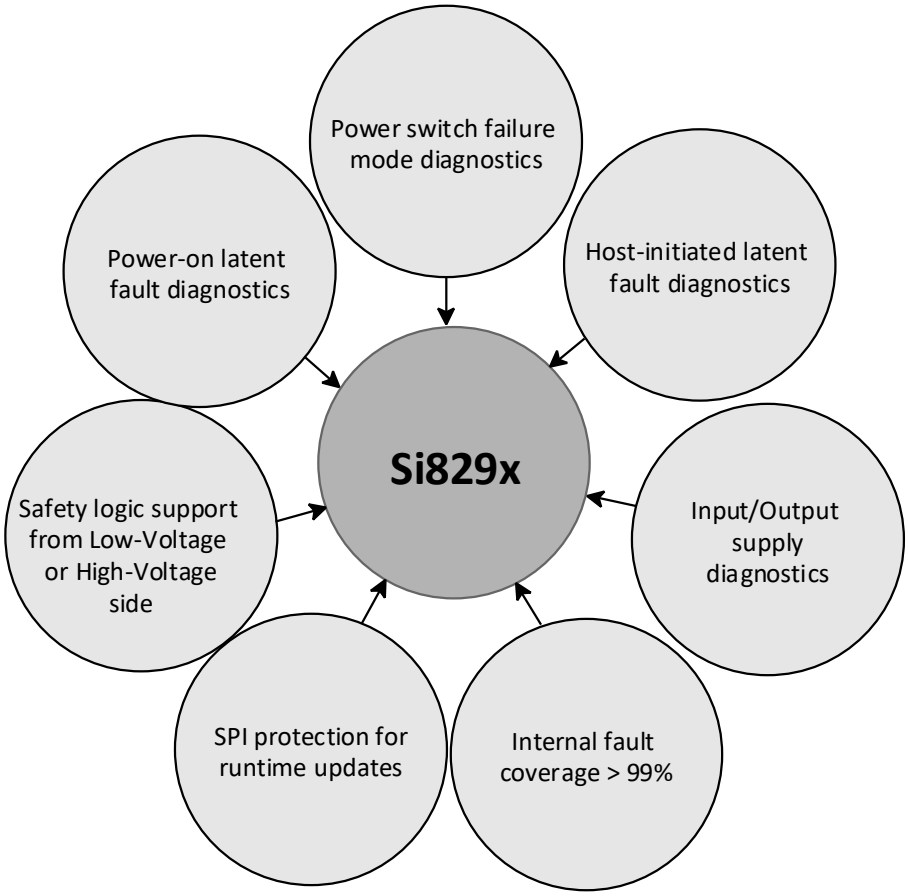

Figure 7. Si829x Functional Safety Highlights

5. Programmable Variable Current Drive (ProVCD™)

ProVCD™ is a new approach to power switch gate drives that utilizes dynamically programmable current sources to precisely control charge delivery to the gate. This current-mode architecture provides on-the-fly control, allowing for flexible drive strength at different stages of turn-on and turn-off in place of current-limiting external gate resistors. It precisely controls the current source waveform, enhancing efficiency by enabling adjustments to drive strength based on system conditions, such as temperature, RPM, and battery voltage fluctuations during discharge or regenerative braking. This approach also minimizes switching losses and delivers notable system advantages by helping to mitigate emissions and overshoot, as well as addressing unsafe shoot-through scenarios. Additionally, it includes soft shutdown alternatives following high-current faults.

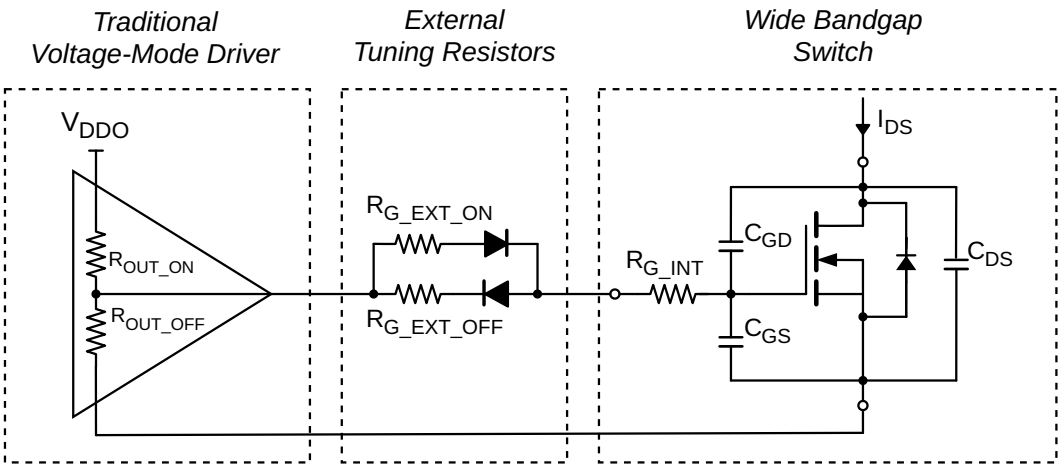

Figure 8. Traditional Voltage-Mode Driver (TVMD)

Traditional voltage-mode driver (TVMD) products rely on well-characterized, fixed-value gate resistors to limit current and control dV/dt in worst-case operating conditions and steering diodes to control the rate of turn-on and turn-off. This approach (with external tuning resistors) reduces overall system efficiency as the design performs sub-optimally in typical operating conditions. Some TVMD architectures include multiple turn-on and turn-off gate resistors (sometimes called “strength control”), but these architectures also operate by voltage-mode control and suffer similar limitations.

Additionally, internal Miller clamps must be implemented as separate circuits that utilize a separate pin to connect downstream of the gate resistors, adding die area and additional layout complexity.

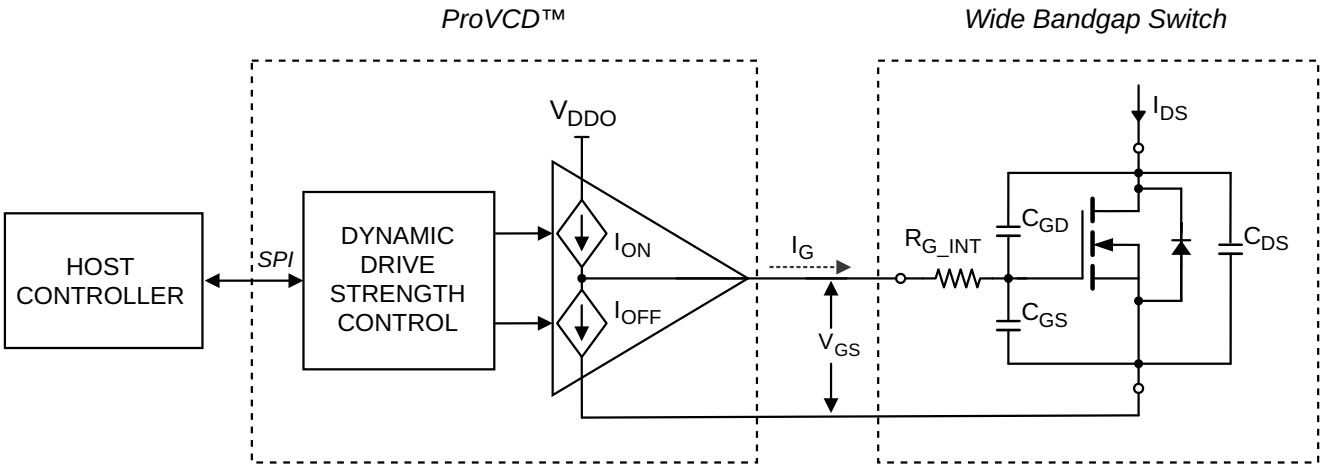

Figure 9. Programmable Variable Current Drive (ProVCD™)

ProVCD™ eliminates fixed gate resistors, replacing them with a carefully controlled current-mode gate drive that includes a fully integrated Miller clamp. The current mode output also drastically reduces gate current variation across temperature and voltage when compared with voltage-mode drivers, ensuring consistent and reliable operation across the spectrum of environmental conditions. The configurable current settings enable generation of unique drive strength settings with small time steps for the duration of the turn-on and turn-off stages. Additionally, the Si829x can be programmed to respond autonomously to fault conditions using alternate soft-shutdown profiles to protect the power switch from damage.

6. Typical Application Circuit

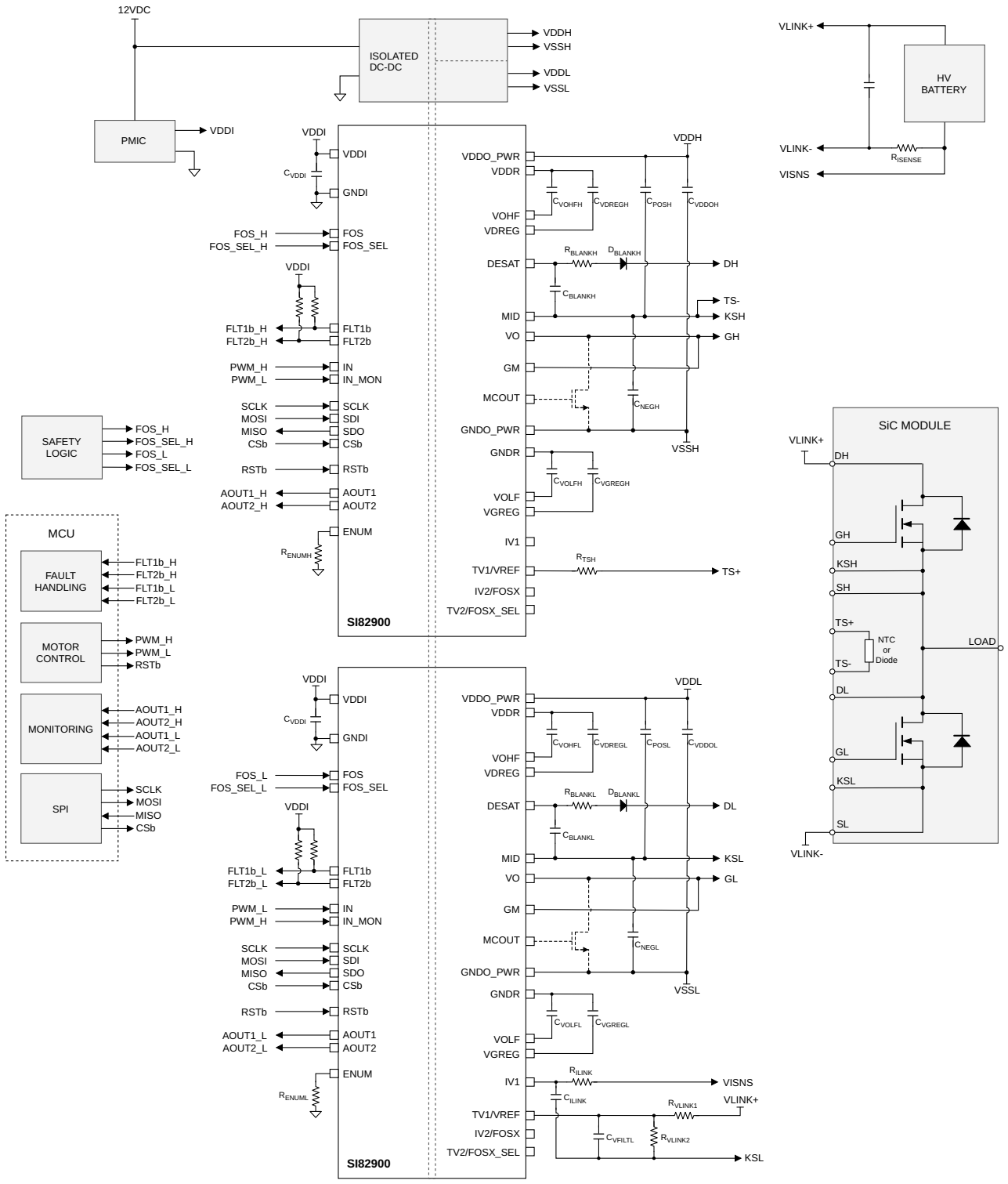

Figure 10. Half-Bridge Gate Drive Circuit Using Two Si82900s

7. Package and Handling Information

7.1. 36-Lead WB SSOP Top Marking

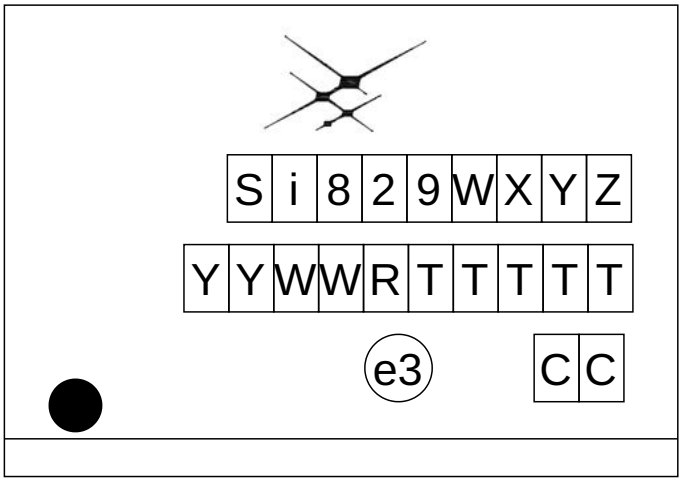

Figure 11. 36-Lead WB SSOP Top Marking

Table 5: 36-Lead WB SSOP Top Marking Explanation

Line 0 Marking:	Centered	Skyworks logo
Line 1 Marking:	Base part number ordering options (see 8. "Ordering Guide" for more information)	Si829 = Isolated safety gate driver WX = Die and package configuration 00 = 3-die, Option 1 single-package solution 10 = 2-die, multi-package option (pairs with Si82911 for Option 2 or Si82913 for Option 3) YZ = VPOS and SPI addressing mode (for Si82900) AA = VPOS enabled; chip select or enumeration AB = VPOS enabled; daisy chain BA = VPOS disabled; chip select or enumeration BB = VPOS disabled; daisy chain Y = SPI addressing mode (for Si82910) A = Chip select or enumeration B = Daisy chain Z = (Unused for Si82910)
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg. Trace Code	Manufacturing traceability code The manufacturing traceability code represented by “RTTTTT” contains, as its first character, a letter in the range N through Z to indicate revision level and automotive grade.
Line 3 Marking:	1.00 mm diameter circle, bottom-left-justified	Pin 1 Indicator
	e3 circle is 1.10 mm diameter	The “e3” symbol indicates Pb-free lead finish.
	CC = Country of origin ISO code abbreviation	TW = Taiwan

7.2. 32-Lead 5x5 mm QFN Top Marking

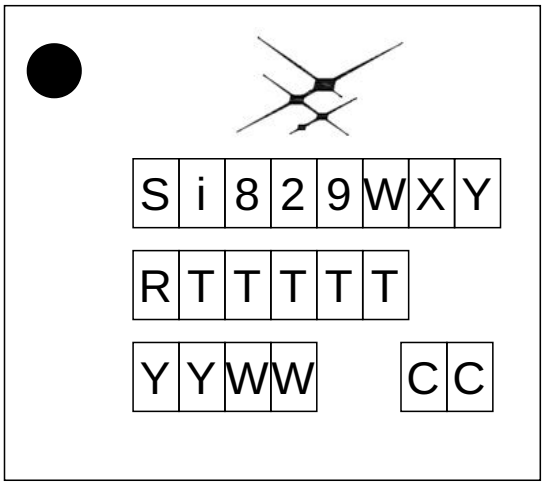

Figure 12. 32-Lead 5x5 mm QFN Top Marking

Table 6. 32-Lead 5x5 mm QFN Top Marking Explanation

Line 0 Marking:	0.40 mm diameter circle, top-left-justified	Pin 1 indicator
	Right-justified with Line 1 text	Skyworks logo
Line 1 Marking:	Base part number ordering options (see 8. "Ordering Guide" for more information)	Si829 = Isolated safety gate driver WX = Die and package configuration 11 = 1-die, multi-package option 2 (pairs with Si82910) Y = VPOS configuration A = VPOS enabled B = VPOS disabled
Line 2 Marking:	RTTTTT = Mfg. trace code	Manufacturing traceability code The manufacturing traceability code represented by “RTTTTT” contains, as its first character, a letter in the range N through Z to indicate revision level and automotive grade.
Line 3 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	CC = Country of origin ISO code abbreviation	TW = Taiwan

7.3. 48-Lead 7x7 mm QFN Top Marking

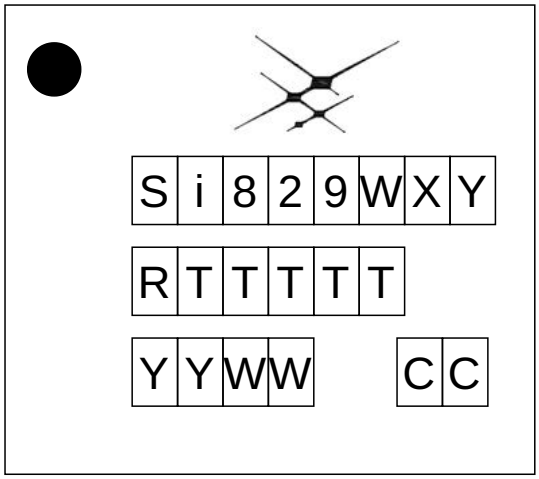

Figure 13. 48-Lead 7x7 mm QFN Top Marking

Table 7. 48-Lead 7x7 mm QFN Top Marking Explanation

Line 0 Marking:	0.50 mm diameter circle, top-left-justified	Pin 1 indicator
	Right-justified with Line 1 text	Skyworks logo
Line 1 Marking:	Base part number ordering options (see 8. "Ordering Guide" for more information)	Si829 = isolated safety gate driver WX = die and package configuration 13 = 1-die, multi-package Option 3 (pairs with Si82910) Y = VPOS Configuration A = VPOS Enabled B = VPOS Disabled
Line 2 Marking:	RTTTTT = Mfg. trace code	Manufacturing Traceability Code The manufacturing traceability code represented by “RTTTTT” contains, as its first character, a letter in the range N through Z to indicate revision level and automotive grade.
Line 3 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	CC = Country of origin ISO code abbreviation	TW = Taiwan

7.4. 36-Lead WB SSOP Package

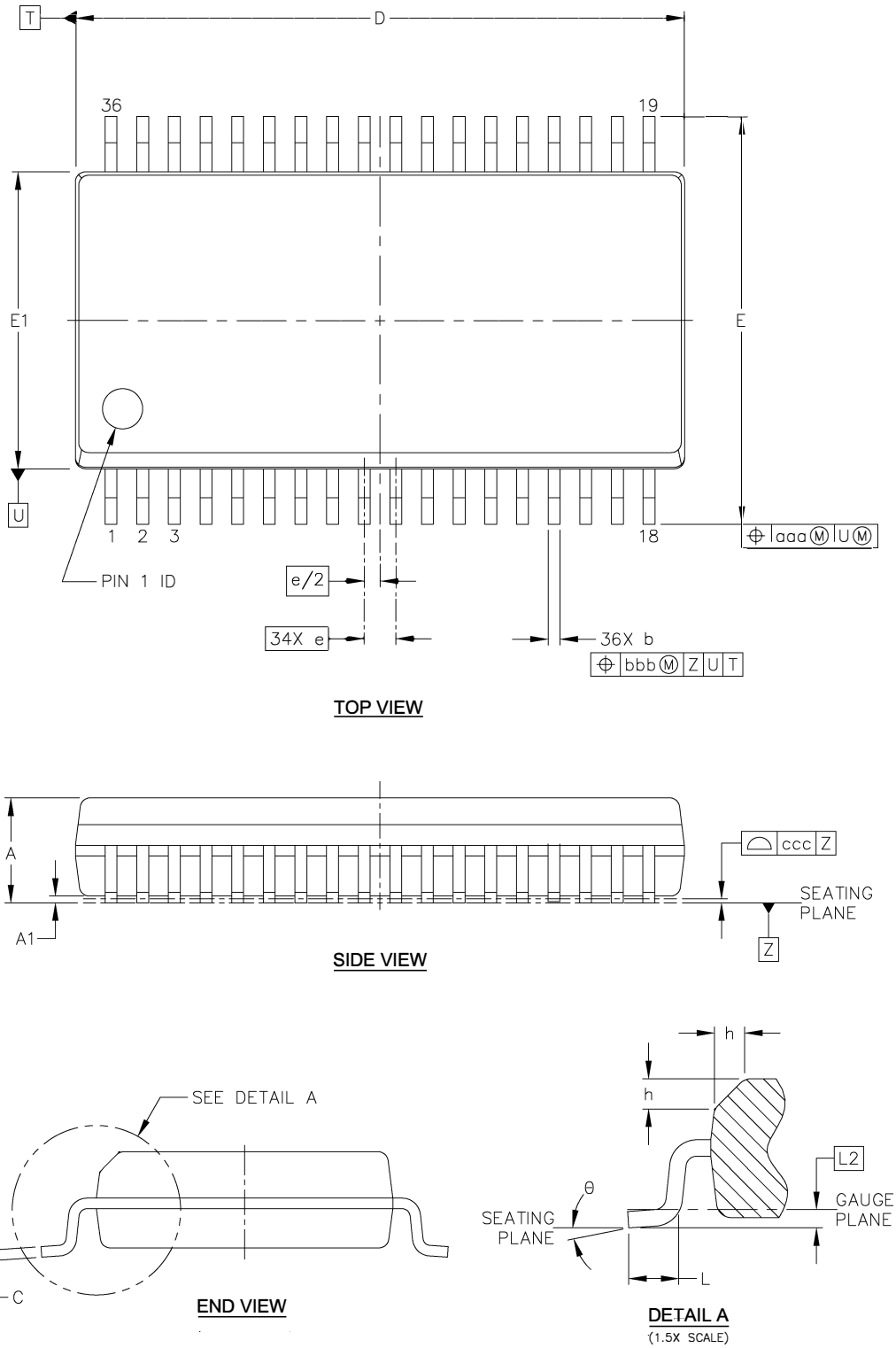

Figure 14. 36-Lead SSOP Package Outline Drawing

Table 8. 36-Lead SSOP Package Dimensions[1,2,3,4]

Dimension	Symbol	Min	Max
Overall height	A	—	2.65
Stand off	A1	0.10	0.30
Lead width	b	0.25	0.35
L/F thickness	c	0.20	0.33
Body size	D	15.20	15.60
	E	10.05	10.55
	E1	7.40	7.60
Lead pitch	e	0.80 BSC	
Lead lengh	L	0.40	1.27
Gauge plane	L2	0.25 BSC	
Corner chamfer	h	0.25	0.75
Foot angle	θ	0°	8°
Lead edge tolerance	aaa	0.25	
Lead offset	bbb	0.25	
Coplanarity	ccc	0.10	

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ANSI Y14.5M.
   BSC: Basic dimension. Theoretically exact shown without tolerance.
   REF: Reference dimension. Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25mm per side.
4. Recommended reflow profile per JEDEC J_STD_020 specification for small-body, lead-free components.

7.5. 32-Lead 5x5 mm QFN Package

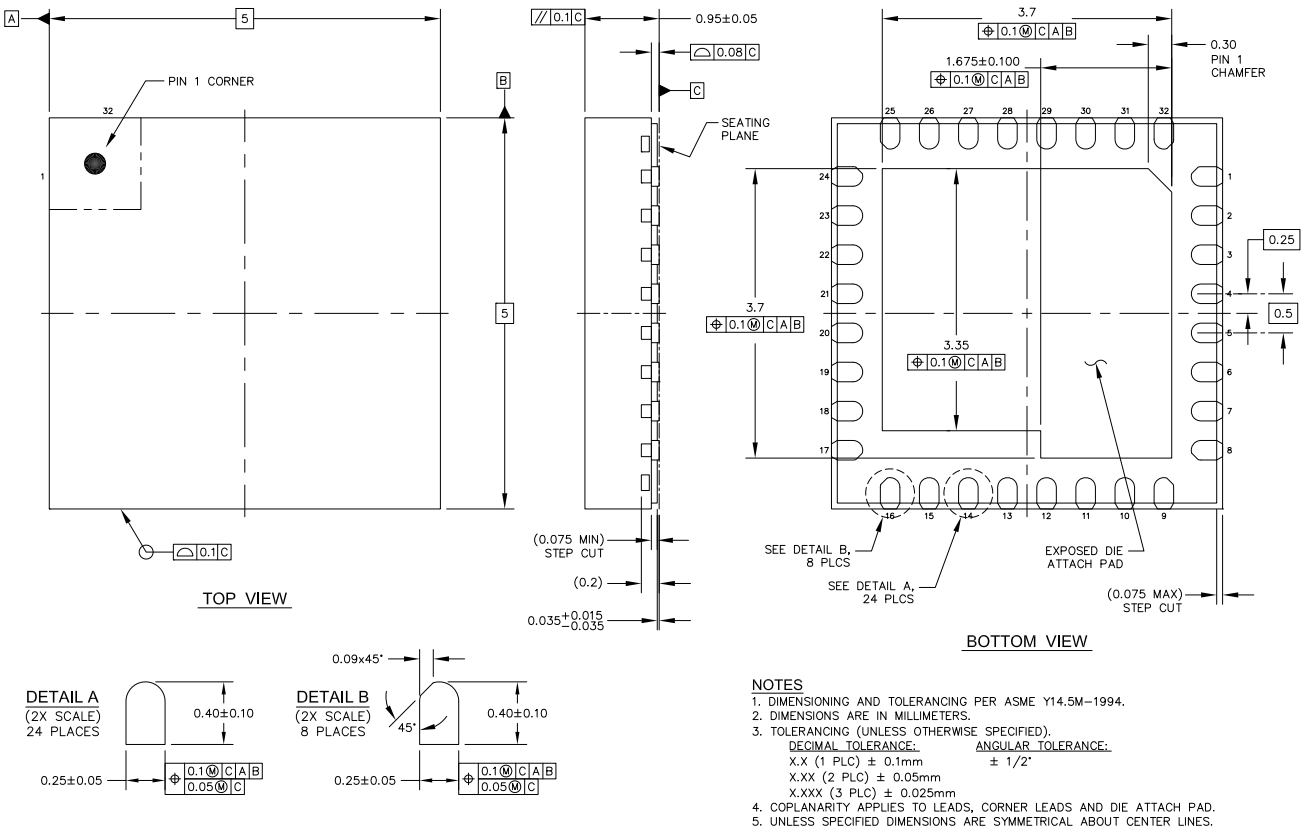

Figure 15. 32-Lead 5x5mm QFN with Wettable Flanks Package Outline Drawing

7.6. 48-Lead 7x7 mm QFN Package

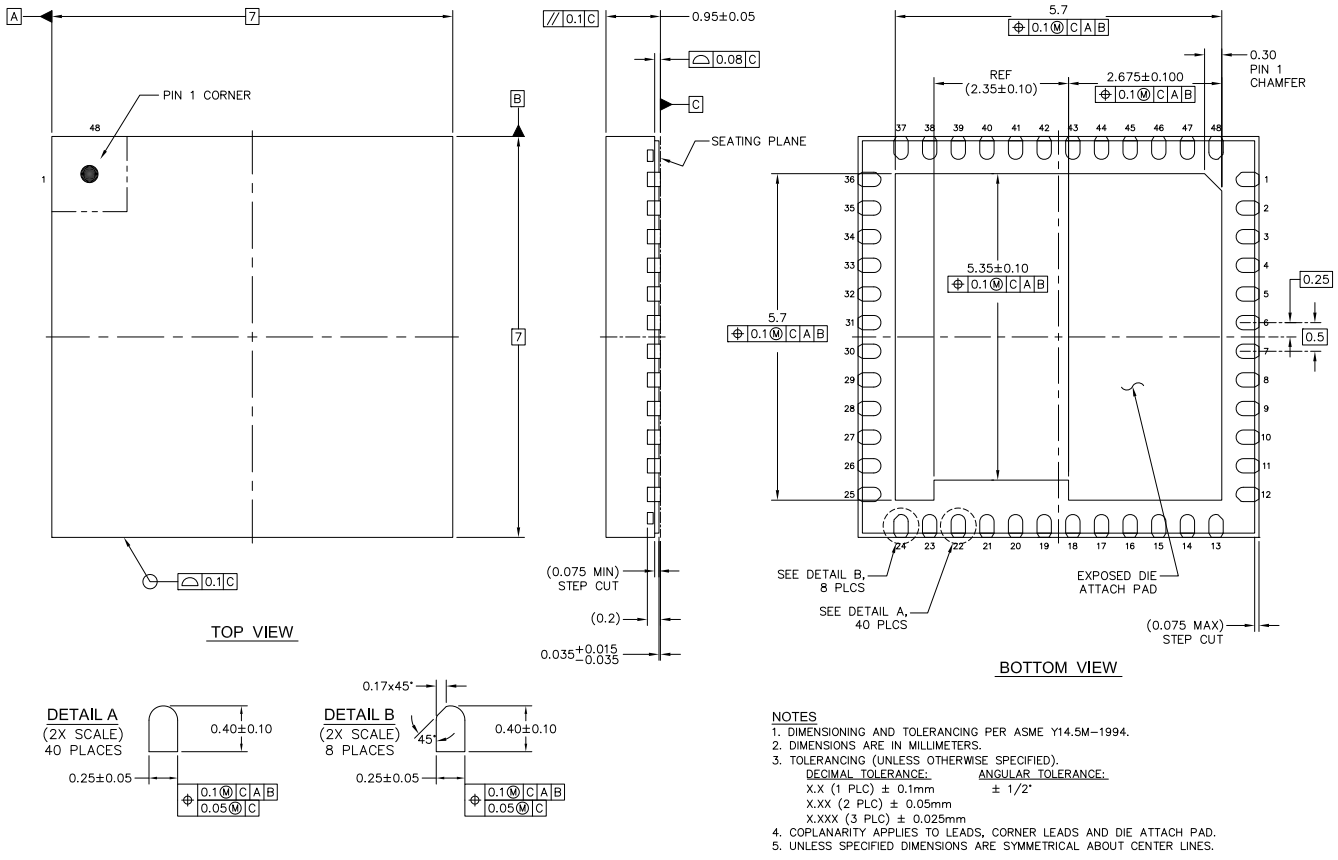

Figure 16. 48-Lead 7x7mm QFN with Wettable Flanks Package Outline Drawing

8. Ordering Guide

Table 9. Si829x Ordering Guide

Ordering Part Number (OPN)[1,2]	Package Option[3,4]	Maximum Constant Current	VPOS Regulator Enabled	SPI Addressing Mode	Isolation Rating	Package Type
Si82900AA-AU	1	15 A	Yes	Chip select or enumeration	6.0 kV_{RMS}	SSOP-36
Si82900AB-AU	1	15 A	Yes	Daisy chain	6.0 kV_{RMS}	SSOP-36
Si82900BA-AU	1	15 A	No	Chip select or enumeration	6.0 kV_{RMS}	SSOP-36
Si82900BB-AU	1	15 A	No	Daisy chain	6.0 kV_{RMS}	SSOP-36
Si82910A-AU	2, 3	N/A	N/A	Chip select or enumeration	6.0 kV_{RMS}	SSOP-36
Si82910B-AU	2, 3	N/A	N/A	Daisy chain	6.0 kV_{RMS}	SSOP-36
Si82911A-AF	2	15 A	Yes	N/A	N/A	32-pin QFN (5 mm x 5 mm) with wettable flanks and ePad
Si82911B-AF	2	15 A	No	N/A	N/A	32-pin QFN (5 mm x 5 mm) with wettable flanks and ePad
Si82913A-AF	3	15 A	Yes	N/A	N/A	48-pin QFN (7 mm x 7 mm) with wettable flanks and ePad
Si82913B-AF	3	15 A	No	N/A	N/A	48-pin QFN (7 mm x 7 mm) with wettable flanks and ePad

1. “Si” and “SI” are used interchangeably.
2. An “R” at the end of the ordering part number indicates tape-and-reel package option.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. Option 2 is implemented with one Si82910 variant plus one Si82911 variant paired together. Option 3 is implemented with one Si82910 variant plus one Si82913 variant paired together. Customers must necessarily order one of each for a gate driver instance on their designs. They only work when paired (there is no use case for the customer using only a stand-alone Si82910, Si82911, or Si82913).

9. Revision History

Revision	Date	Description
A	September, 2026	Initial release