

### Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory- customizable to any frequency, with samples available in one to two weeks.



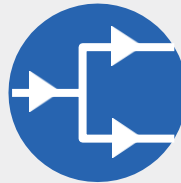
#### Oscillators

- Any frequency up to 3 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)



#### Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs



#### Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant



#### Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs





# Intel FPGA Phase Noise Mask Requirements



Stratix 10 GX/SX Arria 10 GX/SX/GT Stratix V GX/GS/GT Arria V GX/SX		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset	Phase Noise (156.25 MHz)	Si545	Si540	Si570/Si53x	Si56x	Si55x	Si5330x	Si5391	Si5341 Si5340	Si5332	Si539x	Si534x	Si5383/48
10 kHz	-112 dBc/Hz	-140 dBc/Hz	-132 dBc/Hz	-128 dBc/Hz	-136 dBc/Hz	-128 dBc/Hz	-140 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-126 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-137 dBc/Hz
100 kHz	-122 dBc/Hz	-145 dBc/Hz	-139 dBc/Hz	-135 dBc/Hz	-142 dBc/Hz	-133 dBc/Hz	-150 dBc/Hz	-146 dBc/Hz	-141 dBc/Hz	-132 dBc/Hz	-145 dBc/Hz	-141 dBc/Hz	-145 dBc/Hz
1 MHz	-132 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz	-144 dBc/Hz	-150 dBc/Hz	-144 dBc/Hz	-154 dBc/Hz	-149 dBc/Hz	-150 dBc/Hz	-154 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz

Arria V GT/ST		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset	Phase Noise (156.25 MHz)	Si545	Si540	Si570/Si53x	Si56x	Si55x	Si5330x	Si5391	Si5341 Si5340	Si5332	Si539x	Si534x	Si5383/48
10 kHz	-120 dBc/Hz	-140 dBc/Hz	-132 dBc/Hz	-128 dBc/Hz	-136 dBc/Hz	-128 dBc/Hz	-140 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-126 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-137 dBc/Hz
100 kHz	-120 dBc/Hz	-145 dBc/Hz	-139 dBc/Hz	-135 dBc/Hz	-142 dBc/Hz	-133 dBc/Hz	-150 dBc/Hz	-146 dBc/Hz	-141 dBc/Hz	-132 dBc/Hz	-145 dBc/Hz	-141 dBc/Hz	-145 dBc/Hz
1 MHz	-130 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz	-144 dBc/Hz	-150 dBc/Hz	-144 dBc/Hz	-154 dBc/Hz	-149 dBc/Hz	-150 dBc/Hz	-154 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz

# Intel FPGA Phase Noise Mask Requirements



Agilex E-Tile		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset	Phase Noise (156.25 MHz)	Si545	Si540	Si570/Si53x	Si56x	Si55x	Si5330x	Si5391	Si5341 Si5340	Si5332	Si539x	Si534x	Si5383/48
10 kHz	-130 dBc/Hz	-140 dBc/Hz	-132 dBc/Hz	-128 dBc/Hz	-136 dBc/Hz	-128 dBc/Hz	-140 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-126 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-137 dBc/Hz
100 kHz	-138 dBc/Hz	-145 dBc/Hz	-139 dBc/Hz	-135 dBc/Hz	-141 dBc/Hz	-133 dBc/Hz	-150 dBc/Hz	-146 dBc/Hz	-141 dBc/Hz	-132 dBc/Hz	-141 dBc/Hz	-141 dBc/Hz	-145 dBc/Hz
1 MHz	-140 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz	-144 dBc/Hz	-150 dBc/Hz	-144 dBc/Hz	-154 dBc/Hz	-149 dBc/Hz	-160 dBc/Hz	-154 dBc/Hz	-160 dBc/Hz	-160 dBc/Hz	-160 dBc/Hz

For more information, visit [silabs.com/timing](https://www.silabs.com/timing)