# Silicon Labs

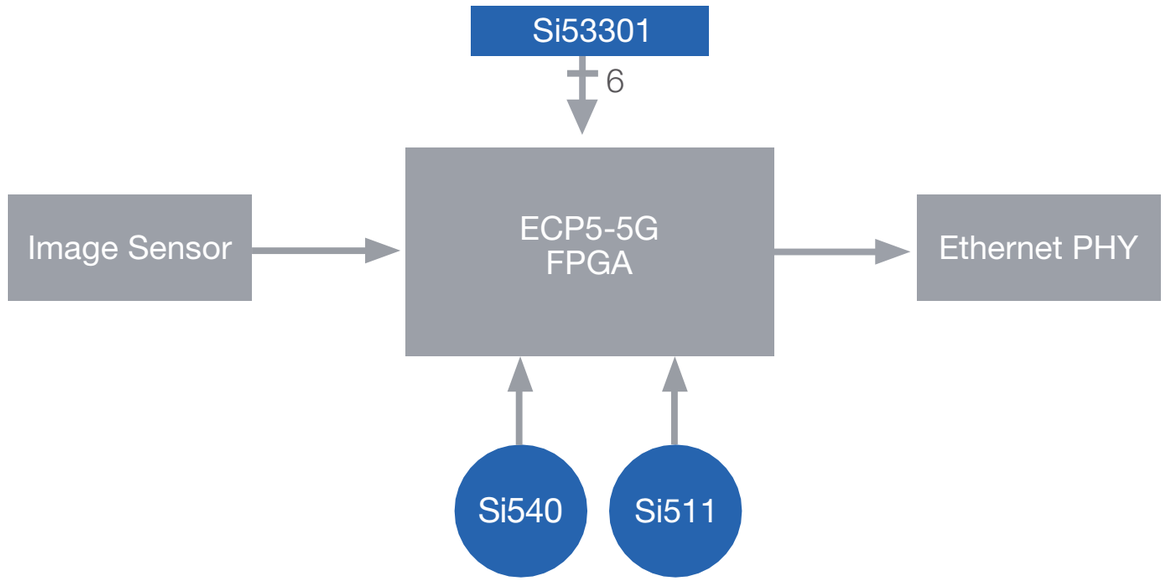
## Timing Solutions for Lattice Semiconductor

## Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.




For more information related to reference designs or partner pricing, please contact your local Silicon Labs sales representative.

### Oscillators

- Any frequency up to 3 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

### Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs
- PCI Express Gen 1/2/3/4/5 compliant

### Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

### Jitter Attenuating Clocks/Network Synchronizers

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs