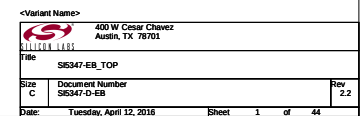
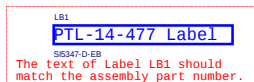


To ascend from a block schematic, right click and select "Previous View".



REVISION CONTROL

Rev 2.1 - Jan 12, 2014, Initial Board Release
Includes PCB and label on BOM.

Rev 2.2 - April 13, 2016, changed U6 to custom
part number CF380P0997AGQ

<Core Design>



400 W Cesar Chavez
Austin, TX 78701

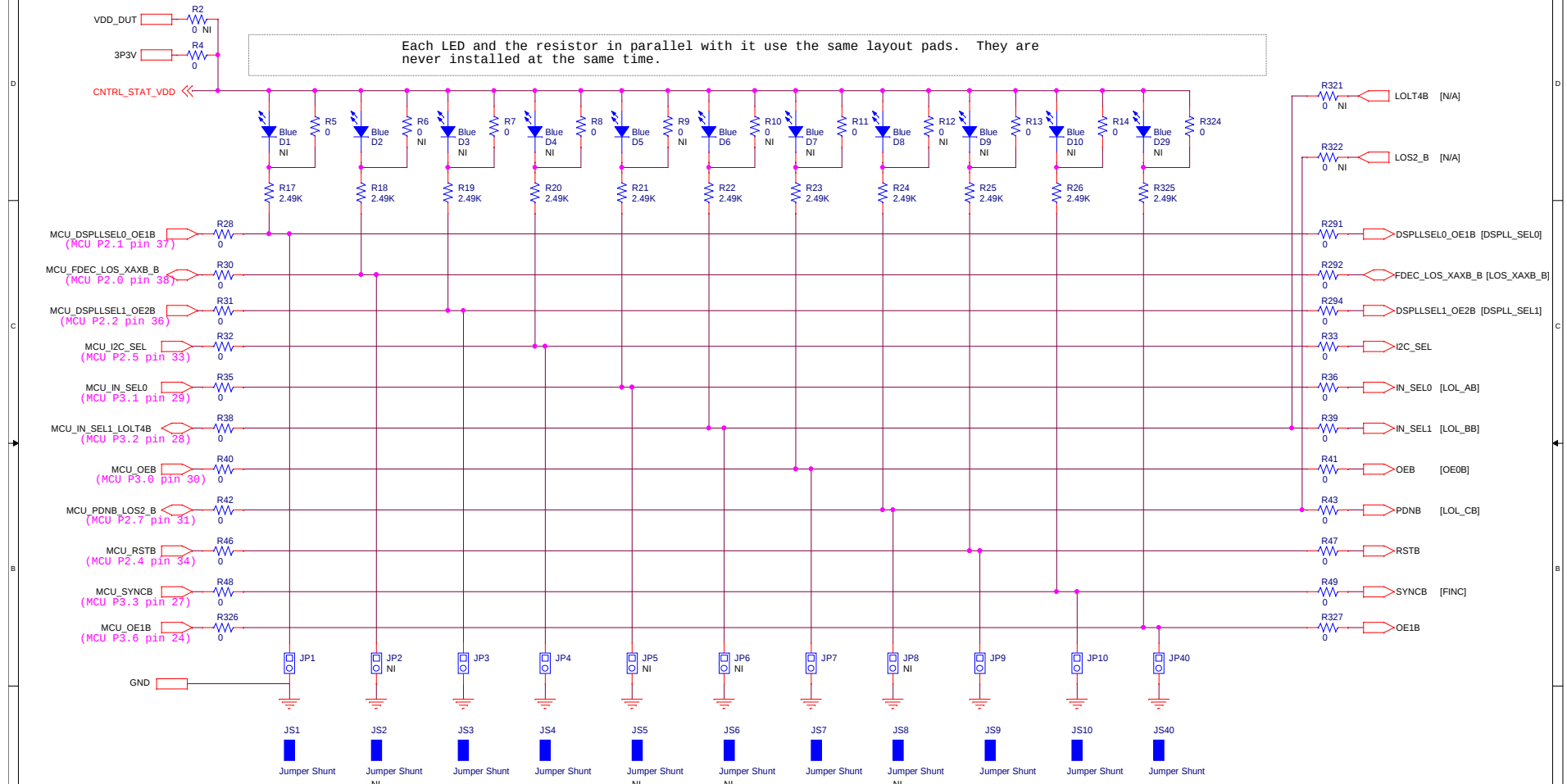
SILICON LABS

Title SI5347-EB_TOP_REVISION

Size	Document Number	Rev
B	SI5347-D-EB	2.2

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CONTROL PINS CONNECTIONS



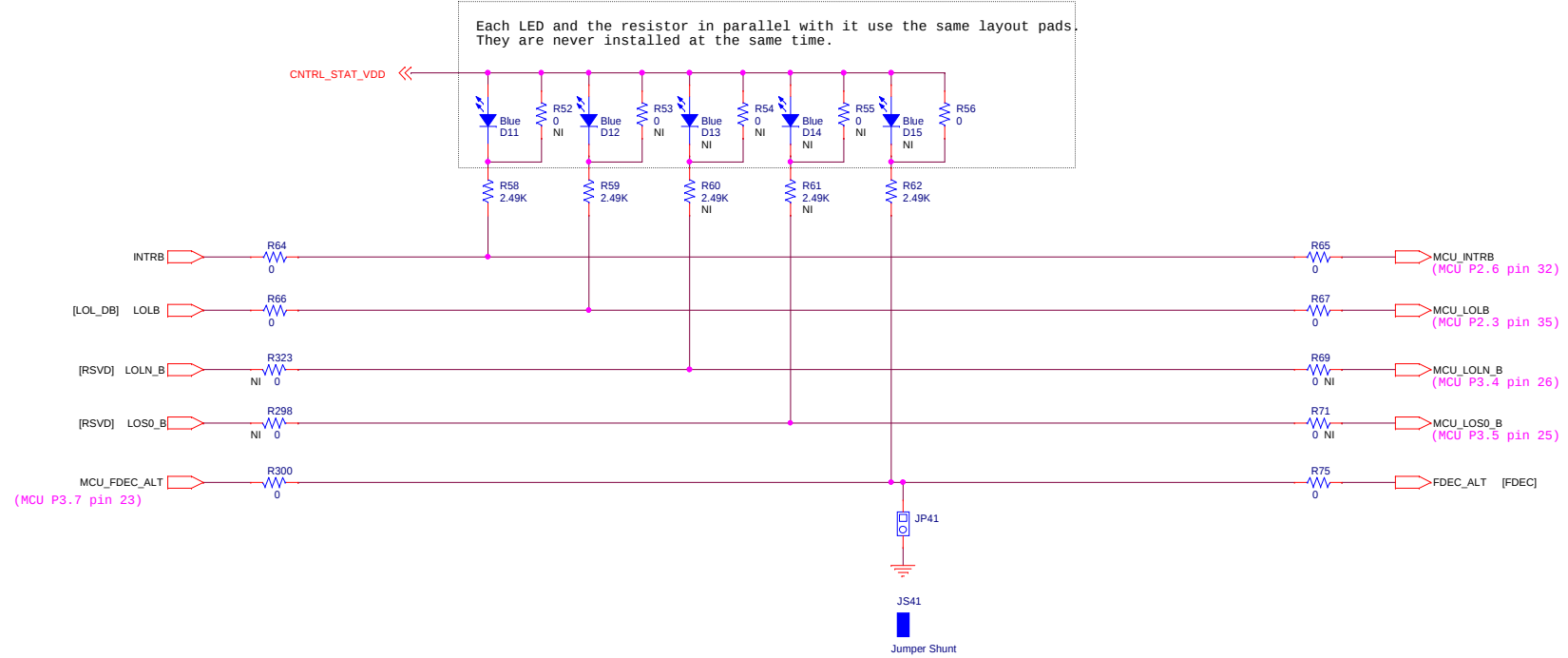
Note:

1. If the net name differs from the DUT pin name, the corresponding DUT pin name is enclosed in brackets. [DUT Pin Name]
2. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]

<Core Design>

400 W Cesar Chavez Austin, TX 78701		
Title		
CONTROL PINS_P1		
Size	Document Number	Rev
B	SI5347-D-EB	2.2
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CONTROL PINS CONNECTIONS



Note:

1. If the net name differs from the DUT pin name, the corresponding DUT pin name is enclosed in brackets. [DUT Pin Name]
2. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]

<Core Design>

400 W Cesar Chavez
Austin, TX 78701

SILICON LABS

Title CONTROL_PINS_P2

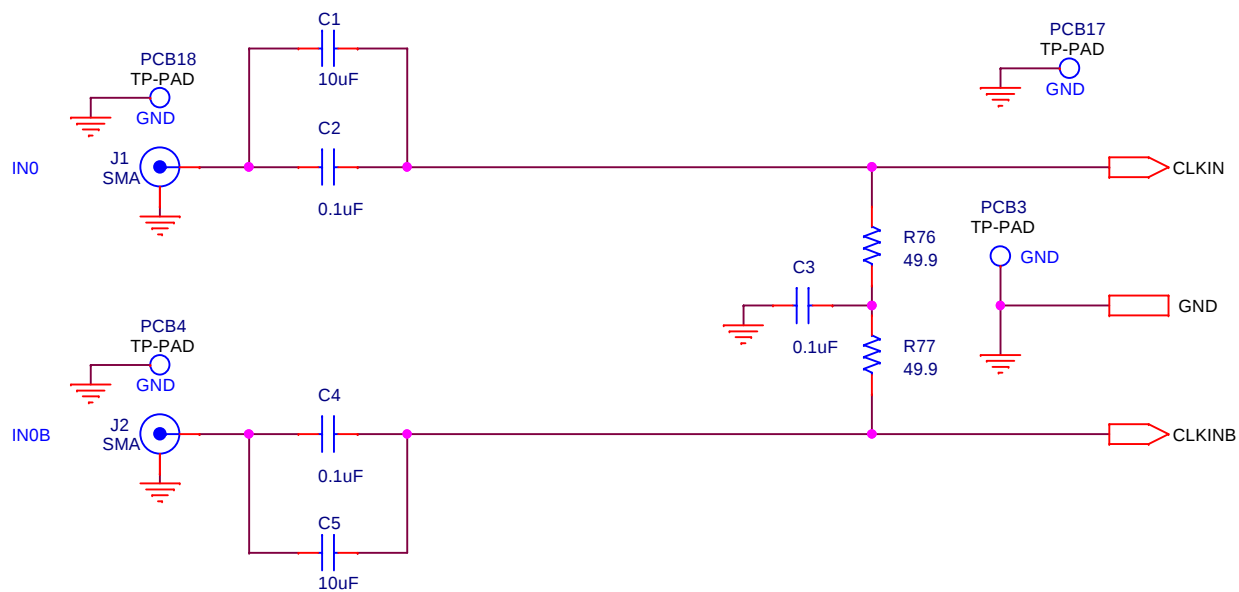
Size B

Document Number SI5347-D-EB

Rev 2.2

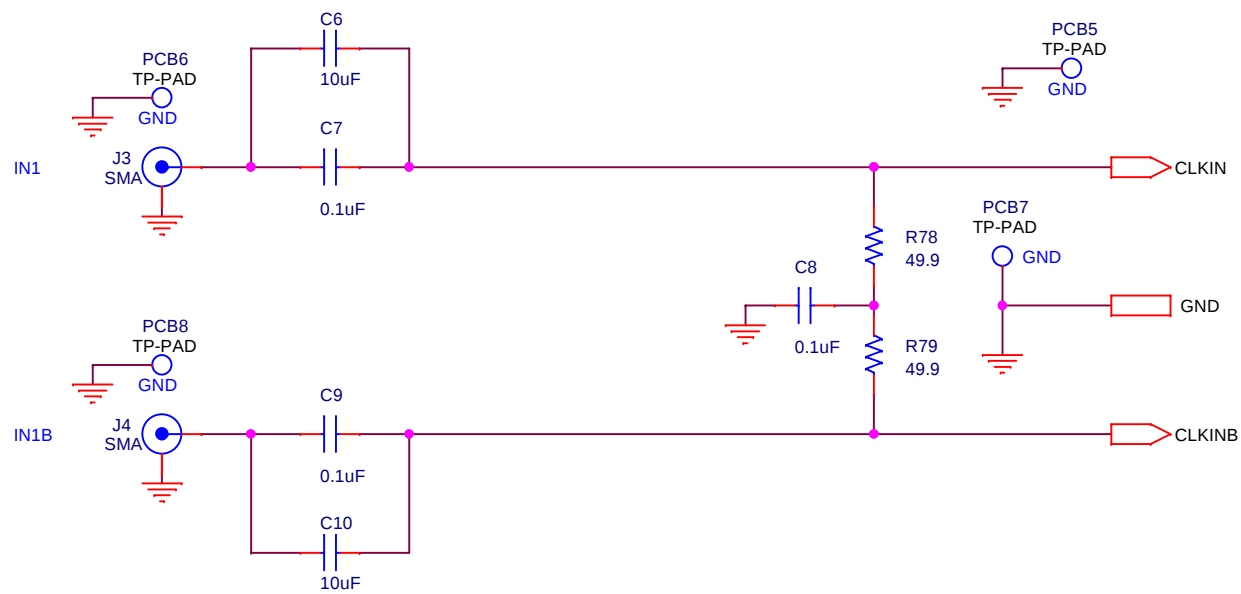
Date: Monday, April 11, 2016

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<Core Design>

 400 W Cesar Chavez Austin, TX 78701		
Title DIFF_INPUT_CLK		
Size A	Document Number SI5347-D-EB	Rev 2.2
Date:	Monday, April 11, 2016	Sheet 5 of 44



<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

DIFF_INPUT_CLK

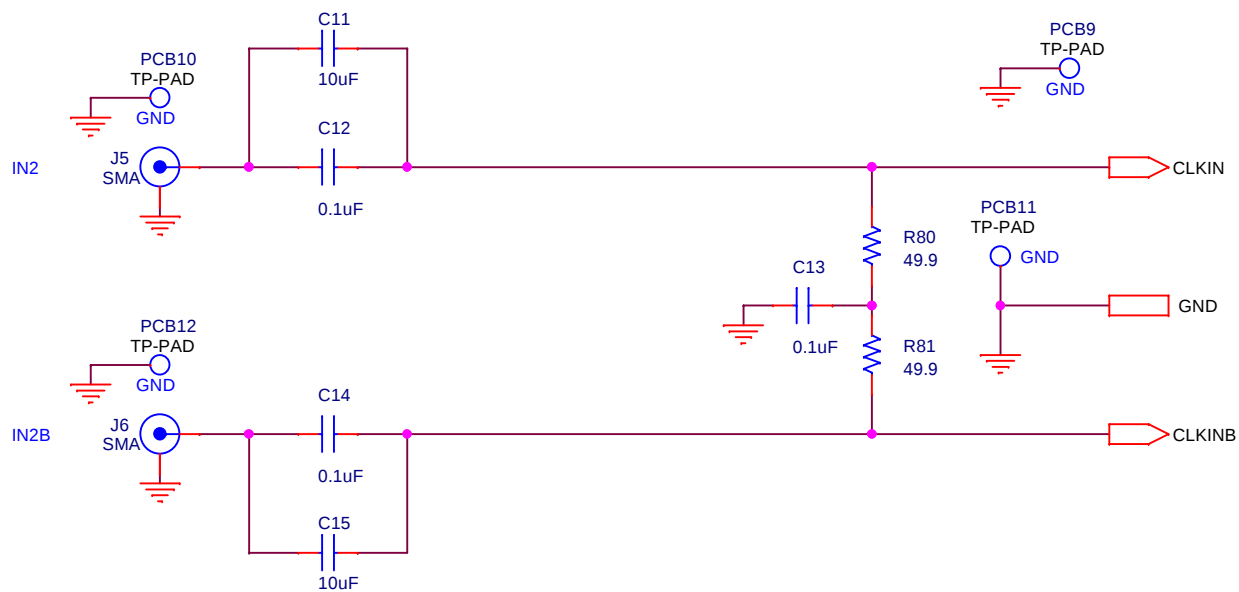
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Document Number
SI5347-D-EB

Rev
2.2

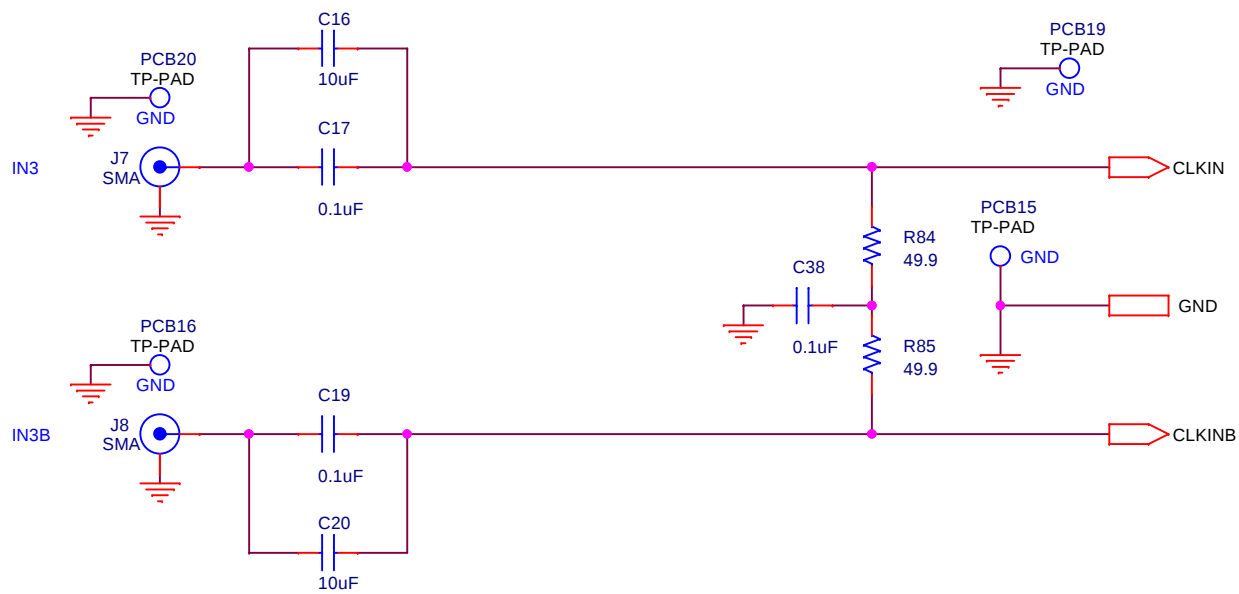
Date: Monday, April 11, 2016

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<Core Design>

 400 W Cesar Chavez Austin, TX 78701		
Title DIFF_INPUT_CLK		
Size A	Document Number SI5347-D-EB	Rev 2.2
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<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title
DIFF_INPUT_CLK

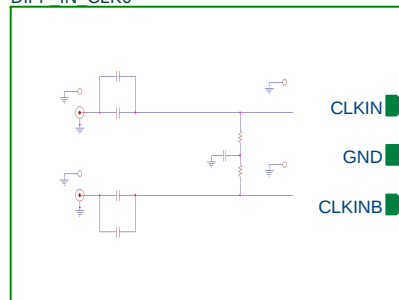
Size A Document Number
SI5347-D-EB

Rev
2.2

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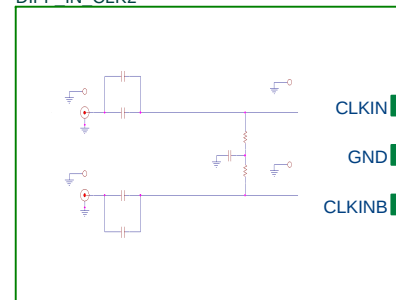
DIFF IN CLK0



CLKIN → CLKIN0
GND → GND
CLKINB → CLKIN0B

DIFF_INPUT_CLK

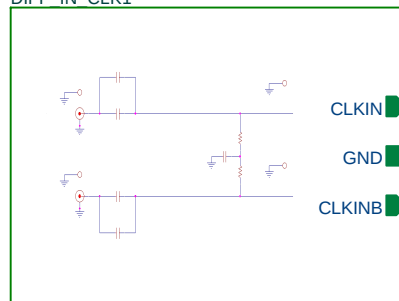
DIFF IN CLK2



CLKIN → CLKIN2
GND → GND
CLKINB → CLKIN2B

DIFF_INPUT_CLK

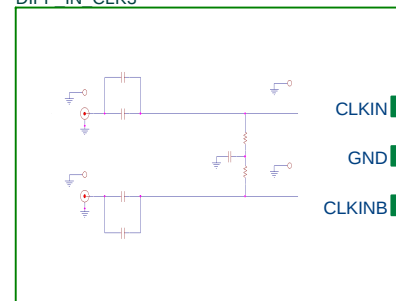
DIFF IN CLK1



CLKIN → CLKIN1
GND → GND
CLKINB → CLKIN1B

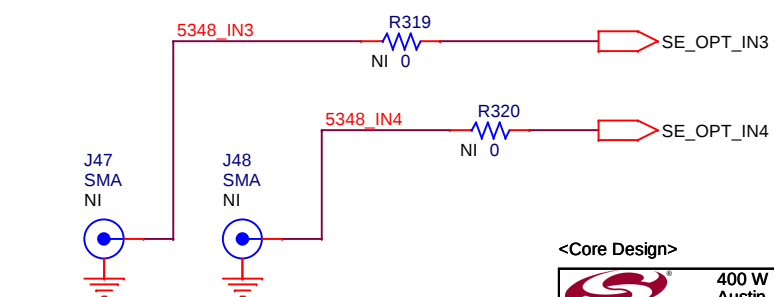
DIFF_INPUT_CLK

DIFF IN CLK3



CLKIN → CLKIN3
GND → GND
CLKINB → CLKIN3B

DIFF_INPUT_CLK



Single-ended clocks only.

<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

DIFF_INPUT_CLOCKS_4

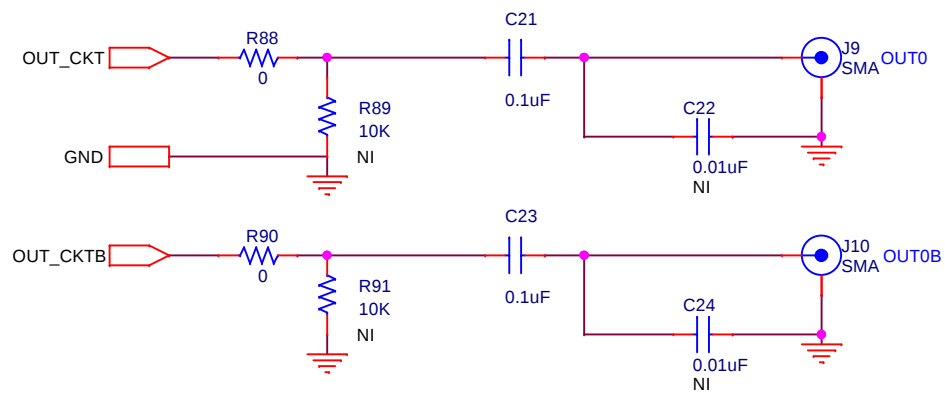
Size
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Document Number
SI5347-D-EB

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2.2

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<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

DIFF_OUTPUT_CLK

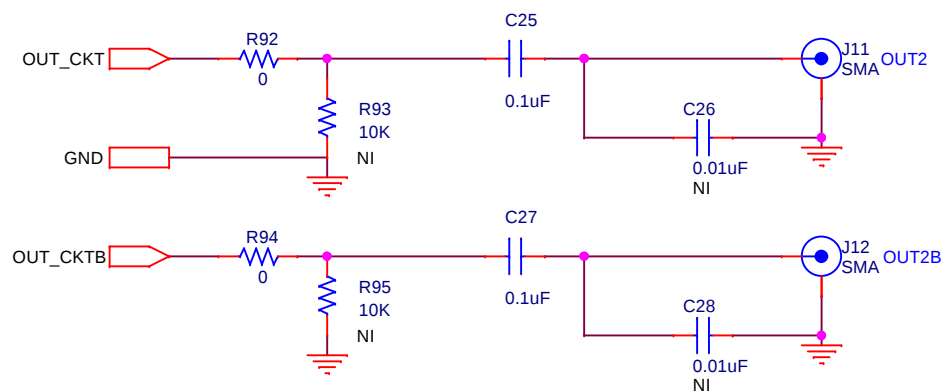
Size
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Document Number
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<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

DIFF_OUTPUT_CLK

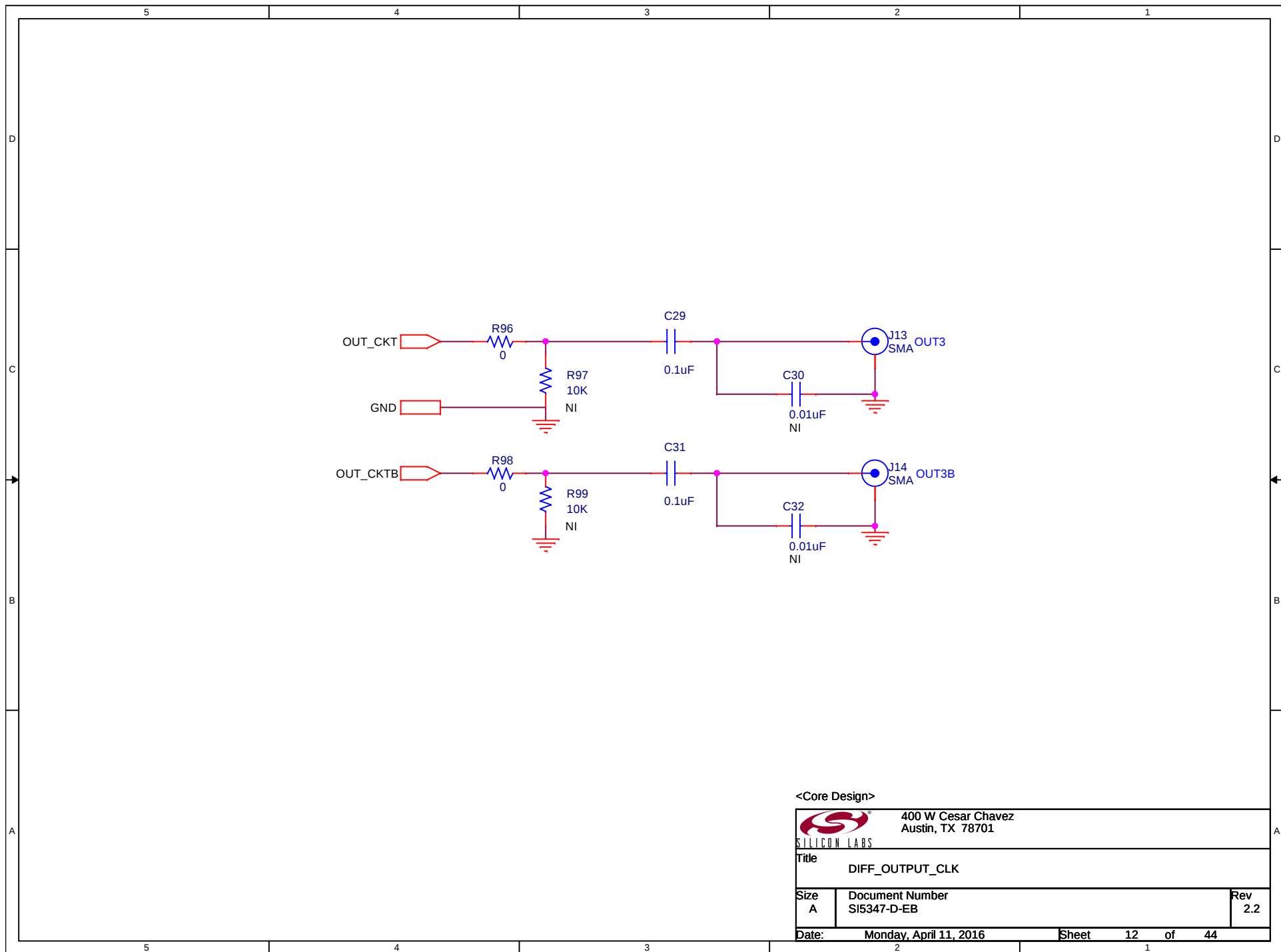
Size
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Document Number
SI5347-D-EB

Rev
2.2

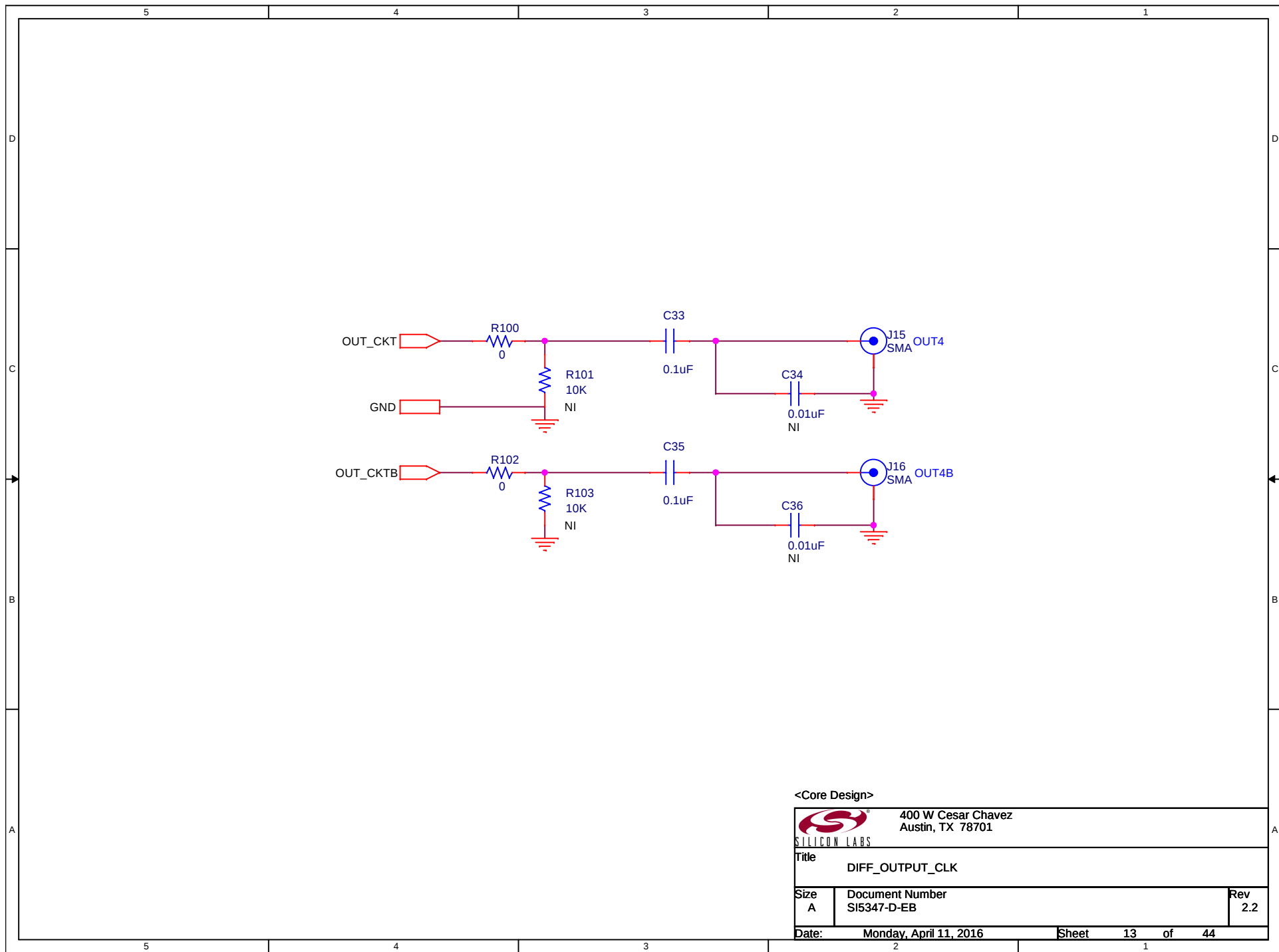
Date: Monday, April 11, 2016

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<Core Design>

 400 W Cesar Chavez Austin, TX 78701		
Title DIFF_OUTPUT_CLK		
Size A	Document Number SI5347-D-EB	Rev 2.2
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<Core Design>



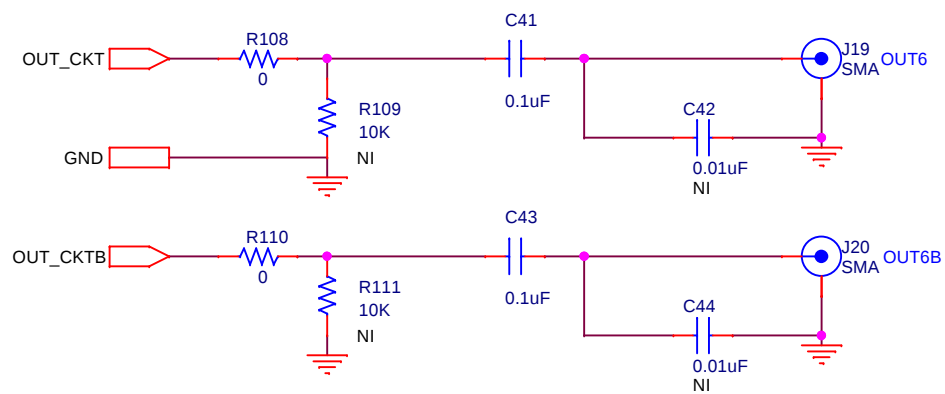
400 W Cesar Chavez
Austin, TX 78701

Title
DIFF_OUTPUT_CLK

Size
A Document Number
SI5347-D-EB

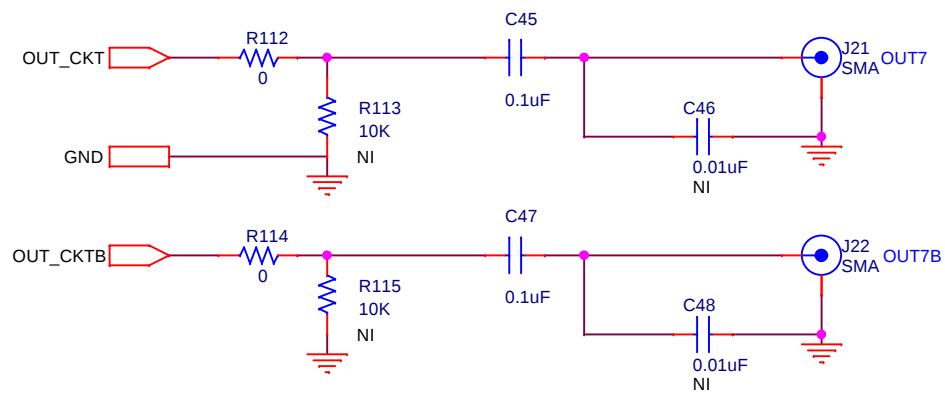
Rev
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<Core Design>

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Title DIFF_OUTPUT_CLK		
Size A	Document Number SI5347-D-EB	Rev 2.2
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<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

DIFF_OUTPUT_CLK

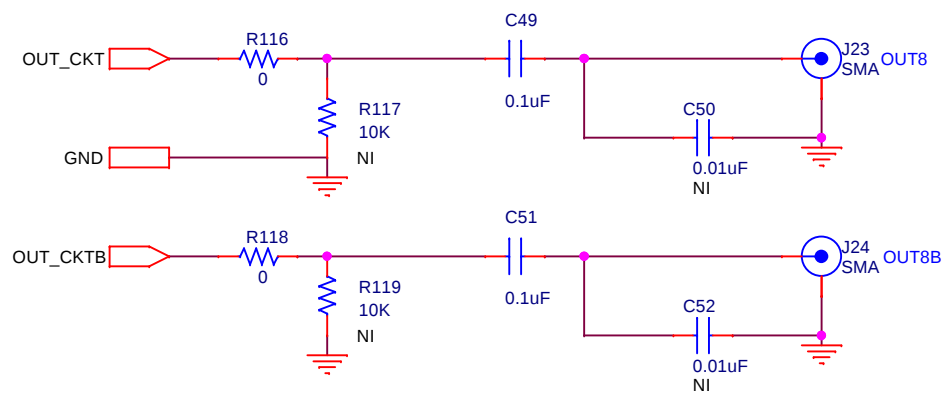
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Document Number
SI5347-D-EB

Rev
2.2

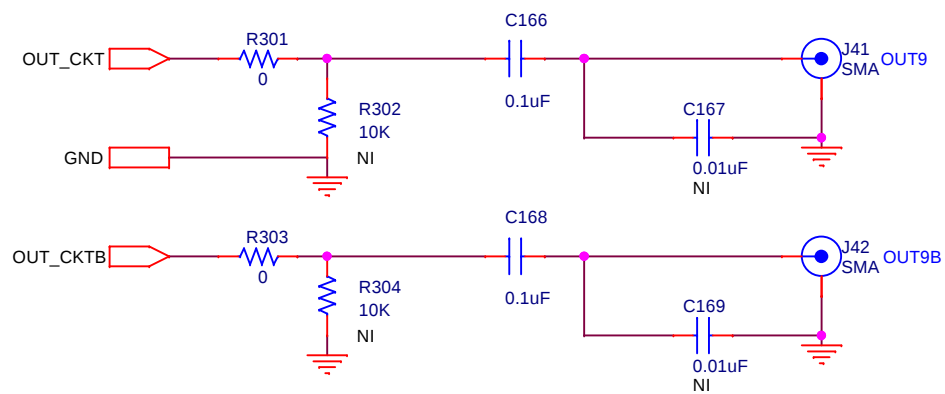
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<Core Design>

		400 W Cesar Chavez Austin, TX 78701
Title		
DIFF_OUTPUT_CLK		
Size A	Document Number SI5347-D-EB	Rev 2.2
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<Core Design>



400 W Cesar Chavez
Austin, TX 78701

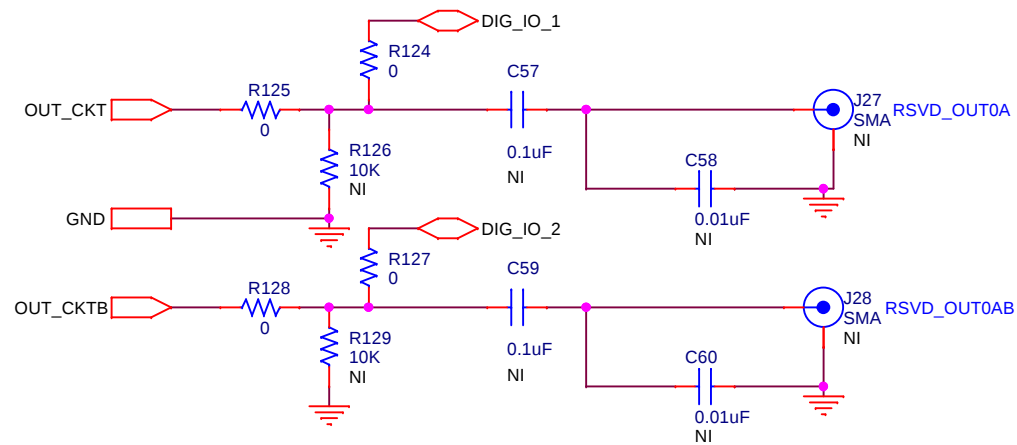
Title
DIFF_OUTPUT_CLK

Size
A Document Number
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DIFF_OUTPUT_CLK_DIG_IO



<Core Design>



400 W Cesar Chavez
Austin, TX 78701

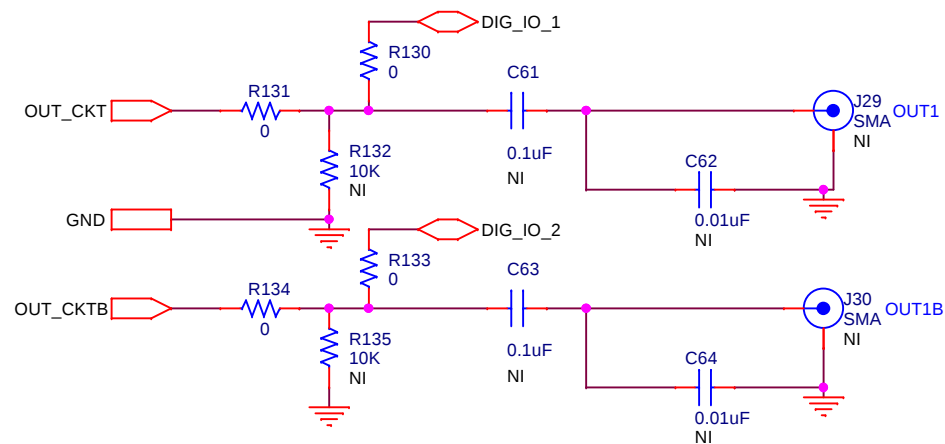
Title
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Size
A Document Number
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DIFF_OUTPUT_CLK_DIG_IO



<Core Design>



400 W Cesar Chavez
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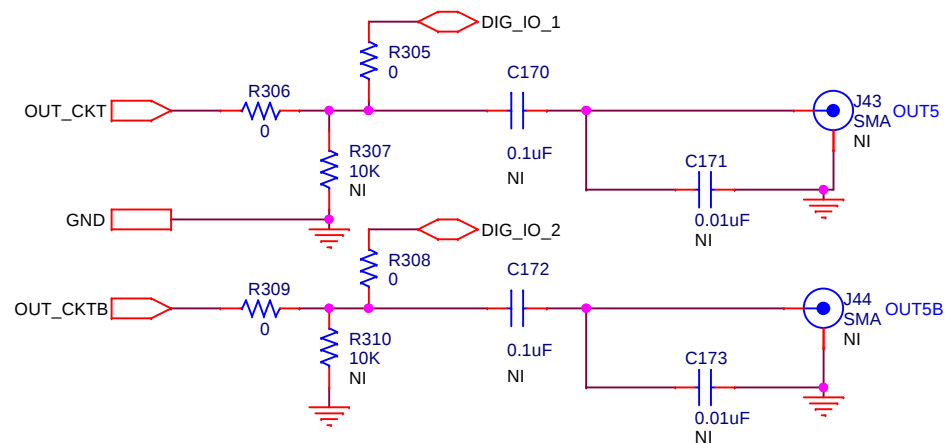
Title
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Size
A Document Number
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DIFF_OUTPUT_CLK_DIG_IO



<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

DIFF_OUTPUT_CLK_DIG_IO

Size
A

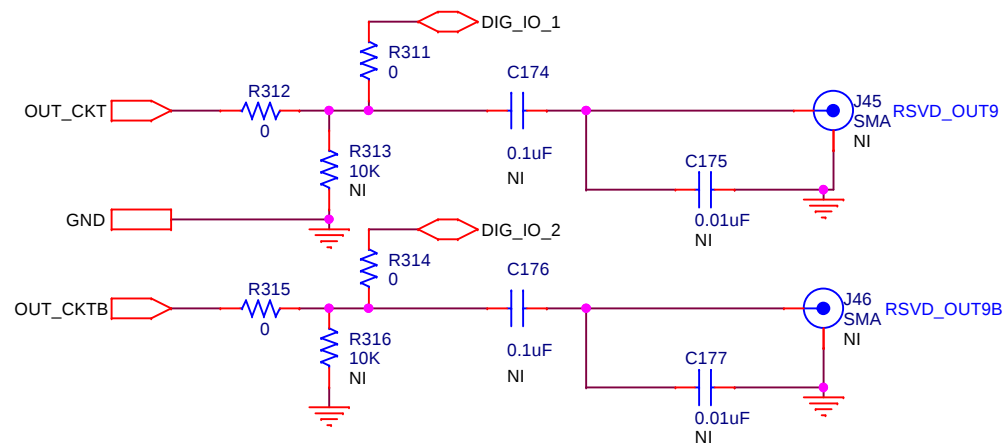
Document Number
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DIFF_OUTPUT_CLK_DIG_IO



<Core Design>



400 W Cesar Chavez
Austin, TX 78701

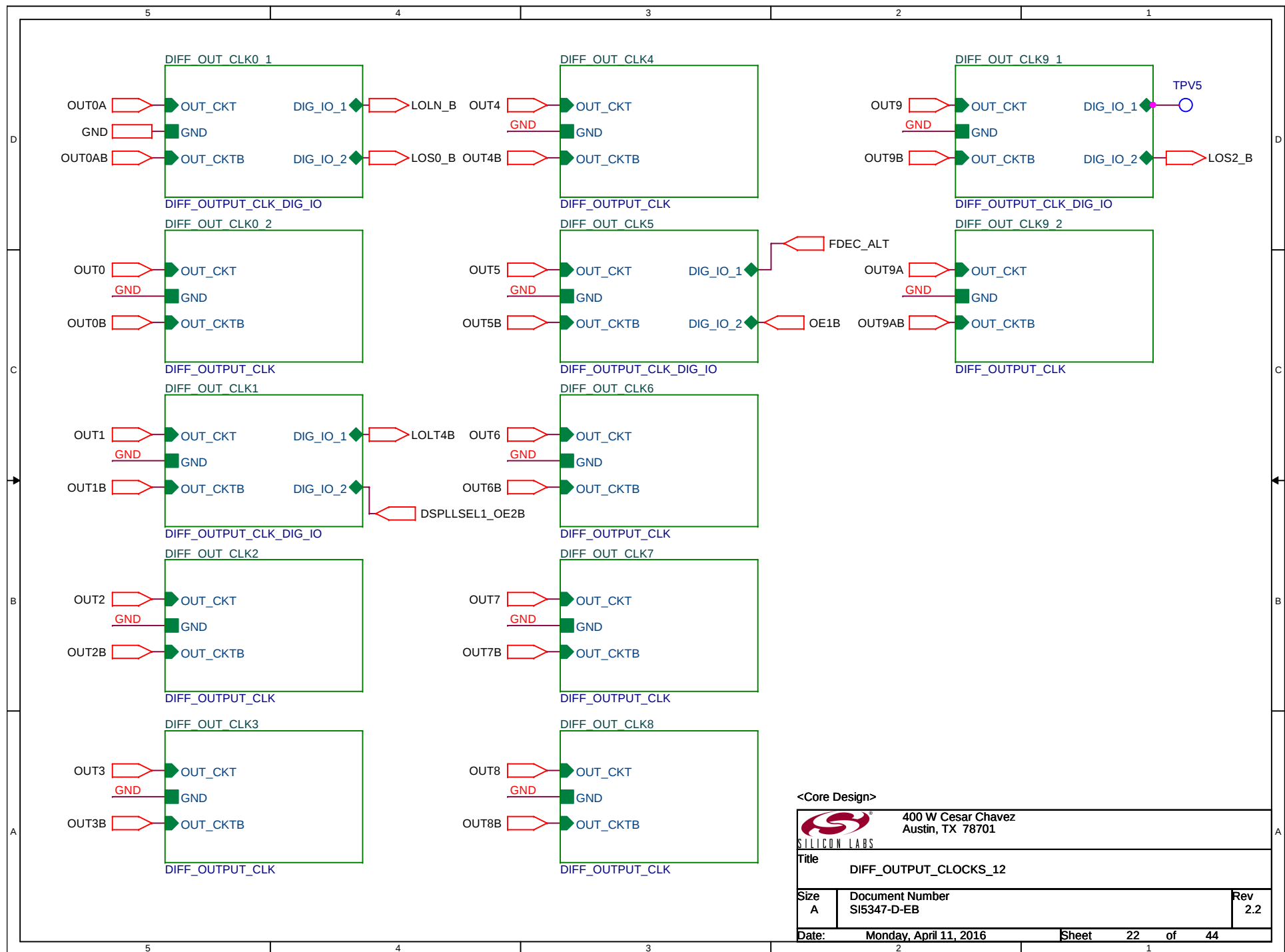
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Size A Document Number
SI5347-D-EB

Rev
2.2

Date: Monday, April 11, 2016

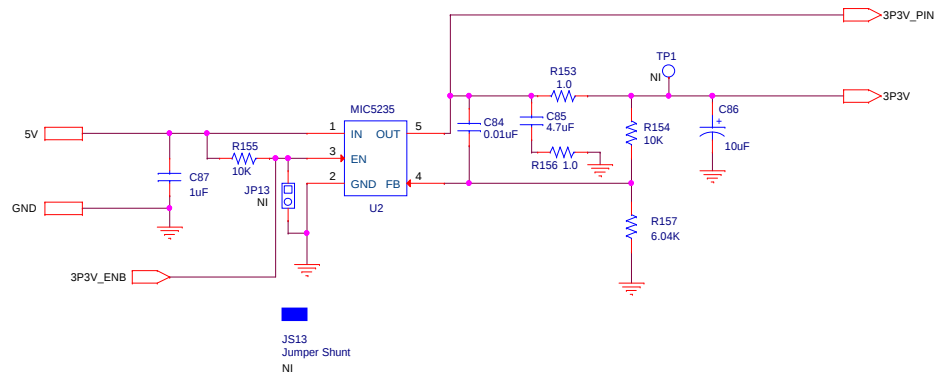
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<Core Design>

 SILICON LABS		400 W Cesar Chavez Austin, TX 78701	
Title DIFF_OUTPUT_CLOCKS_12			
Size A	Document Number SI5347-D-EB		Rev 2.2
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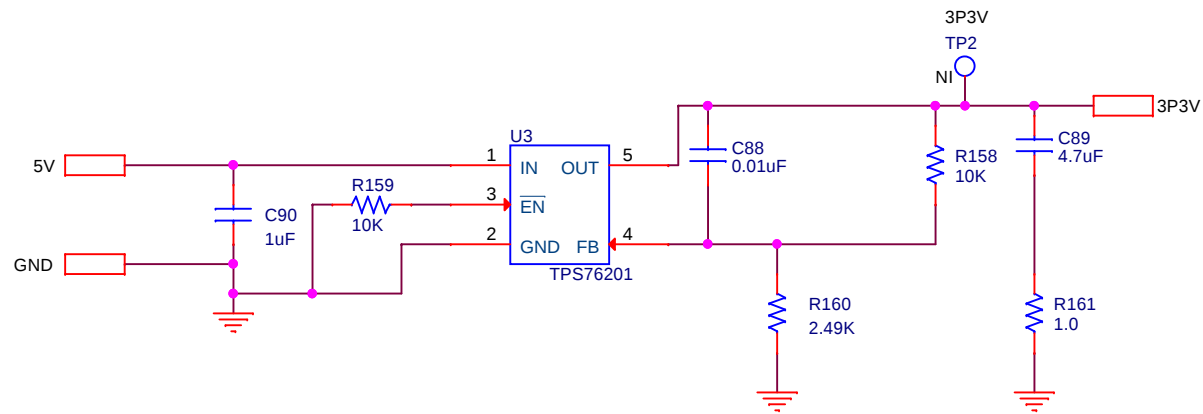
Fixed 3.3V 150 mA Voltage Regulator



3P3V_DUT (In Schematic)
VDDA DUT (Board Silkscreen)

 400 W Cesar Chavez Austin, TX 78701			
Title VDD_REG_TPS76201			
Size B	Document Number SI5347-D-EB	<Core Design>	Rev 2.2
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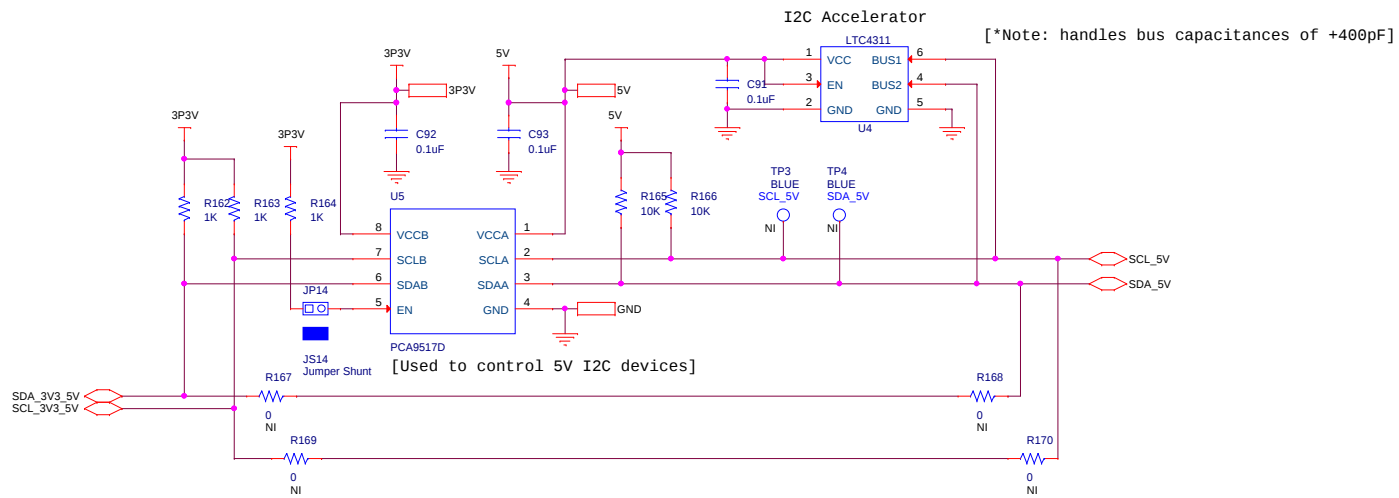
Fixed 3.3V 100 mA Voltage Regulator (Enabled, no current measurement supported.)



3P3V (In Schematic)
3P3V (Board Silkscreen)

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Title		FIXED_3V3_REG_TPS76201_EN_NO_IM	
Size A	Document Number SI5347-D-EB	<Core Design>	Rev 2.2
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I2C LEVEL TRANSLATORS



<Core Design>

400 W Cesar Chavez
Austin, TX 78701

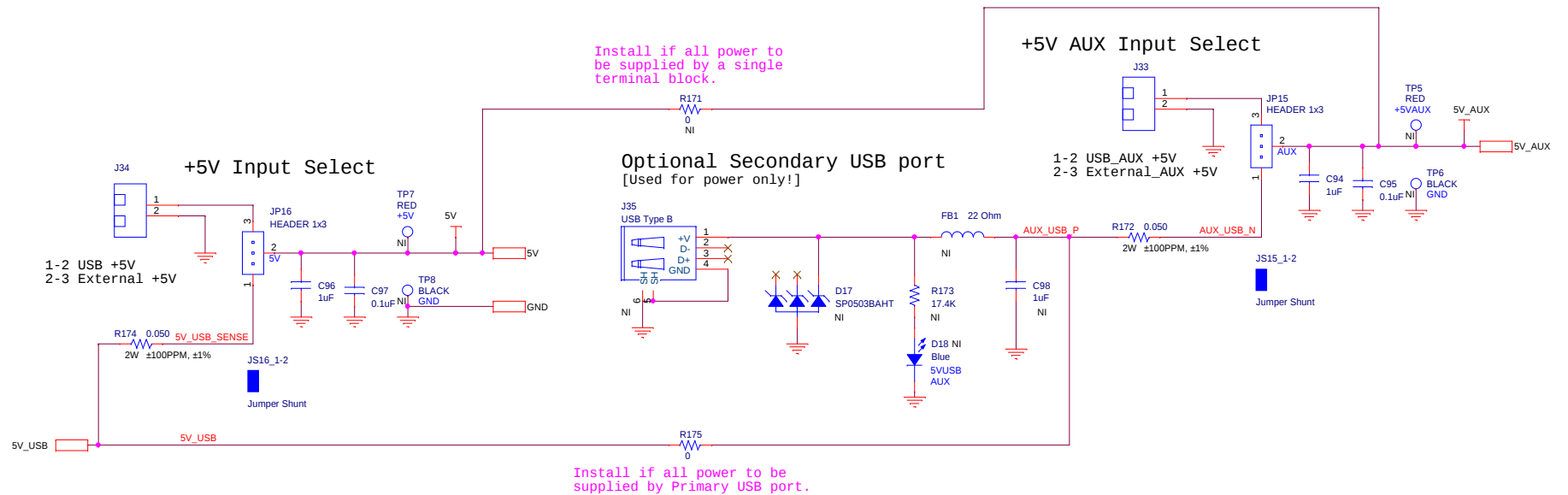
SILICON LABS

Title I2C_TRANSLATORS

Size B	Document Number SI5347-D-EB	Rev 2.2
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MAIN POWER INPUT SELECTS EXTERNAL OR USB



<Core Design>



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SILICON LABS

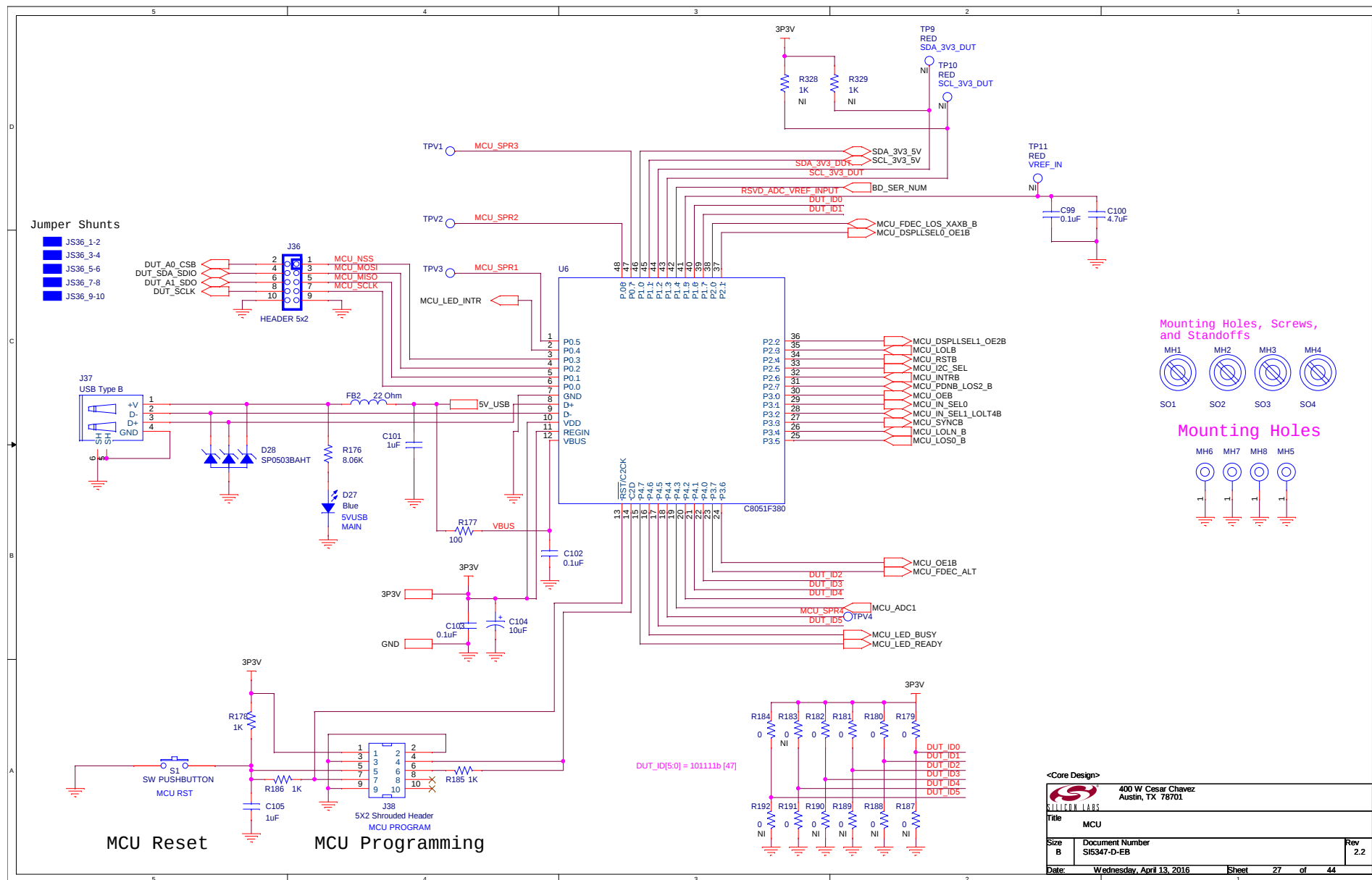
Title MAIN_POWER_CONNECTIONS

Size B Document Number SI5347-D-EB

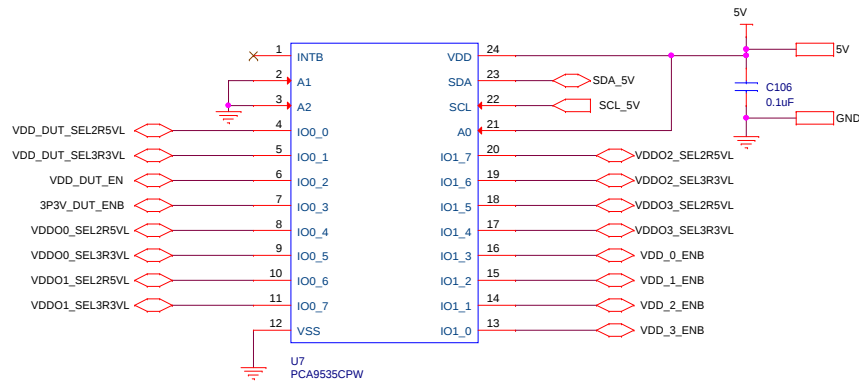
Rev 2.2

Date: Monday, April 11, 2016

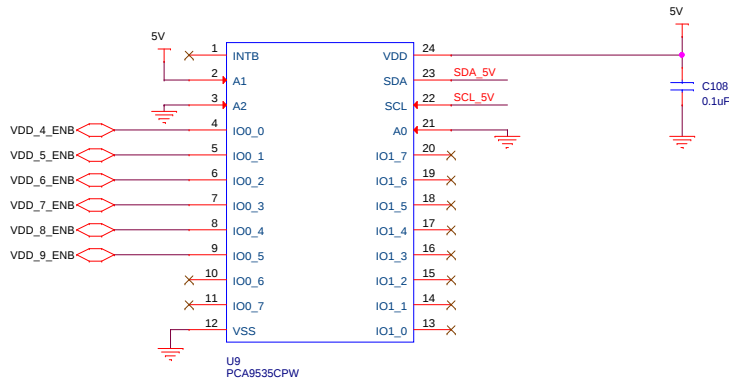
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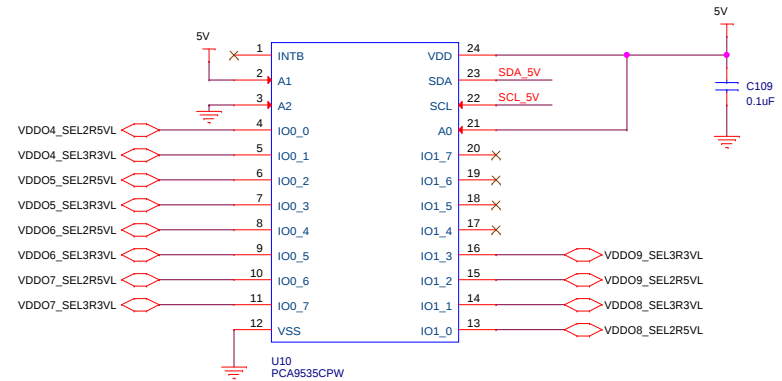
PERIPHERALS



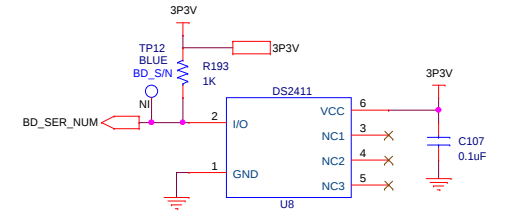
I2C VDD ENABLES/SELECTS FOR REGULATORS
I2C address: 0100001



I2C VDD ENABLES/SELECTS FOR REGULATORS
I2C address: 0100010



I2C VDD ENABLES/SELECTS FOR REGULATORS
I2C address: 0100011



Board Serial Number

<Core Design>



400 W Cesar Chavez
Austin, TX 78701

Title

PERIPHERALS

Size

B

Document Number

SI5347-D-EB

Rev

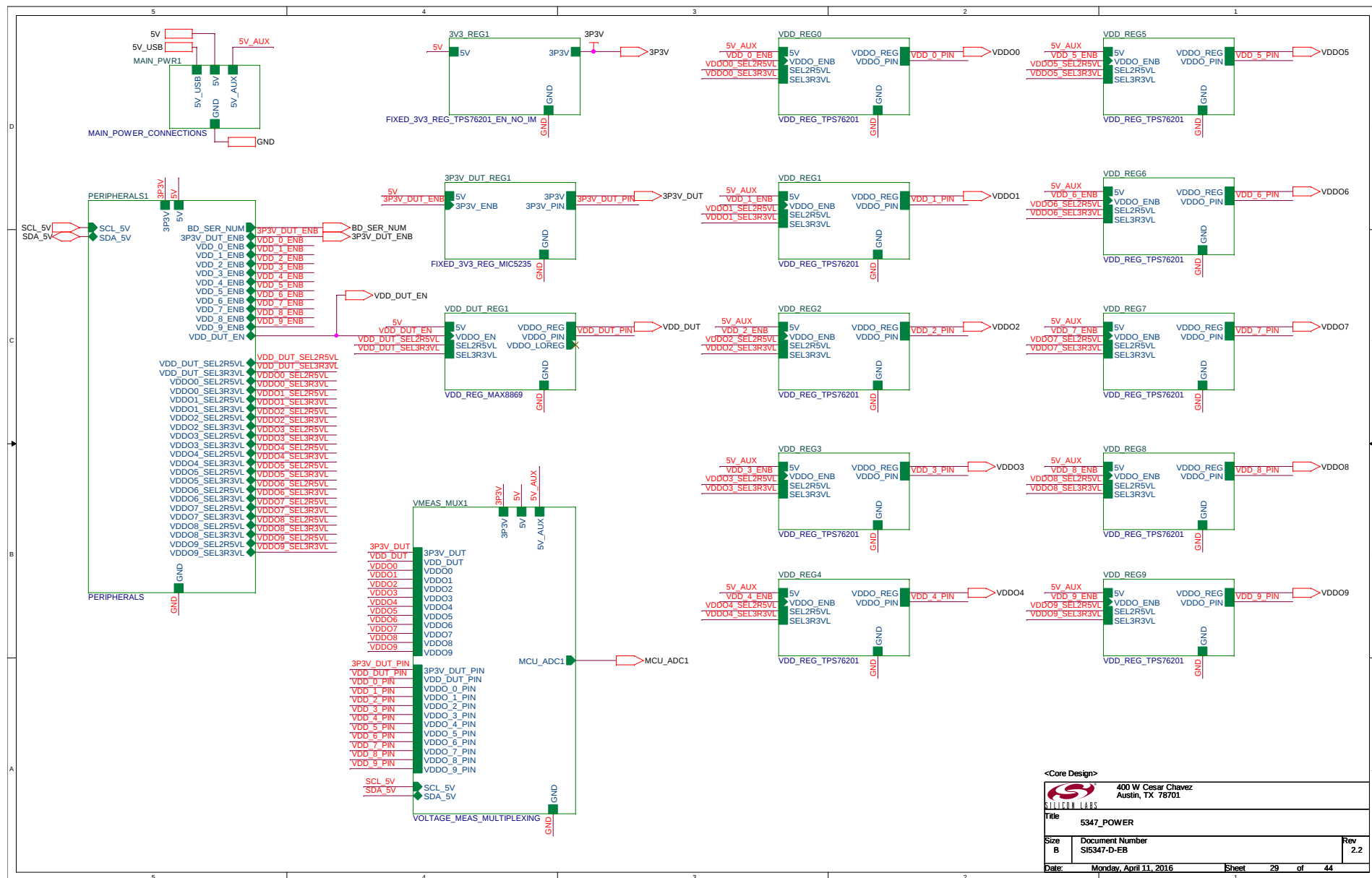
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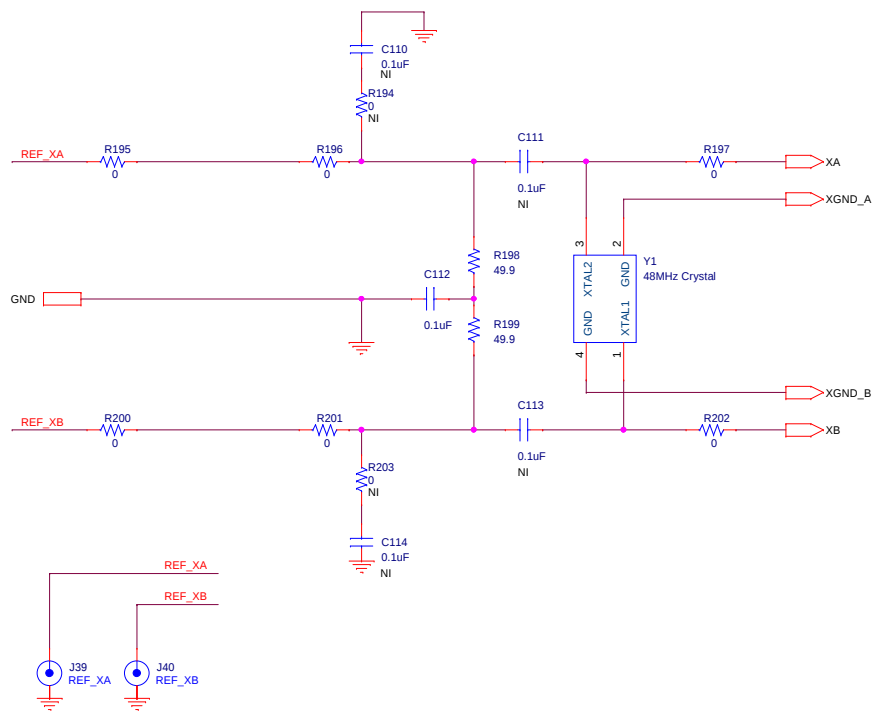
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REFERENCE INPUT CONNECTIONS



<Core Design>



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SILICON LABS

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Austin, TX 78701

400 W Cesar Chavez

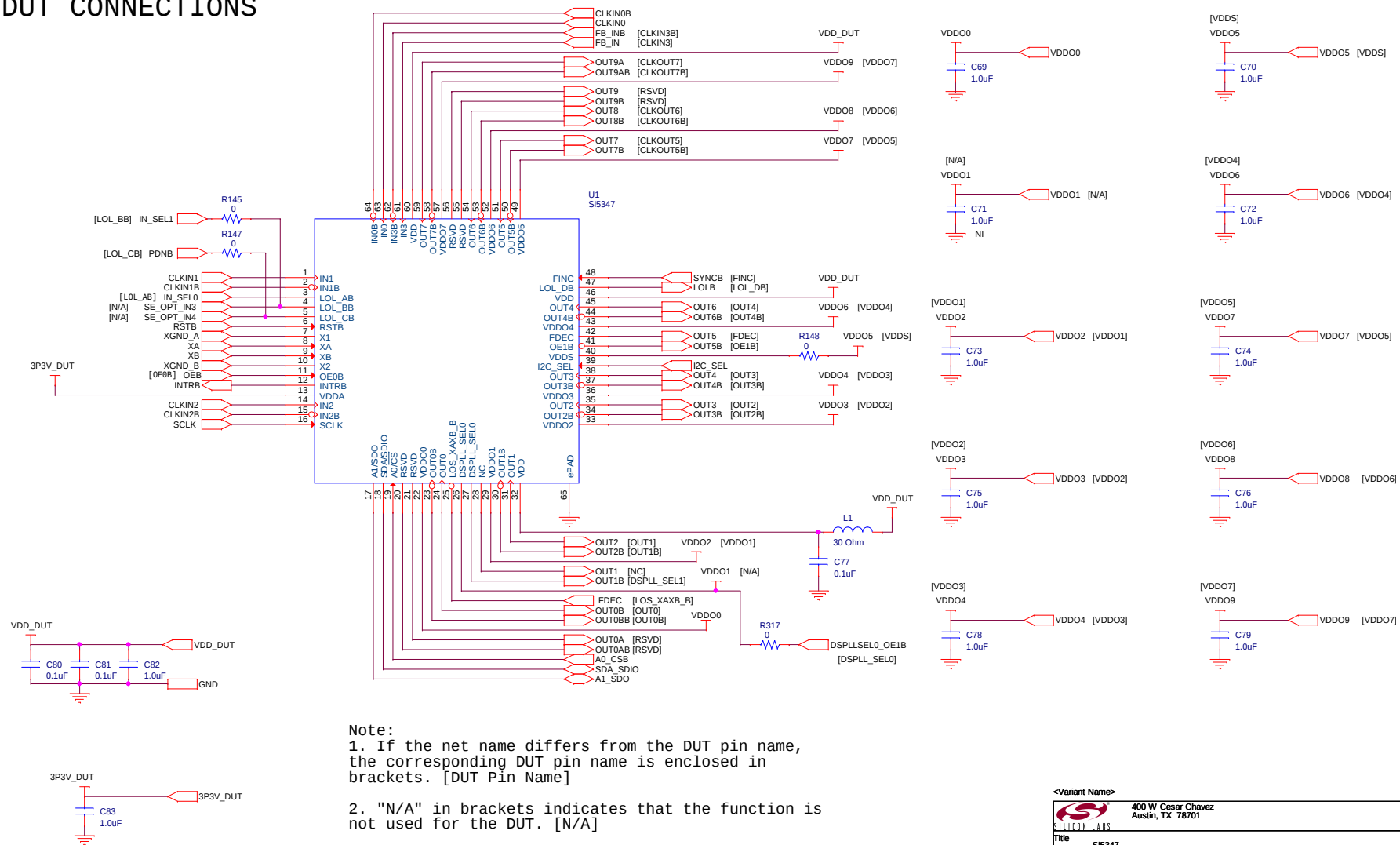
Austin, TX 78701

400 W Cesar Chavez

Austin, TX 78701

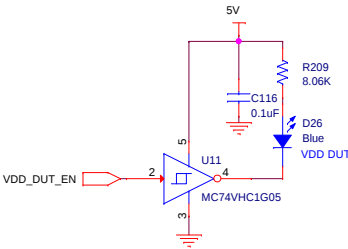
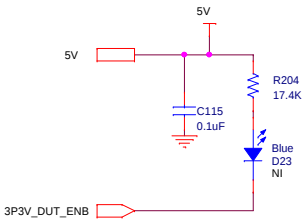
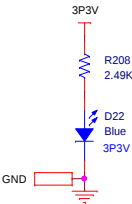
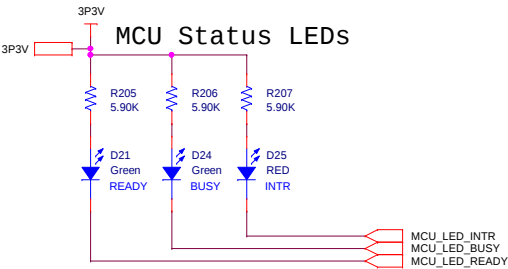
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Size	Document Number	Rev
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DUT CONNECTIONS

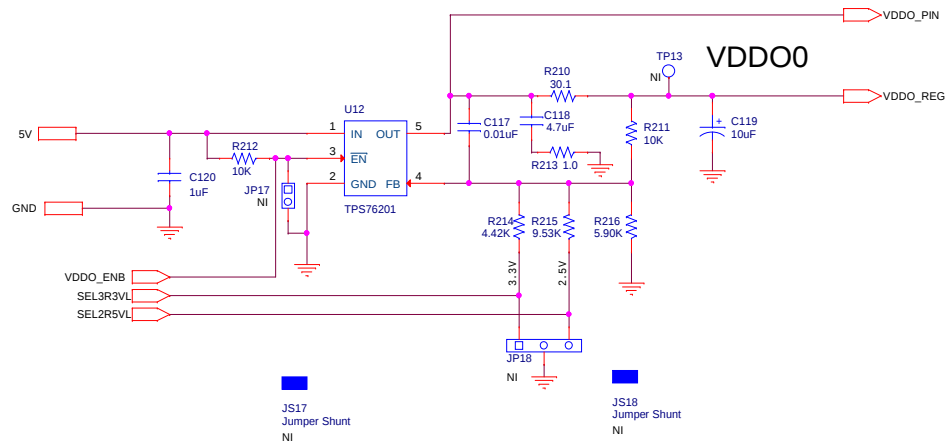


<Variant Name>		
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Title SI5347		
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LEDS - SUPPLIES & STATUS

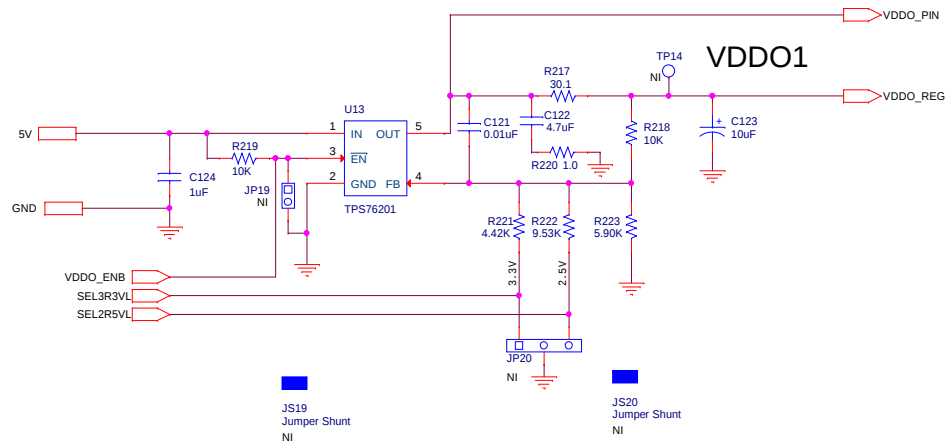


100 mA Adjustable Voltage Regulator



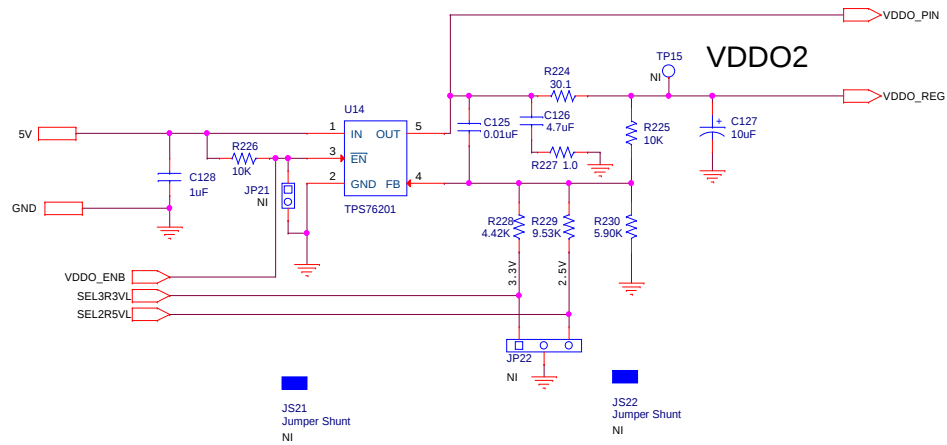
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Title VDD_REG_TPS76201			
Size B	Document Number SI5347-D-EB	<Core Design>	Rev 2.2
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100 mA Adjustable Voltage Regulator



 400 W Cesar Chavez Austin, TX 78701			
Title			
VDD_REG_TPS76201			
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100 mA Adjustable Voltage Regulator



 400 W Cesar Chavez Austin, TX 78701			
Title			
VDD_REG_TPS76201			
Size	Document Number	<Core Design>	Rev
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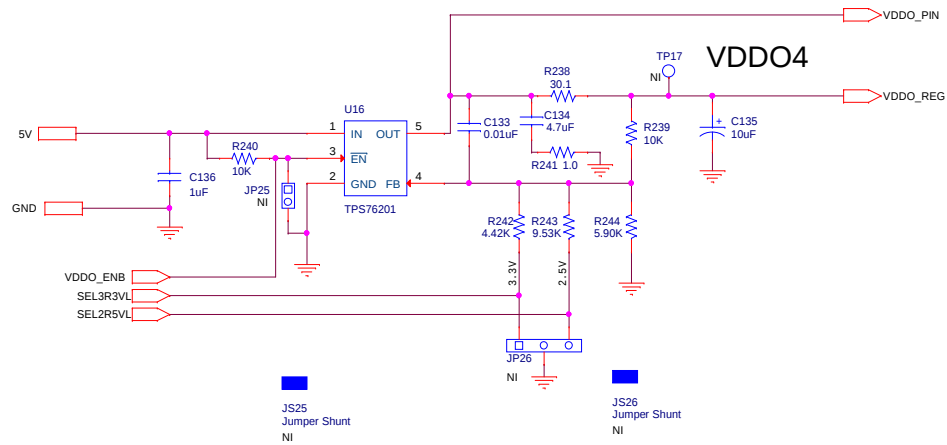
100 mA Adjustable Voltage Regulator

The schematic diagram illustrates a 100 mA Adjustable Voltage Regulator circuit. The circuit is powered by a 5V input and a GND connection. The input is connected to the IN pin of the TPS76201 (U15) through a 10k resistor (R233) and a 1uF capacitor (C132). The output of the regulator (U15) is connected to a 10k resistor (R232) and a 10uF capacitor (C131). The output voltage is labeled VDDO3 and VDDO_REG. The circuit also includes a 3.3V and 2.5V output section with resistors R235 (4.42k), R236 (9.53k), and R237 (5.90k). A 1.0 resistor (R234) is connected to the feedback pin (FB). The circuit is labeled with various components and their values.

Size	Document Number	Rev
B	SI5347-D-EB	2.2

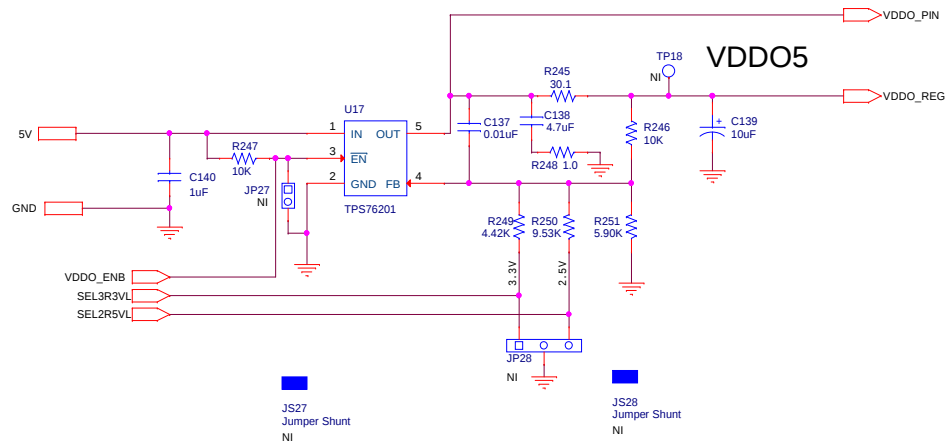
Date: Monday, April 11, 2016 Sheet 36 of 44

100 mA Adjustable Voltage Regulator



 400 W Cesar Chavez Austin, TX 78701			
Title			
VDD_REG_TPS76201			
Size	Document Number	<Core Design>	Rev
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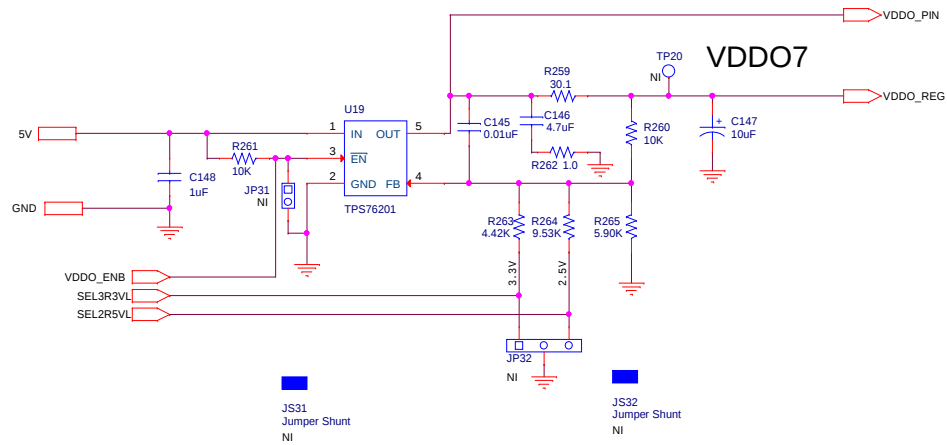
100 mA Adjustable Voltage Regulator



 400 W Cesar Chavez Austin, TX 78701			
Title			
VDD_REG_TPS76201			
Size	Document Number	<Core Design>	Rev
B	SI5347-D-EB		2.2
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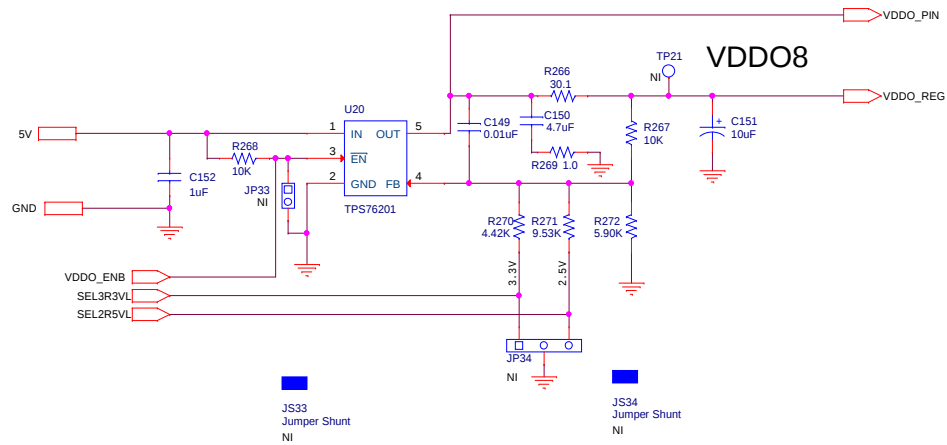
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100 mA Adjustable Voltage Regulator



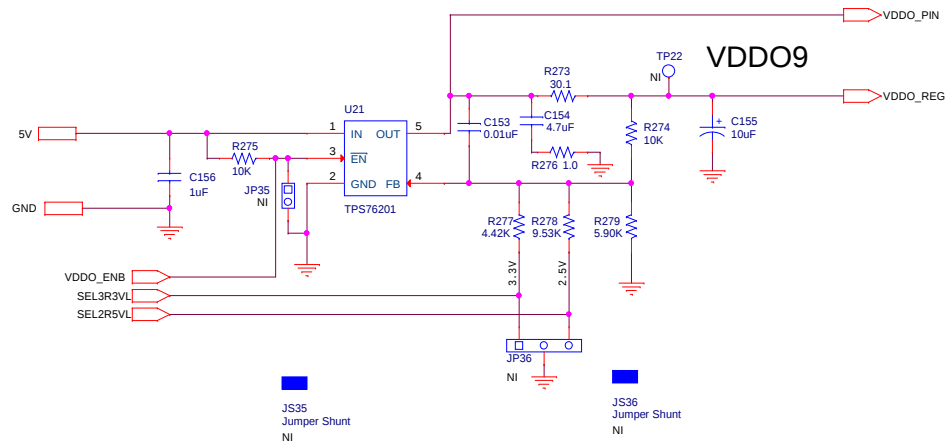
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Title			
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Size	Document Number	Rev	
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100 mA Adjustable Voltage Regulator

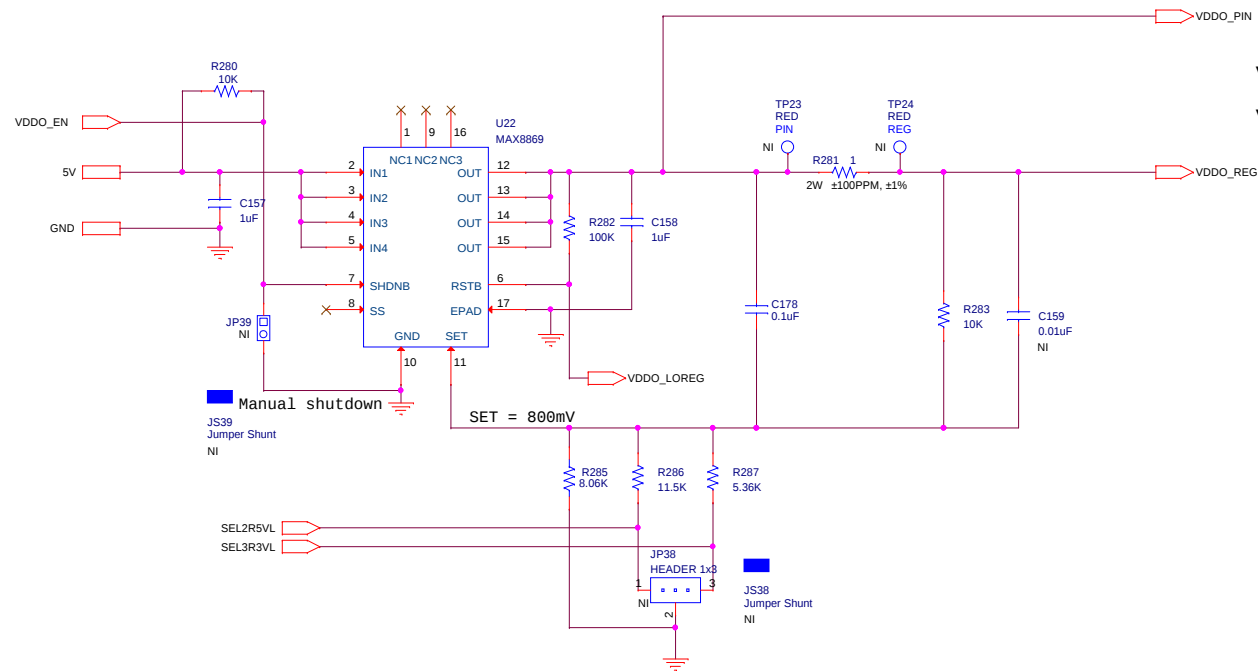


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100 mA Adjustable Voltage Regulator



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VDD_DUT (In Schematic)
VDD DUT (Board Silkscreen)

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VDD_REG_MAX8869		
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VOLTAGE MEASUREMENT MULTIPLEXING

