USER GUIDE

UG531: Skyworks Pluto Evaluation Platform

Features

- The Skyworks Pluto Evaluation Board (EVB) is used with Skyworks ClockBuilder Pro® (CBPro) software to evaluate SKY63104, SKY63105, SKY63106, SKY62101, SKY69102, SKY69003, and SKY63001.
- Powered by a single 5 V dc adapter included in the evaluation kit
- Flexible power supply tree allows evaluation of both LDOs and dc-dc converter
- Low dropout (LDO) voltages programmable to 3.3 V, 2.5 V, and 1.8 V using the CBPro EVB GUI
- Current, voltage, and power sensing per LDO
- Onboard OCXO, TCXO, XO and crystal as well as SubMiniature version A (SMA) connectors to connect external oscillators
- SMA connectors for clock inputs and outputs
- Status LEDs for the device under test (DUT) GPIO status pins
- Header pins for the DUT GPIO control pins
- Onboard temperature sensor

Description

The Skyworks Pluto Evaluation Platform is used for evaluating clock devices that utilize fifth-generation DSPLL® and MultiSynth™ technologies in an 8 x 8 mm quad flat no-lead (QFN) package. This document covers all ordering option variants of the Pluto Evaluation Platform. See “12. Ordering Information” on page 31 for more details on supported clock devices. The supported devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) or external flash memory, which allow power-up with a known frequency configuration. The EVB is designed to be used in conjunction with CBPro software to evaluate the configuration and performance of the clock device.

The exact Skyworks device and revision is distinguished by a white label underneath the silkscreen name on the board. Strictly for ordering purposes, the terms “EB” and “EVB” refer to the board and kit, respectively. In this document, the terms are synonymous.

1. Functional Block Diagram

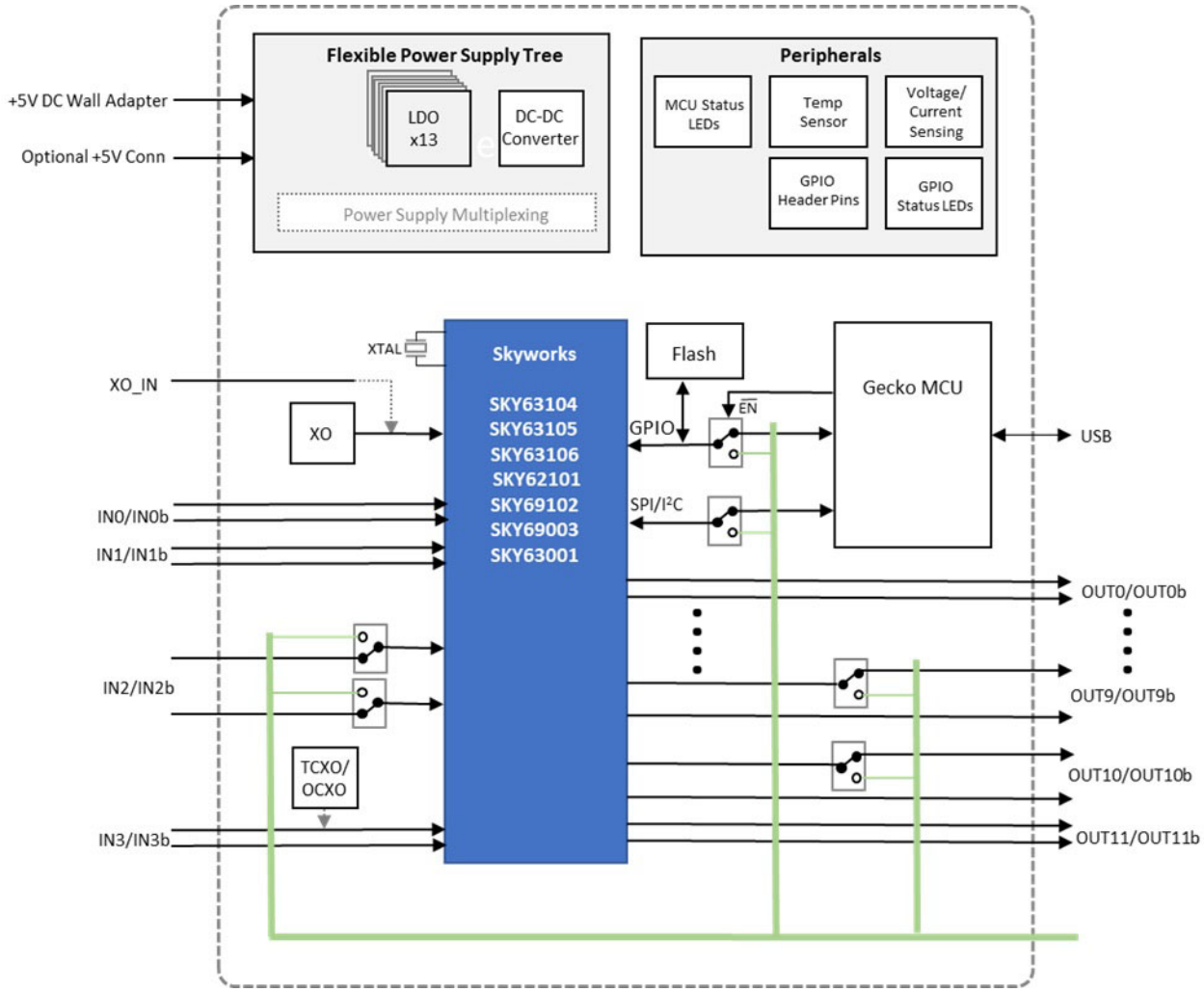

Figure 1. Evaluation Board Block Diagram

2. Quick Start Guide

When first receiving the Pluto EVB, configure the jumper settings as shown in Figure 2 to ensure that the DUT receives power and signal communications. Jumpers that require installation are shown in green and jumpers that need to be uninstalled are shown in red.

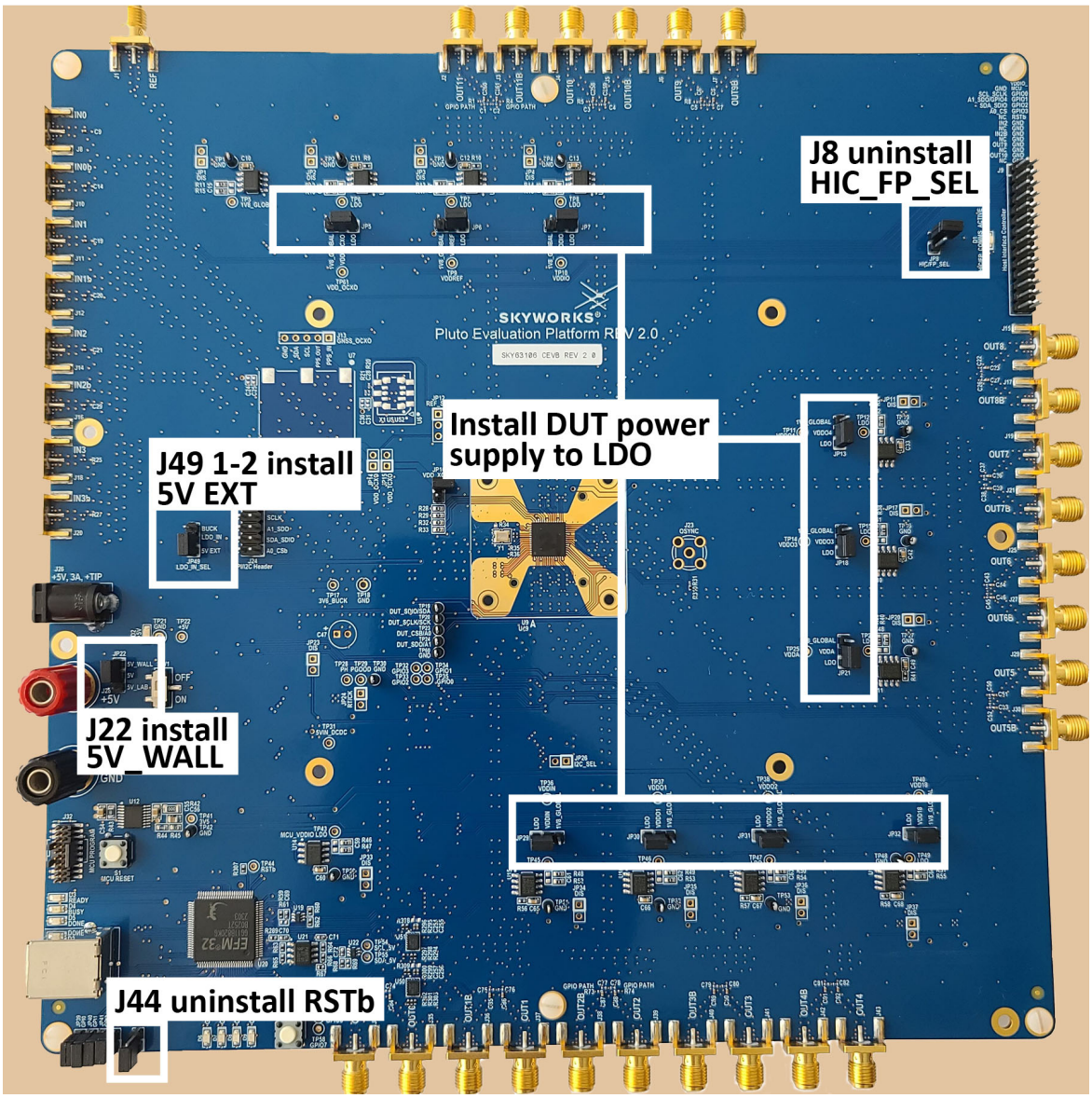

Figure 2. Evaluation Board Quick Start Jumper Setting

After the jumpers are installed correctly as shown above, plug the 5 V dc adapter included in the EVB kit into the J26 barrel plug, then plug in the included USB cable. Turn SW1 to "ON." VDDA/VDDREF/VDDIO/VDD_OCXO/ VDDIN regulators are set to 3.3 V and VDD18/1V8 Global is set to 1.8 V. VDDO1-VDDO4 remains OFF.

After turning the board on, a frequency plan may be written to the DUT. "3. Using the EVB with ClockBuilder Pro" on page 4 briefly covers using ClockBuilder Pro with the EVB as a quick start guide. For more guidance on using ClockBuilder Pro and creating a frequency plan, see the reference manual.

3. Using the EVB with ClockBuilder Pro

The EVB is designed to work alongside ClockBuilder Pro to streamline the development process. The following example uses the SKY63104-A-EVB for reference. To get started with a sample frequency plan, open ClockBuilder Pro and select “Open Sample Project” (Figure 3). Select the application by function or application, or directly search by the DUT part number for the project you are trying to build (Figure 4).

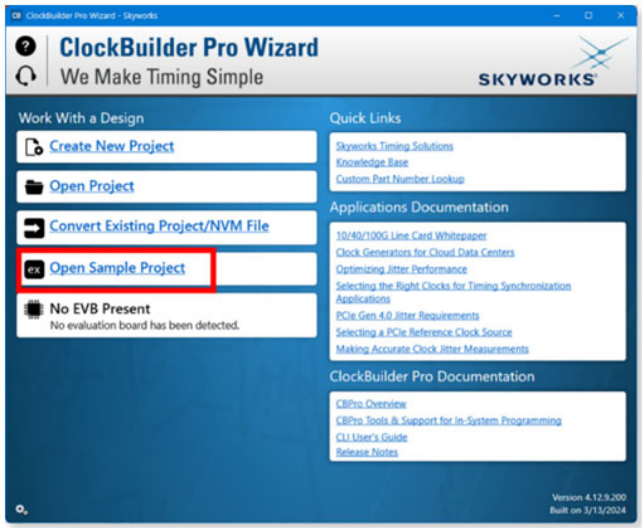

Figure 3. Opening a Sample Project in CBPro

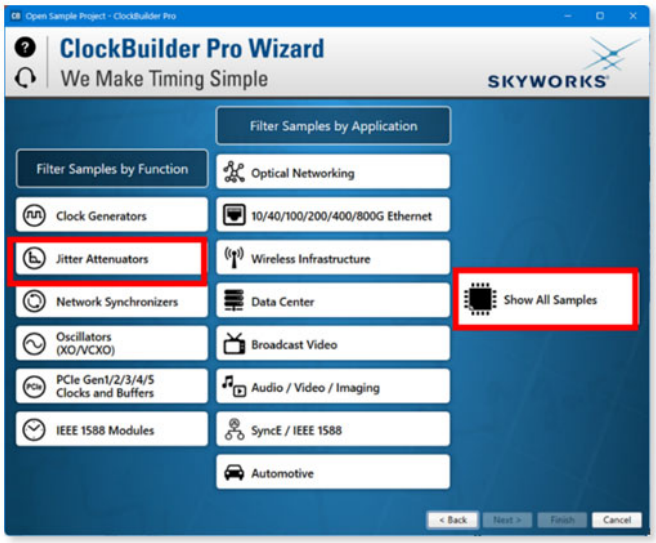

Figure 4. Selecting a Project Sample in CBPro

The user may modify the sample project or create a new project from scratch following the Configuration Wizard. If the EVB USB is plugged into a PC with power on, it appears under “Evaluation Board Detected.” Make sure there is no error warning displayed in the GUI so the opened frequency plan can then be written to the DUT by clicking **Write DUT Volatility** (Figure 5). The user plan writes to the DUT RAM, which is volatile after a power cycle/hard reset. For more details on writing a plan to the DUT NVM or external flash memory, please refer to the product reference manual.

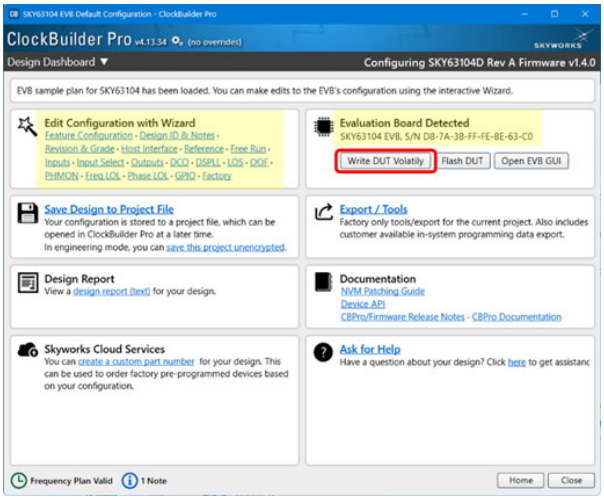

Figure 5. Write a Design to EVB in CBPro

4. EVB Overview

Figure 6 shows an overhead picture of the EVB highlighting the main areas the user may reconfigure to meet application needs. The EVB supports a socket for internal Skyworks use only.

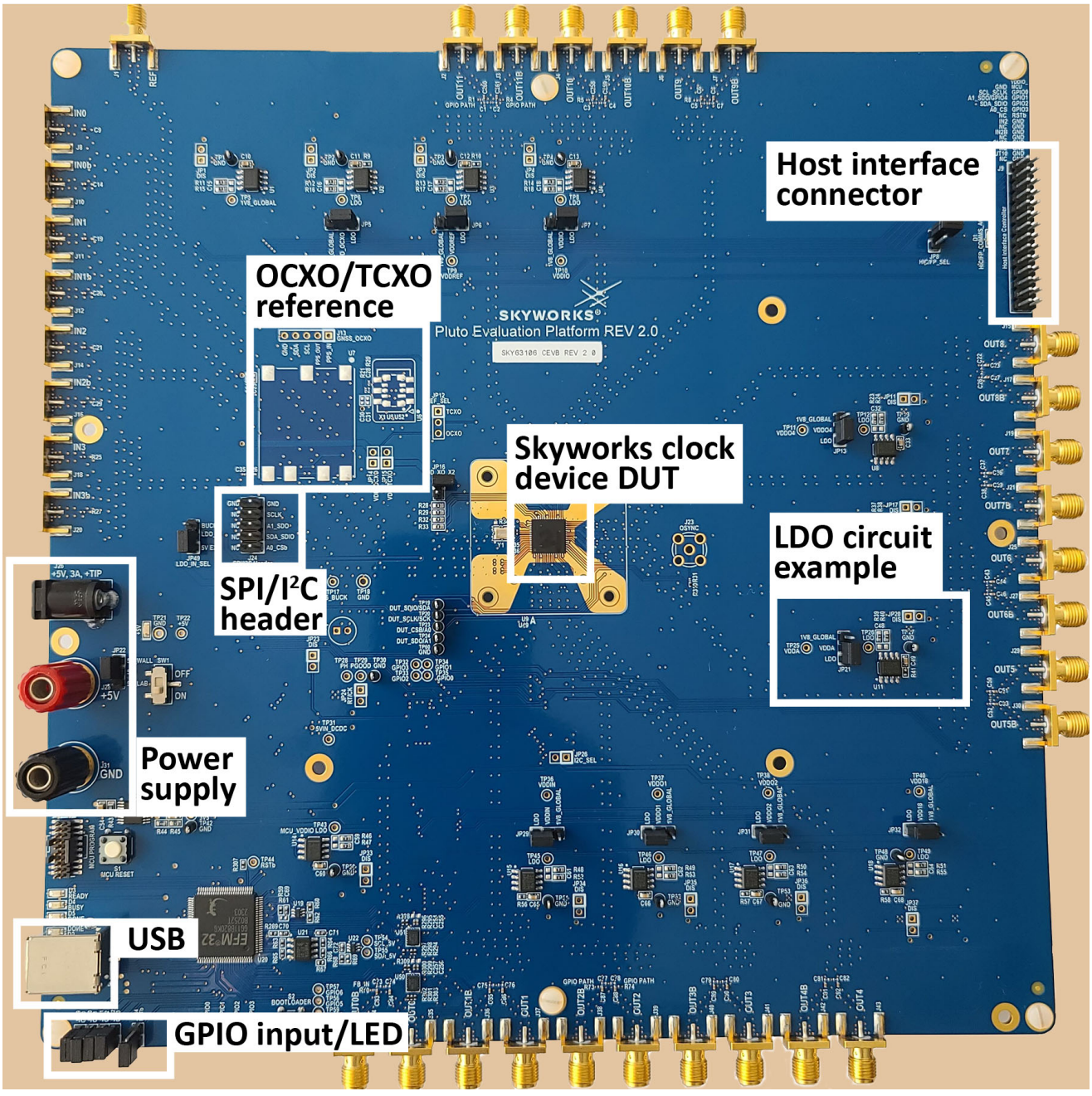

Figure 6. Evaluation Board Overview

5. Power Supply Topology

A block diagram of the evaluation board power supply tree is shown in Figure 7. It powers the DUT as well as the on-board oscillators and MCU. The flexible design allows the user to evaluate various power supply topologies, ranging from an all-LDO configuration (the default configuration) to an all-switching configuration or an external power supply. Multiplexing is performed on a per-VDD pin basis, allowing for further flexibility. Power the board using the +5 V dc adapter included in the kit.

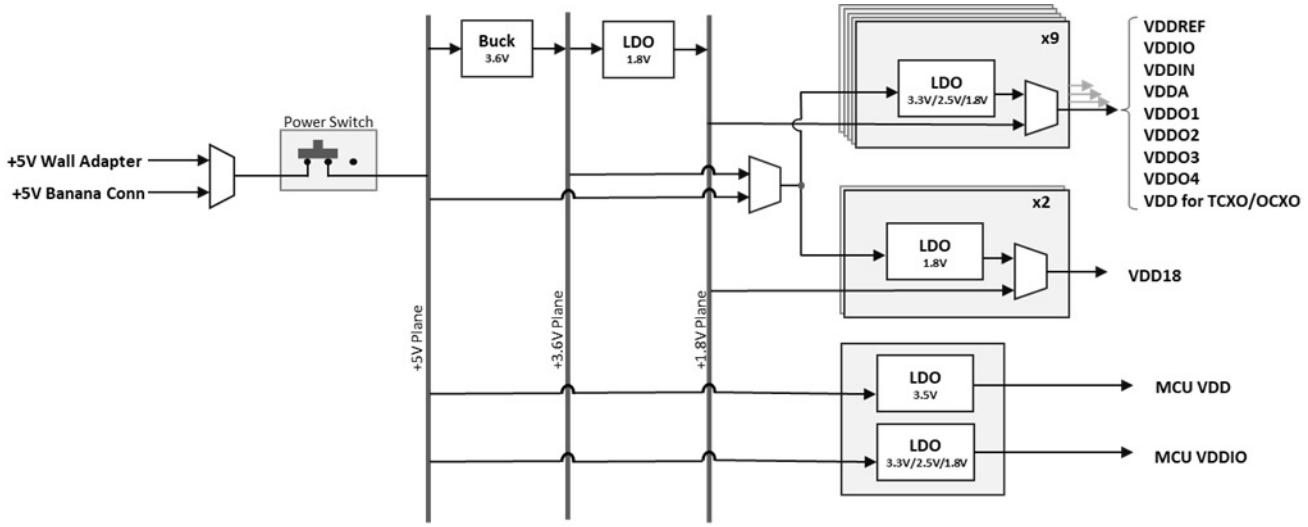

Figure 7. EVB Power Supply Tree

"5.1. Power Supply Jumper Settings" on page 7 discusses the jumper settings related to the power supplies. It should be emphasized that no modifications to the default jumper settings are needed in order to start using and testing the evaluation board. The jumper settings may only need to be changed when evaluating different power supply topologies, which comes later in the design process.

5.1. Power Supply Jumper Settings

5.1.1. Configuring the +5 V Supply Plane

A +5 V supply is required for the board to operate. The +5 V supply plane options and features are detailed below. Circled numbers indicate locations on the dc power supply shown in Figure 8.

1. J26 [①] connector for the +5 V dc adapter (included in the kit). This is the default method of powering the board
2. J28/J31 [②] banana connectors for an optional +5 V supply. By default, these connectors are not used, but they can be used as a substitute for J26.
3. JP22 [③] selects which +5 V source will be used:
   a. Installing a jumper shunt on JP22 pins 1-2 [5V_WALL:5V] selects the dc adapter by default, or
   b. Installing a jumper shunt on JP22 pins 2-3 [5V:5V_LAB] selects the banana connectors.
4. SW1 [④] power switch turns the +5 V power supply on or off.
5. D2 [⑤] LED indicates whether the +5 V plane is powered on.

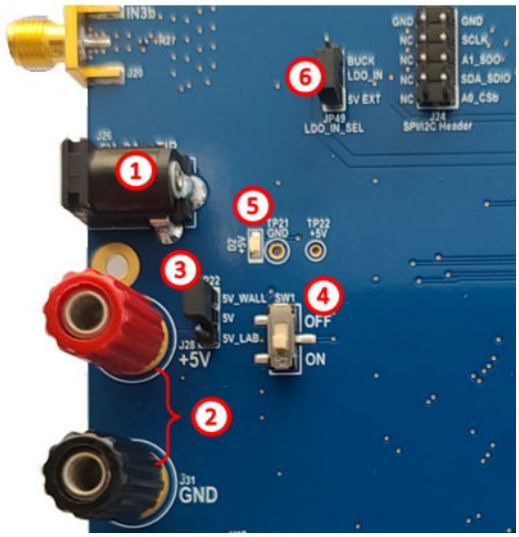

Figure 8. +5 V DC Power Supply

5.1.2. Configuring the DUT LDO Input Supply

The DUT power supply pins can be supplied by a 3.3 V, 2.5 V, or 1.8 V LDO, or a global 1.8 V plane. The applicable VDD pins are VDDO[1:4], VDDIN, VDDA, VDDIO, VDDREF, and VDD_OCXO. The LDO supply can be set from the 5 V supply or the 3.6 V buck switching regulator (Figure 8 [⑥]):

- Install a jumper shunt on J49 pins 2-3 for LDO input from 3.6 V buck switching regulator
- Install a jumper shunt on J49 pins 1-2 for LDO input from the 5 V plane

5.1.3. DUT VDD IN Selection

The DUT VDDOx, VDDIN, VDDA, VDDIO, VDDREF, and external reference VDD_OCXO power supply can be configured from the individual LDO or from a single global LDO. For each DUT VDD supply, the user can select the VDD supply source via jumper setting. Please note that VDDA must be the highest voltage among all DUT VDD supplies. Refer to Table 4 for the factory default settings and available options. Figure 9 shows an example of the DUT VDDO3/VDDO4 supply selected from each individual LDO.

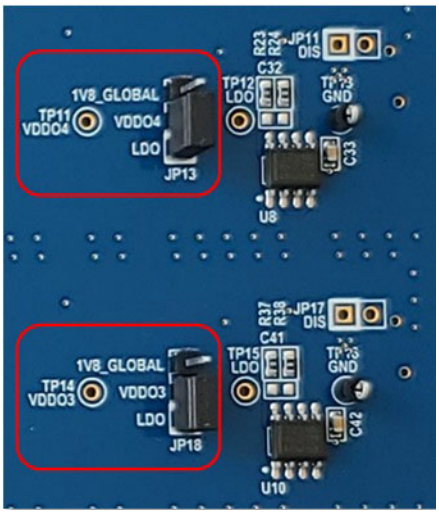

Figure 9. VDDO3/VDDO4 IN Selection

5.2. Power Supply Use Cases

The flexible power supply allows the user to evaluate various power supply topologies. Three typical use cases are presented below using the VDDO3 pin as an example.

1. **Use Case #1: LDO Only Configuration (Out-of-the-Box Default Setting)**

   Power the DUT using all LDOs supplied by the external 5 V power supply.

   ① JP49 header determines the source of the VDD pin. Installing a jumper shunt on J49 pins 1-2 selects the 5 V dc as a VDDO3 LDO input.

   ② Installing a jumper shunt on JP18 pins 1-2 switches the VDDO3 LDO output to DUT.

   ③ The VDDO3 LDO output voltage can be configured or disabled by the CBPro frequency plan.

   ④ TP14 test point for VDDO3 pin voltage.

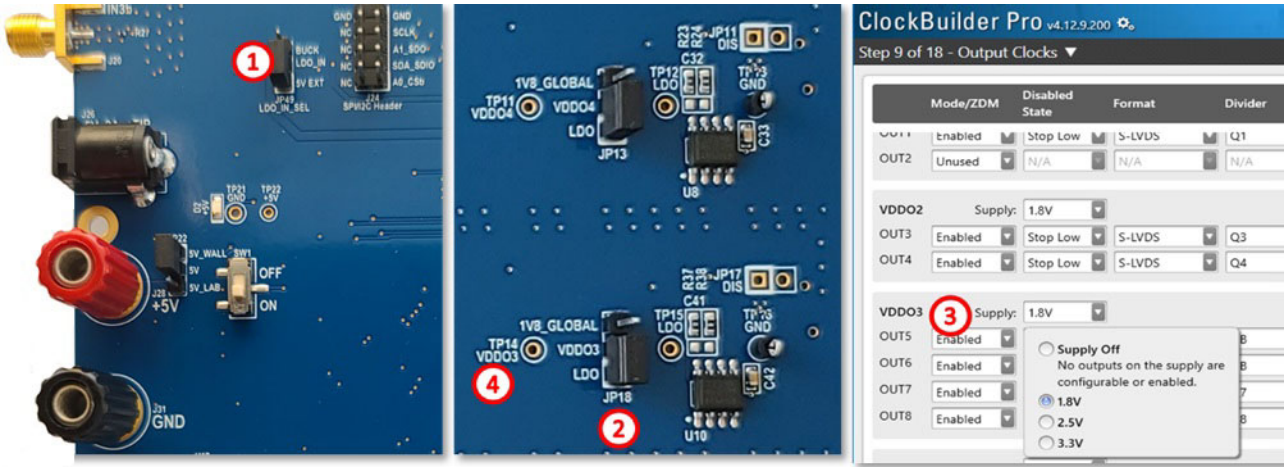

Figure 10. Power Supply Use Case #1 and LDO Configuration

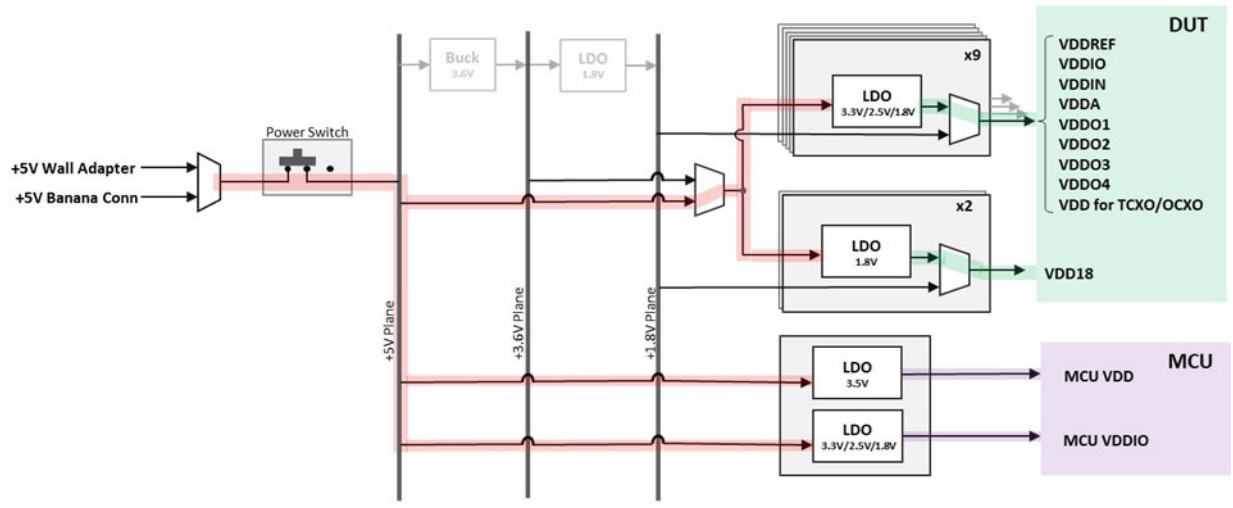

Figure 11. Power Supply Use Case 1 Diagram

2. Use Case #2: Mixed Buck Switching Regular and LDO Configuration

A buck converter is used to convert the 5 V input to 3.6 V, which is then used as the supply for each LDO. This reduces the LDO dropout voltage and the heat dissipation from the LDOs, therefore improving power supply efficiency.

① JP49 header determines the source of the VDD pin. Installing a jumper shunt on J49 pins 3-4 selects the BUCK as a VDDO3 LDO input.

② Installing a jumper shunt on JP18 pins 1-2 switches the VDDO3 LDO output to DUT.

③ The VDDO3 LDO output voltage can be configured or disabled by the CBPro frequency plan.

④ TP14 test point for VDDO3 pin voltage.

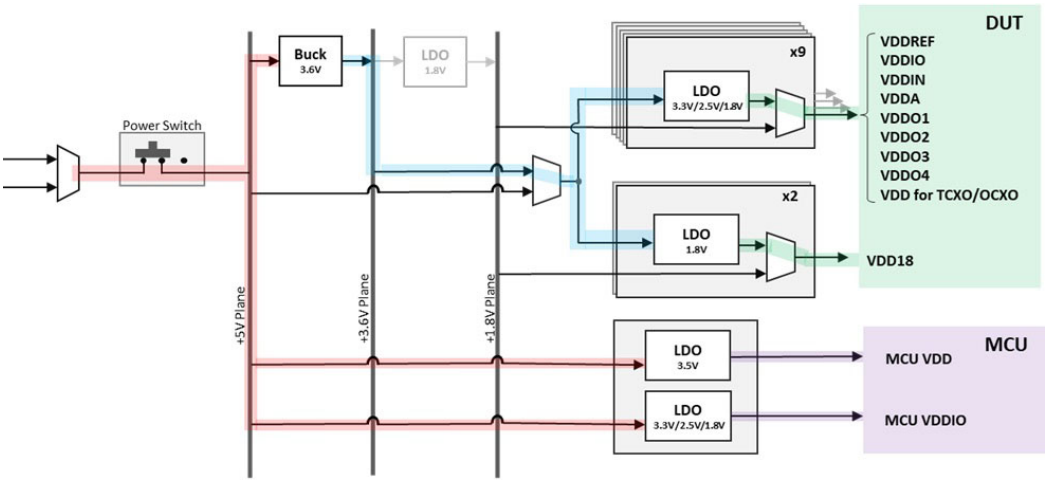

Figure 12. Power Supply Use Case 2 Diagram

3. Use Case #3: Single Global Power Supply

A buck converter is used to convert the 5 V input to 3.6 V then, using LDO, convert to global 1.8 V supply. This is the simplest power supply design as the entire clock device is powered by a single LDO.

① Installing a jumper shunt on JP49 pins 2-3 selects buck convert output.

② Installing a jumper shunt on JP18 pins 2-3 switches the 1.8 V global output to DUT VDDO3. See Figure 13.

③ Installing the jumper shunts for all other DUT VDDs switches them to 1.8 V global.

Figure 13. Supply Use Case – Global 1.8 V Supply

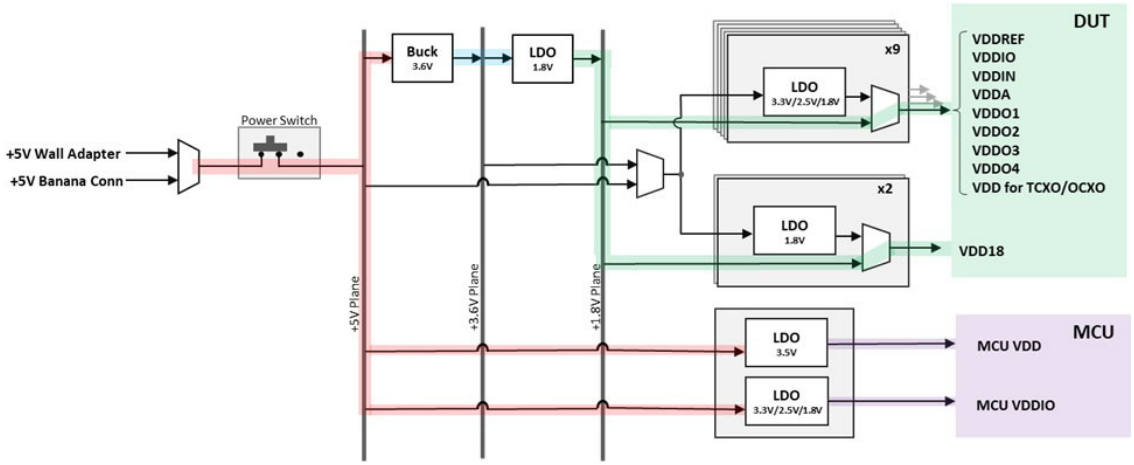

Figure 14. Power Supply Use Case 3 Diagram [③]

6. References

6.1. Configuring the XTAL/XO Reference Clock

The SKY63104, SKY63105, SKY63106, SKY62101, SKY69102, SKY69003, and SKY63001 require a low-noise reference clock. This can either be a crystal (XTAL) or a crystal oscillator (XO). The recommended XTAL/XO reference can be found in the Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual.

The evaluation board can be configured to support either an on-board XTAL/XO or an external reference clock.

For different DUT ordering options there are different XTAL and XO and OCXO included in the BOM. Please refer to "12. Ordering Information" on page 31.

- To configure the XTAL as reference, power down the XO by removing the jumper shunt on JP16 to avoid interference.
- To configure the on-board XO as reference, install a jumper shunt on JP16.
- External reference can be also supported by connecting the reference to the REF SMA connector and removing the on-board XO reference by removing R130 and populating R127/R129 with zero-ohm resistors. Only single-ended signal formats are supported for XO reference.
- Make sure the reference XO_IN signal swing matches the VDDREF. Modify the R127/R128/R129/R130 value to divide the voltage down if required.

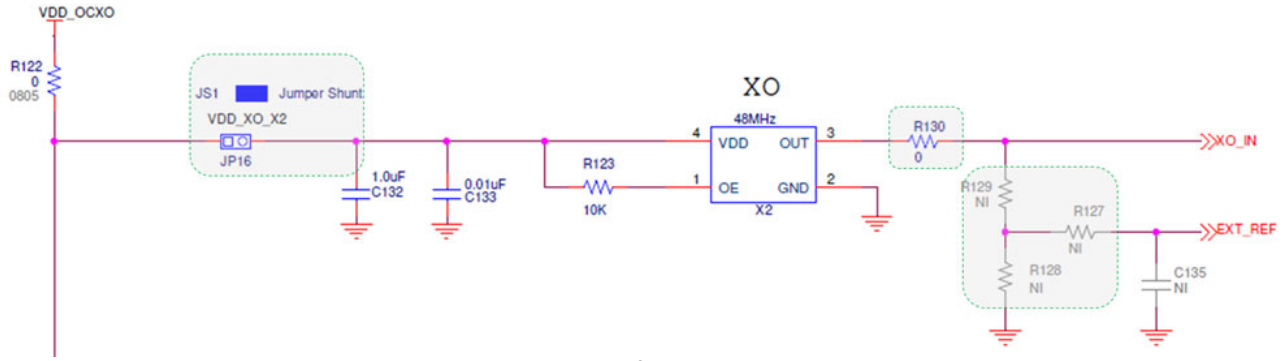

Figure 15. XO Reference Schematic

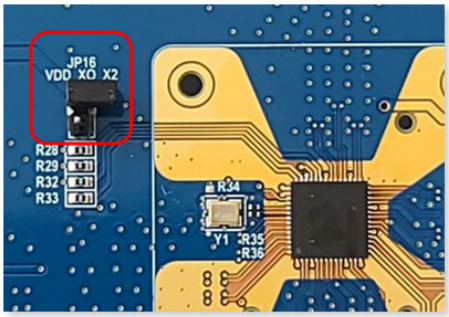

Figure 16. VDD for Reference XO

6.2. Configuring OCXO/TCXO References

SKY69102 and SKY69003 are used in network synchronization applications such as Synchronous Ethernet and IEEE 1588 PTP, and require a stable local oscillator such as an OCXO/TCXO in addition to the XO/XTAL reference for free-run and holdover mode. There are STP3608LF 38.88 MHz OCXO on SKY69102 EVB and U7958LF 48 MHz OCXO on SKY69003 EVB. There are PCB footprint reserved for testing with different OCXO/TCXO than the on-board default. The recommended OCXO/TCXO can be found in the Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual.

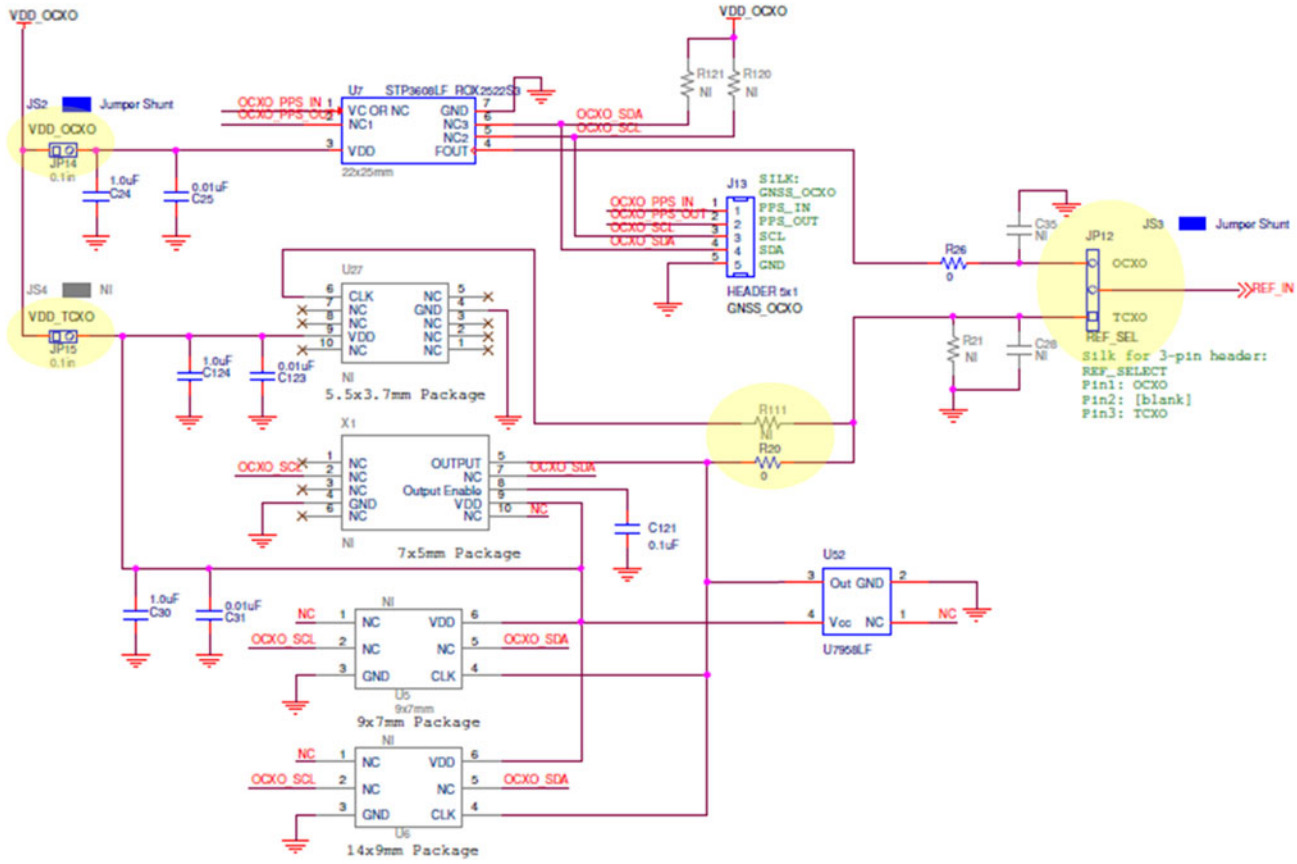

Figure 17. Schematic for External OCXO/TCXO Reference

The oscillator footprints supported on this evaluation board are:

- 22 x 25 mm (U7)
- 14 x 9 mm (U6)
- 9 x 7 mm (U5)
- 9.7 x 7.5 mm (U52)
- 7 x 5 mm (X1)
- 5.5 x 3.7 mm (U27) – U27 can be found on the back side of the PCB.

6.2.1. Using the Onboard OCXO

The SKY69102 evaluation board is populated with a 22 x 25 mm, 38.88 MHz OCXO (U27). The SKY69003 evaluation board is populated with a 9.7 x 7.5 mm, 48 MHz OCXO (U52). To use the oscillator:

- Install a jumper on JP14 for the U27 OCXO power supply
- Install a jumper on JP15 for theU52 OCXO power supply
- Install a jumper on JP12 pins 2-3 to select U27 OCXO to REF_IN or JP12 pins 1-2 to select U52 OCXO to REF_IN
- The default populated oscillator requires VDD_OCXO to be set to 3.3 V
- Populating C35/R21 with a resistor and modifying the R26/R29 value to divide the OCXO output voltage is required.

6.2.2. Using the 14 x 9, 9 x 7, 7 x 5, and 5.5 x 3.7 mm Oscillators

These oscillators are not populated on the EVB by default. A different oscillator can be populated on U27, X1, U5, and U6, but X1, U5, U6, and U52 share the PCB footprint and only one oscillator may be populated at a time. To use this oscillator:

- Remove the jumper from JP14 to power off the default on-board OCXO.
- Install the jumper on JP15 to power on the user-selected oscillators.
- Install the jumper on JP12 pins 1-2 to set the user oscillator to REF_IN
- Populate the zero-ohm resistor on R111 for U27 or R20 for X1/U5/U6, but not both resistors. Populate R21 if needed to divide down the oscillator output voltage.

7. Clock I/O

The evaluation board clock I/O is designed to support flexible functions while requiring minimal or no board rework.

7.1. Standard Clock Inputs [IN0-IN3]

IN0-IN3 supports differential or LVCMOS clock inputs. By default, IN0-IN2 are ac-coupled for differential input and terminated with 100 ohm. IN3/IN3b are dc-coupled for LVCMOS input. They can be reworked to support differential input. IN2/IN3 allow both legs of the input to be utilized as independent LVCMOS clocks, whereas IN0-IN2 allows only the positive leg to be used as an independent LVCMOS clock.

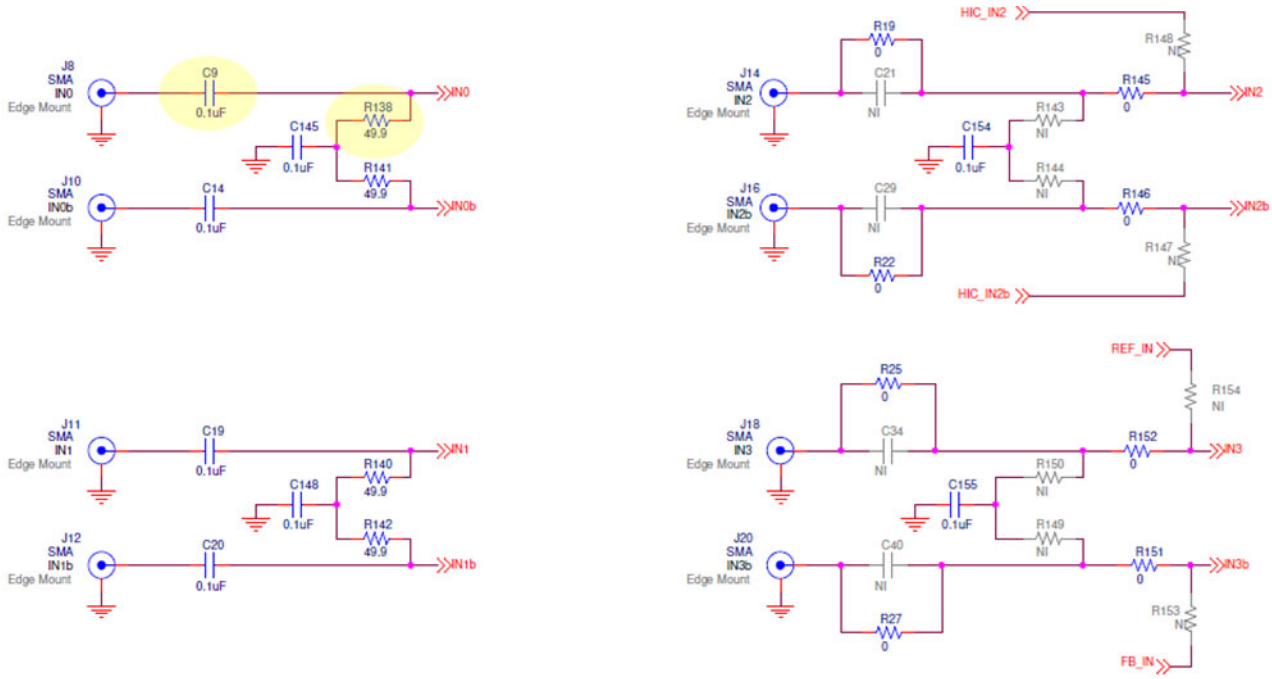

Figure 18. EVB Input Schematic

Follow the steps below to reconfigure IN0 for dc-coupled LVCMOS. IN1-IN3 is similarly reconfigured.

1. Remove R138.
2. Install a zero-ohm resistor in C9.

7.2. Clock Inputs from the Host Connector [IN2]

IN2/IN2B can be connected to either the SMA connector or the host interface connector. The default mode of operation is to use the SMA connectors. The host interface connector may be used when evaluating the SKY69102/SKY69003 with a third party CPU EVB for AccuTime™ evaluation.

- SMA connector: populate R145/R146, remove R147/R147 (EVB default)
- Host interface connector: remove R145/R146, populate R147/R148

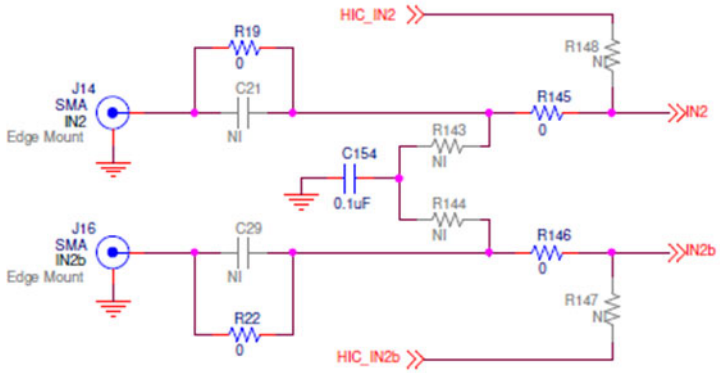

Figure 19. IN2/IN2b SMA/HIC Connection

7.3. Clock Input from OCXO/TCXO

When using the SKY69102/SKY69003 EVB for evaluation, IN3 is connected to the OCXO/TCXO as a single-ended LVCMOS input. The CBPro clock plan for SKY69102 has dedicated input naming for the on-board OCXO that physically takes the IN3 port. IN3b is renamed as IN3. As all DUT variants share the same EVB, the silk screen text for SKY69102 EVB IN3/IN3b can be ignored.

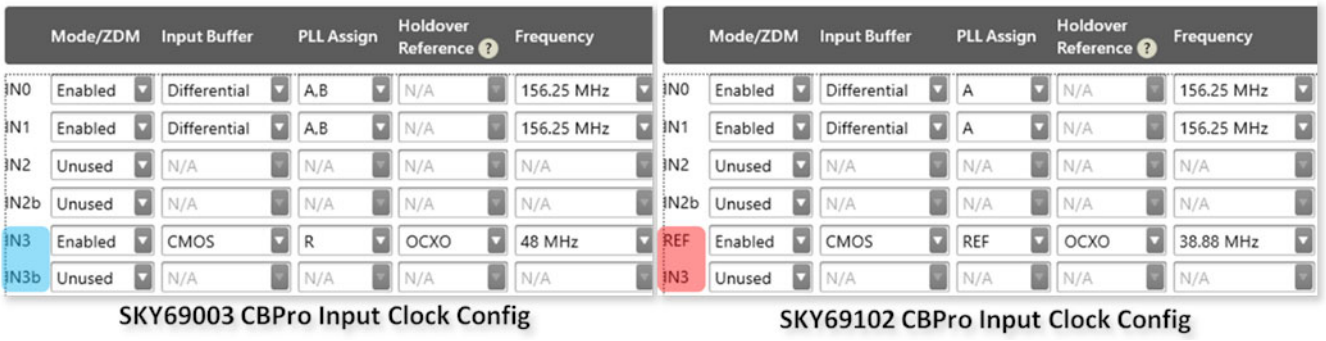

Table 1. IN3 Cross Reference

IN3 naming in CBPro	EVB IN3	EVB IN3b
SKY62101 EVB	IN3	IN3b
SKY63104 EVB	IN3	IN3b
SKY63105 EVB	IN3	IN3b
SKY63106 EVB	IN3	IN3b
SKY69003 EVB[1]	IN3 On-Board OCXO	IN3b
SKY69102 EVB	REF On-Board OCXO	IN3

1. SKY69003BA-EVB can be used to evaluate SKY69003 and SKY63001 clock devices.

7.4. Clock Outputs [OUT0-OUT11]

OUT0-OUT11 can support both ac-coupled and dc-coupled clock outputs. OUT10 and OUT11 are dc-coupled by EVB default.

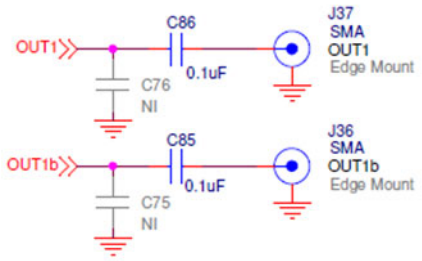

Figure 20. Output Schematic

OUT1 can be configured according to the instructions below. Other outputs are configured similarly.

- AC-coupled differential
  - Populate C85/C86 with 0.1 µF
- DC-coupled
  - Populate C85/C86 with a zero-ohm resistor
- PCIe output
  - Populate C75/C76 with a 2 pF load
  - Populate C85/C86 with zero-ohm resistors for PCIe jitter evaluation or 950 ohm resistors for PCIe SI valuation

7.5. Clock Outputs from Host Connector [OUT9-OUT10]

OUT9 and OUT10 can be connected to either the SMA connector or the host interface connector. The default mode of operation uses the SMA connectors. The host interface connector may be used when evaluating the SKY69102/SKY69003 with a third-party CPU EVB for AccuTime evaluation.

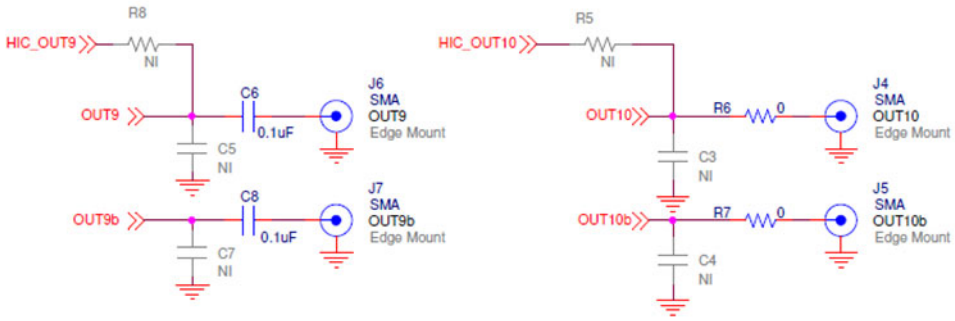

Figure 21. OUT9/10 to Host Interface

Follow the steps below to configure OUT9. OUT10 is configured similarly.

1. SMA connector: Populate C6 (EVB default)
2. Host interface connector: Populate zero-ohm in R8, remove C6

7.6. Clock Outputs Configured as GPIO

OUT2/OUT2B and/or OUT11/OUT11B can be configured as GPIO ports.

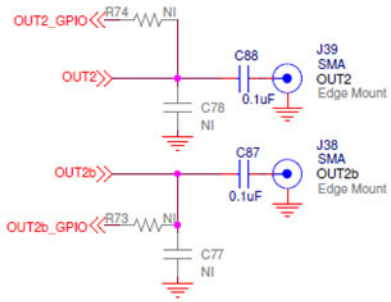

Figure 22. OUTPUTs Configured as GPIO

Populate R73/R74 with zero-ohm resistors to route the output signal to MCU. The user may set or read the state of the GPIO port from the CBPro EVB GUI. OUT11 is configured similarly. The VDDO1 (for Out2/2b) and VDDO4 (for Out11/11b) need to be set to the same voltage as VDDIO.

8. Serial Communication and Bus Switch

The EVB DUT can be controlled by variety of sources:

- Default mode: Controlled by ClockBuilder Pro via on-board MCU
- AccuTime mode: Controlled by host interface connector
- Field programmer mode

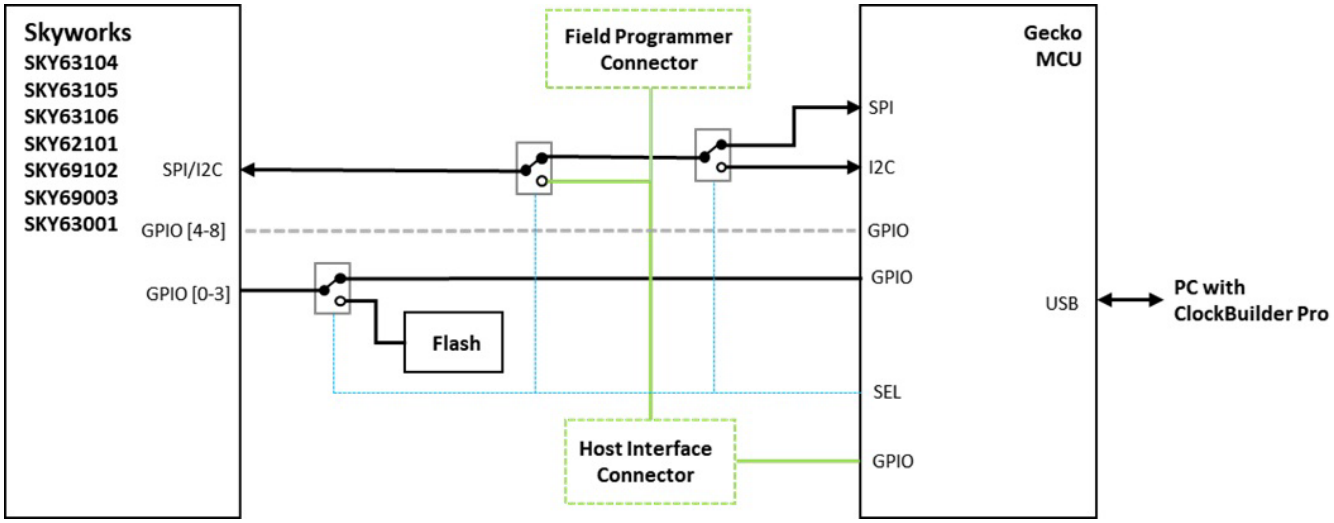

Figure 23. DUT Serial Communication and GPIO

8.1. Default Mode: Controlled by ClockBuilder Pro via MCU

The default mode of operation is to have ClockBuilder Pro control the DUT using the on-board MCU and USB cable. Generally, this is the recommended mode because ClockBuilder Pro can control all components on the board such as the DUT, regulators, LEDs, and sensors. In this mode, the host interface connector and field programming connector are not used.

There must be agreement between the serial port master and DUT as to what voltage level to use to communicate. When using ClockBuilder Pro (default mode) with the EVB, there's a level converter between the DUT and MCU that is automatically set appropriately by the MCU.

8.2. AccuTime Mode: Controlled by Host Interface Connector

When evaluating SKY69102/SKY69003 in conjunction with AccuTime, a third-party CPU evaluation board is required to run the AccuTime software and communicate with the SKY69102/SKY69003-EB. In this case, the third-party CPU will need to take control of the DUT instead of the MCU/CBPro.

To configure the SKY69102/SKY69003-EB for AccuTime mode:

- Install jumper JP8. Confirm that LED D1 is turned on
  - This routes the DUT serial port as well as GPIO0-GPIO3 toward the host interface connector (J9), according to the block diagram
- If the third-party CPU needs access to the DUT clock I/O, follow the instructions in "7.2. Clock Inputs from the Host Connector [IN2]" on page 14 and "7.5. Clock Outputs from Host Connector [OUT9-OUT10]" on page 16 to route IN2/IN2B/OUT9/OUT10 to the host interface connector.

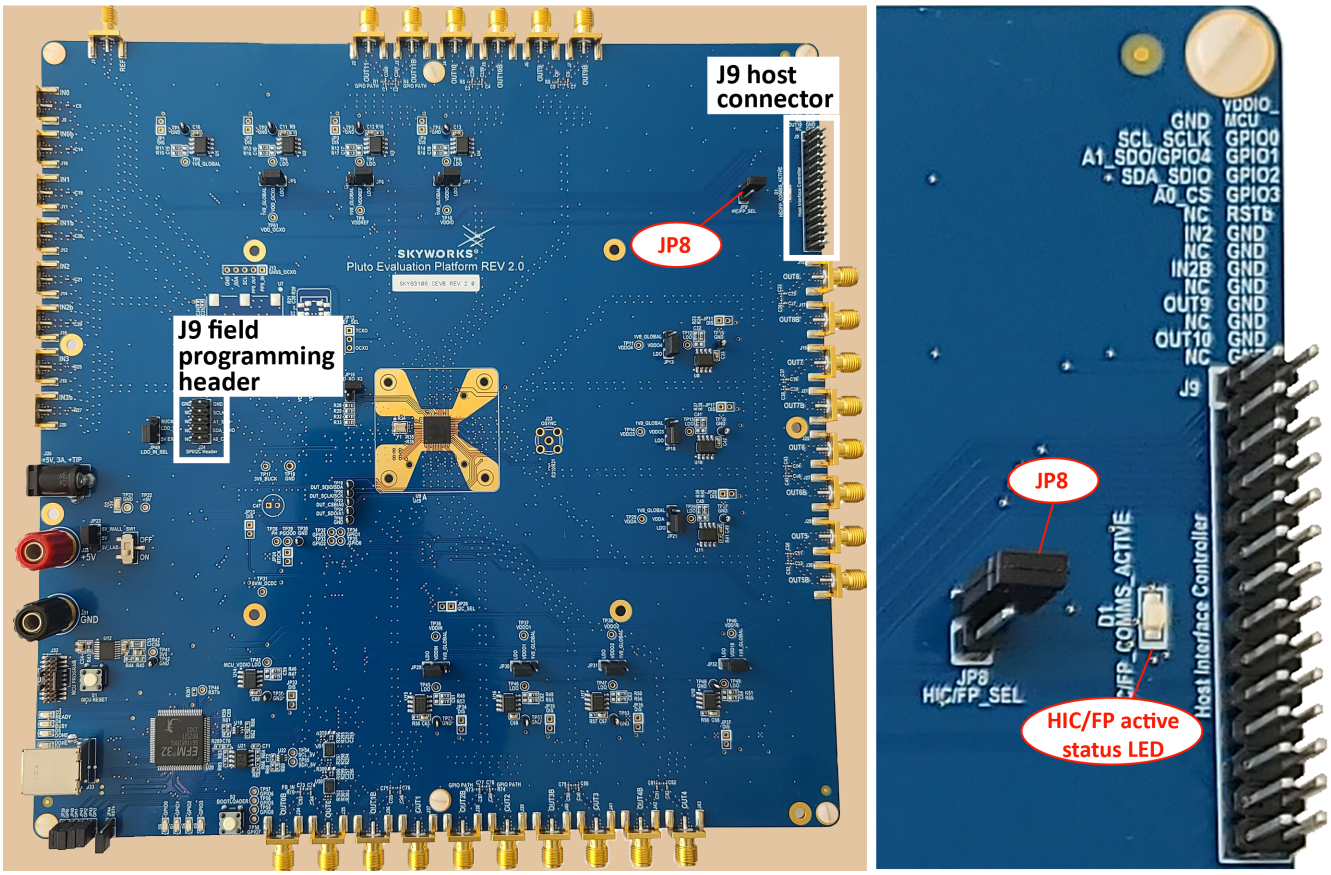

Figure 24. Host Interface and Field Programmer Connector Selection

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Note: *Although the host interface connector gives control of the DUT to a third-party CPU, the voltage regulators still need to be set to the desired levels. This is typically done by connecting the Pluto EVB to the CBPro EVB GUI via a USB cable and setting the voltage regulator levels in the GUI. Please set the VDDIO voltage to match the host interface serial I/O voltage levels.*

8.3. Field Programmer Mode

The ClockBuilder Pro field programmer is typically used to debug devices already in the field. It is typically not useful when used with the EVB because it has an existing way of interfacing with CBPro using the on-board MCU and USB cable. However, connecting the field programmer to the EVB can be useful when learning how to use the field programmer. The field programmer can be connected to the EVB by connecting the field programmer through the J24 10-pin connector connected to the serial communication port of the DUT. A jumper shunt on JP8 (see Figure 24) needs to be installed to switch the DUT serial comm port connection from MCU to J24.

Note: *Although the field programmer takes control of the DUT, the voltage regulators still need to be set by the user to the desired levels. This is typically accomplished by connecting the EVB to the CBPro EVB GUI via a USB cable and setting the voltage regulator levels in the GUI. Please match the field programmer I/O voltage setting to the VDDIO setting on the CEVB.*

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9. EVB Peripherals

9.1. OUT Reset Pin

The DUT reset (RSTb) pin can be asserted by any of the following actions:

- Installing a jumper on JP44
- Using the CBPro EVB GUI
- Device API reset command from an external CPU connected to the host interface connector

Asserting the pin holds the DUT in reset until the pin is de-asserted. See the data sheet for further information. This reset pin has no effect on other components on the board.

9.2. DUT GPIO

The SKY63104, SKY63105, SKY63106, SKY62101, SKY69102, and SKY69003 have 10 GPIO status/control pins, each of which have programmable functions and polarities. GPIO0-GPIO3 are dedicated GPIO ports, GPIO4-GPIO9 are shared with A0/A1/outputs and they can be configured as GPIO ports or for other functions. Common status functions include loss-of-lock (LOL) or interrupt (INTR) common control functions, including output enable (OE) or input select (IN_SEL).

For GPIO0-3 configured as status, the LED D6-D9 turns on when the status pin asserts. The corresponding control header has no effect. The behavior applies when the GPIO is configured as active-high or active-low.

For GPIO pins which are configured as control, installing a jumper on the header pin (JP39-JP42) asserts the pin. The corresponding LED turns on. The behavior applies when the GPIO is configured as active-high or active-low.

Additionally, GPIO pins can be read and set from the CBPro EVB GUI software without utilizing the control header pins and status LEDs. The CBPro EVB GUI dominates the control input when both GUI software and control headers are in play.

9.3. GPIO Control Headers and Status LEDs

Table 2. GPIO Control Header and Status LED

GPIO	Control Header (Silk/Reference Designator)	Status LED (Silk/Reference Designator)
GPIO0	GPI0 / JP39	GPIO0 / D6
GPIO1	GPI1 / JP40	GPIO1 / D7
GPIO2	GPI2 / JP41	GPIO2 / D8
GPIO3	GPI3 / JP42	GPIO3 / D9
GPIO / A0_CSb[1]	N/A	N/A
GPIO / A1_SDO[1]	N/A	N/A
GPIO5 / OUT2b[2]	N/A	N/A
GPIO6 / OUT2[2]	N/A	N/A
GPIO7 / OUT11b[2]	N/A	N/A
GPIO8 / OUT11[2]	N/A	N/A

1. Not available for the EVB since the DUT Serial Communication interface is SPI-4 by default.
2. In order to read or control the OUTx/GPIO signals through the EVB GUI, on-board resistor modifications are necessary. See "7.6. Clock Outputs Configured as GPIO" on page 16 for more details.

9.4. Board Status LEDs

Table 3. Board Status LEDs

LED	LED ON Indication	On During Normal Operation
D2	Power applied to +5 V plane	Yes
D3	MCU ready	Blink every 1 second
D4	MCU busy	Yes
D5	MCU done	Yes

9.5. External Flash Memory

By default, the DUT comes with a blank part without firmware or a user application plan. The user can design and write a plan to the DUT RAM for evaluation testing. All the data in RAM is volatile after a power cycle. The user can also burn a plan to the DUT NVM, however there are limited burn counts with NVM. The external flash supports unlimited burn times. Since the flash uses the GPIO0-GPIO3 as a serial data bus to the DUT, the GPIO0-GPIO3 cannot be used as a general GPIO function when the external flash is enabled.

9.5.1. Using the External Flash

There is an on-board 2 Mb flash memory for the DUT firmware/clock plan. To enable the external flash, the flash driver needs to be burned to the NVM before using the external flash. The EVB DUT does not support external flash by default, and the user can patch the DUT to support external flash or disable flash support through the ClockBuilder EVB GUI (Figure 25). There are limited entries to patches to the NVM. The user may need to populate a zero-ohm resistor on R304 to power up the flash (Figure 26).

Please note that, once the external flash driver is patched in the NVM, the user may not be able to burn a customer plan to the NVM. This is not a common use case.

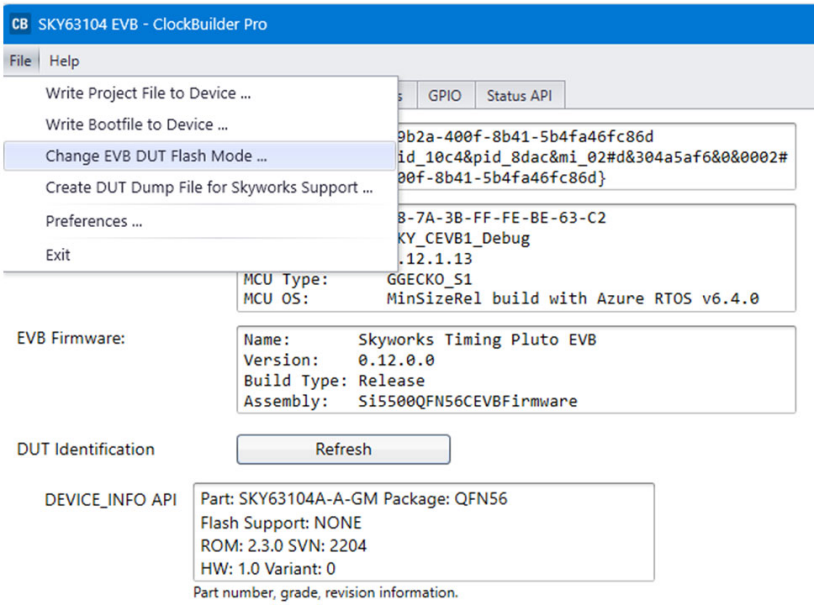

Figure 25. Converting DUT to Enable/Disable External Flash Support

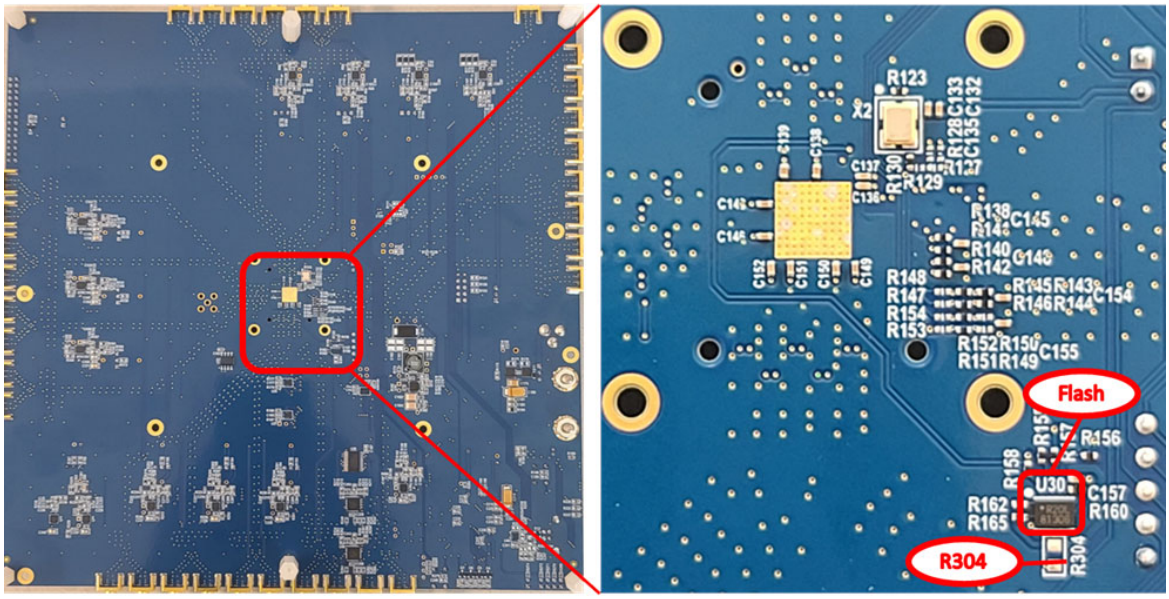

Figure 26. R304 Location on the Back Side of the EVB

There is a DUT GPIO switch in the EVB GUI; when GPIO_SEL is set to high, the GPIO0-GPIO3 are assigned as SPI bus to the external flash. The GPIOs cannot be assigned for another function.

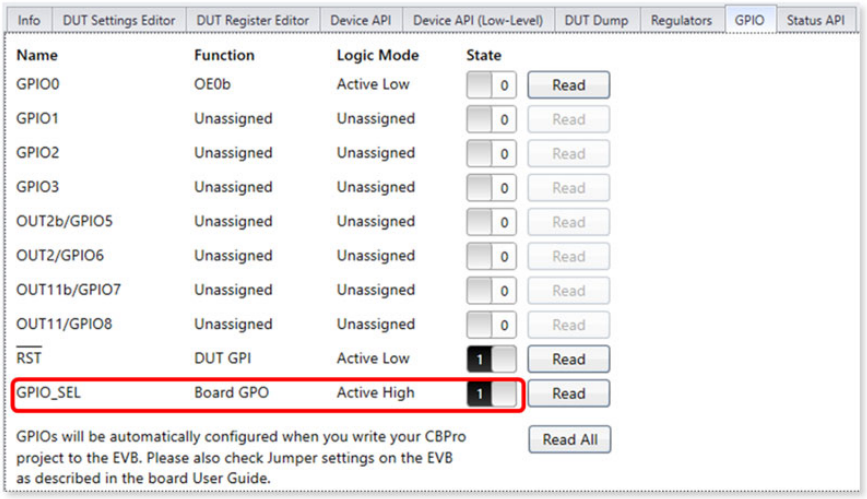

Figure 27. Enable External Flash Via the EVB GUI

After the flash is enabled, the flash info appears in the EVB GUI:

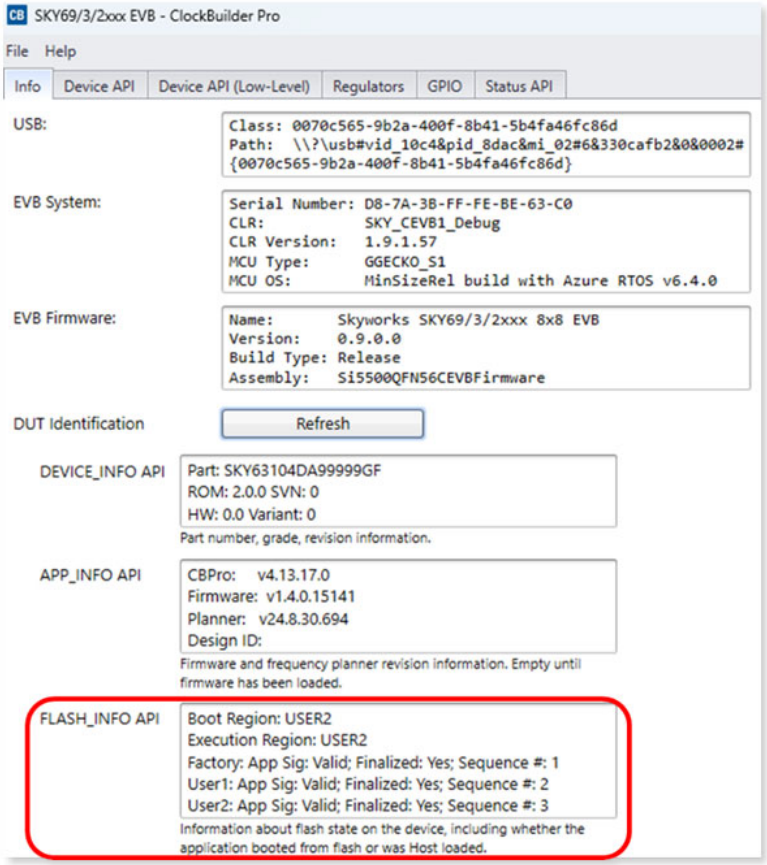

Figure 28. EVG GUI Flash Info

The EVB still supports host loading the application/frequency plan to the DUT RAM for evaluation testing after the external flash support is enabled. The user has an option to write a clock plan to the DUT RAM or write the clock plan to external flash.

Please note that the VDDx were configured by the EVB GUI when writing a plan. When booting the DUT directly from the external flash, the user may need to manually set the VDDx in the EVB GUI regulator page.

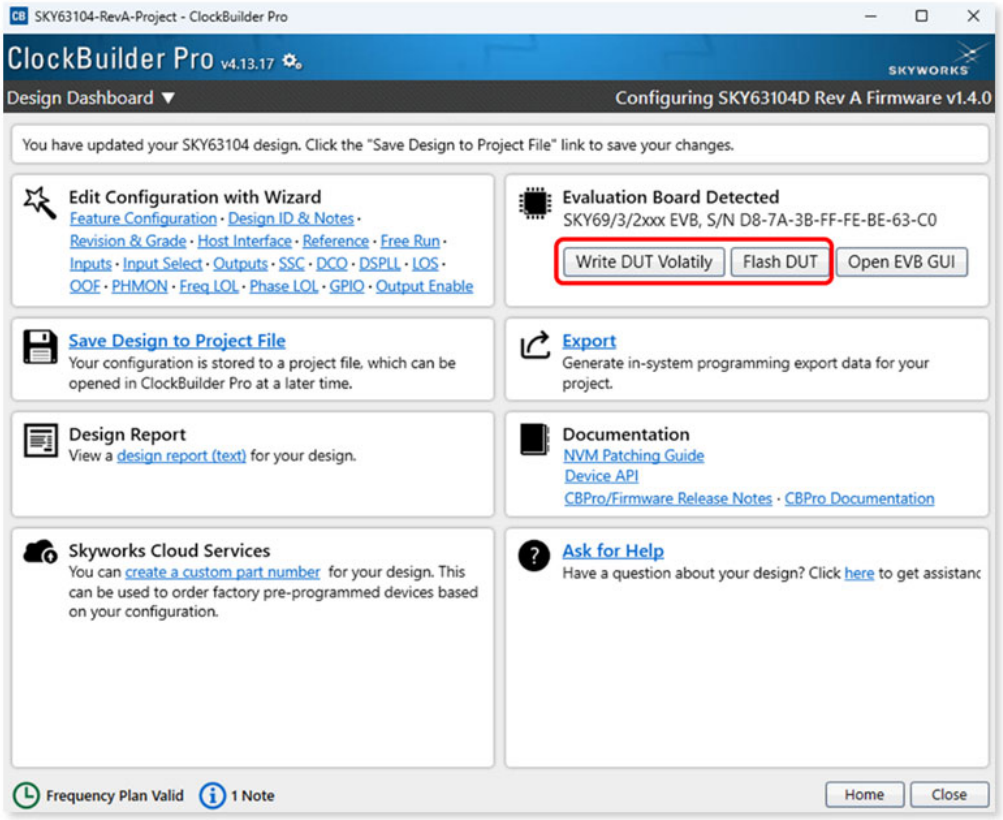

Figure 29. Writing a Clock Plan to DUT RAM or External Flash

10. Best Practices for Taking Measurements

The following sections outline a few basic techniques that are useful when taking measurements on the DUT with the EVB.

10.1. Phase Noise Measurements and Baluns

For the differential clock output measurement, a balun is required to convert the output signal into a single-ended clock since the phase noise analyzer input port is typically single-ended. A balun is included with the EVB kits. Differential clocks should be connected to a balun using phase-matched cables.

While it is possible to connect one leg of a differential clock to the phase noise analyzer eliminating the need for a balun, it is generally not recommended to do so because the measurement of interest is the differential phase noise of the clock, not the single-ended phase noise.

Single-ended LVCMOS clocks can be connected to the phase noise analyzer without a balun. Typically, ac-coupling is required, but that may depend on the model of the phase noise analyzer being used.

10.2. Termination of Outputs

All used outputs must be terminated appropriately, even if they are not being analyzed. If differential outputs are not properly terminated, there are unwanted reflections between the load and source. This generally causes crosstalk to be more severe in phase noise measurements. For details on the recommended termination for a given output format, see the product reference manual. For the most common differential output formats, which are LVDS and LVPECL, a 50 ohm SMA terminator should be placed on both legs of the output, with ac-coupling enabled. LVCMOS outputs should be left unterminated because they are intended to drive high impedance loads.

When taking measurements on one leg of a differential clock (e.g., oscilloscope measurements), it is important to terminate the other leg properly. Because both legs of the output driver operate as a differential pair, one unterminated leg may lead to distortion in both legs of the clock signal. For the most common differential output formats (LVDS and LVPECL), one leg can be ac-coupled to the instrument, and the other leg can be ac-coupled to a 50 ohm SMA terminator.

LVCMOS outputs require an external source resistance to match the total source resistance to the trace impedance. See the DUT reference manual for more information on the recommended CMOS termination. Replace the output ac-coupling capacitor with a resistor if required.

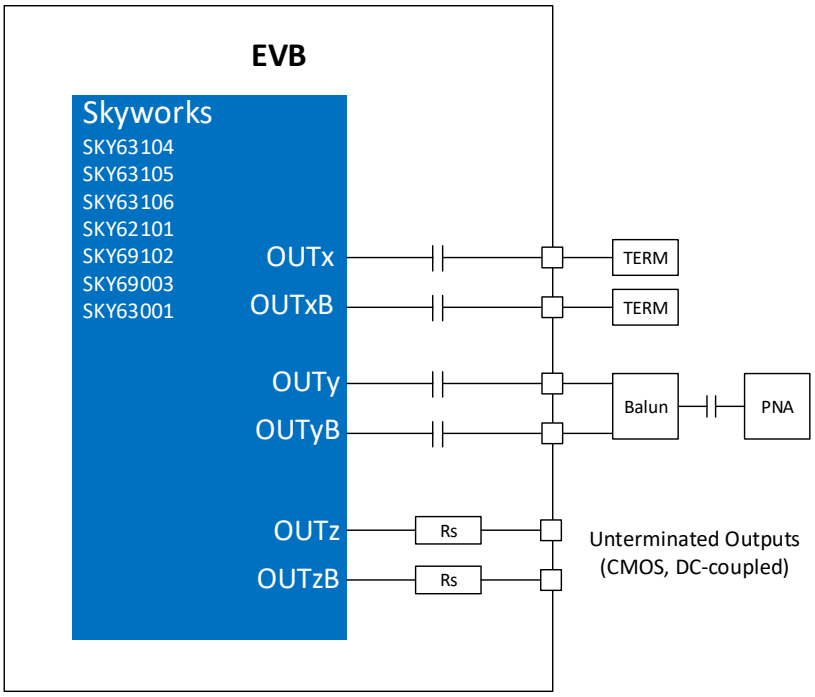

Figure 30. Output Termination

10.3. Zero Delay Mode

Zero Delay Mode (ZDM) externalizes the feedback path of the DSPLL to bring the I/O delay of the DSPLL to nominally zero with a very tight tolerance.

Typically, the ZDM external feedback path is implemented using a very short trace from the chip OUT0b to chip IN3b by populating R170/R153 with zero-ohm resistors on the EVB.

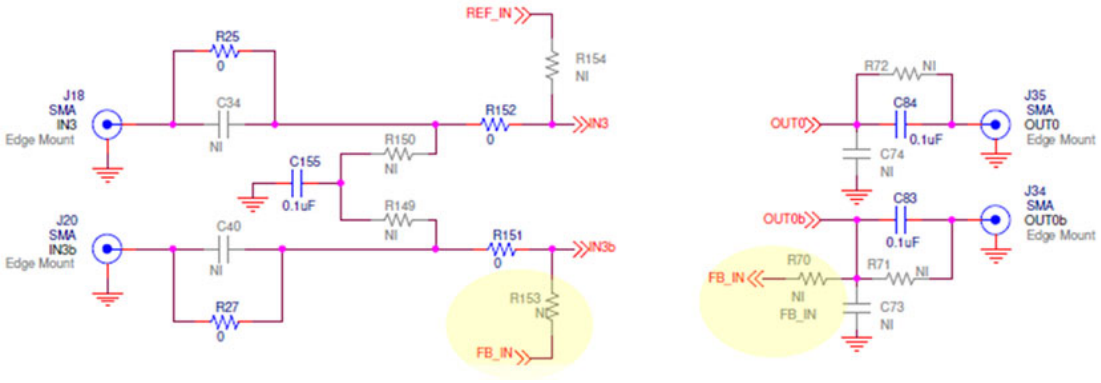

Figure 31. On-board Zero Delay Mode

Another solution is to use an SMA cable from the output SMA routed back to the input SMA. To do this, two pairs of phase-matched cables can be used (shown in green and orange in Figure 32). The PLL is trying to match the phase of INx and IN_ZDM by adjusting the edge of OUT_ZDM. If the feedback path has the same propagation delay as the path to INx from the clock generator, the OUT_ZDM edge (and therefore the OUTx edge) should be completely in phase with the clock edge at the clock generator output, assuming both outputs from the clock generator are in phase to begin with. If the remaining cable pair is also phase-matched, then the edge difference between the two clocks seen on the oscilloscope should ideally be 0, but realistically reflects the ZDM performance of the DUT. All clock pair traces on the EVB are phase-matched.

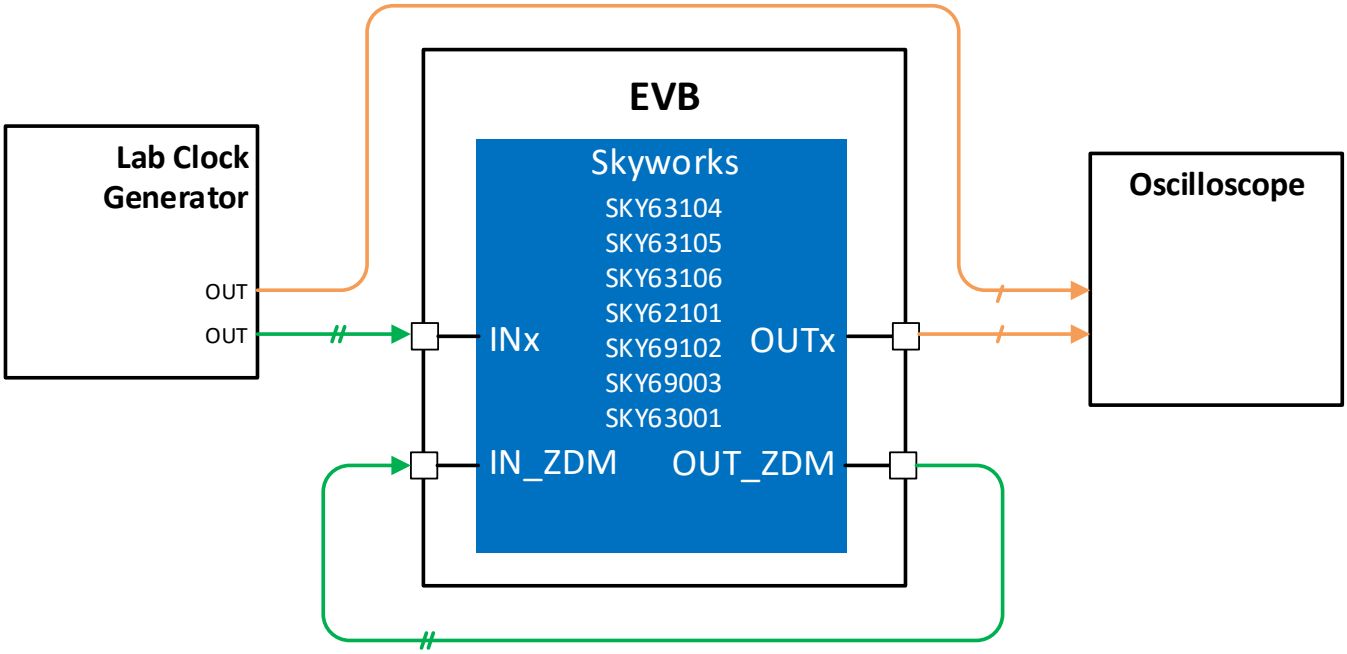

Figure 32. Measurement for DUT ZDM performance

10.4. Output Clock Skew Measurement

The measuring phase between clock outputs may be important in some applications. Frequency counters may be used if they have time interval measurement capability. However, the oscilloscope is the preferred instrument because the entire clock waveform can be seen. In both cases, the zero-crossing voltage should be equal to the midpoint of the clock waveform period. For ac-coupled clocks, this is 0 V. Phase-matched cables should be used, and oscilloscope channel-to-channel skew should be calibrated out prior to taking the measurement in order to minimize errors due to instrumentation. Sufficient oscilloscope bandwidth is also critical to getting an accurate skew measurement on high-speed clock edges.

11. Appendix

11.1. Factory Default Jumper Settings

The following factory default jumper settings match those described in "2. Quick Start Guide" on page 3. They configure the board so the DUT is:

- Controlled by ClockBuilder Pro via MCU (see "8.1. Default Mode: Controlled by ClockBuilder Pro via MCU" on page 17).
- Powered by the LDO-only power supply configuration using the 5 V dc adapter (see "5.2. Power Supply Use Cases" on page 9).

Table 4. Default Jumper Settings

Location	Type	Description of Signal[1]	Jumper Shunt[2]
JP5	3-pin	VDD_OCXO selection: 1.8 V global / **LDO**	1-2
JP6	3-pin	VDDREF selection: 1.8 V global / **LDO**	1-2
JP7	3-pin	VDDIO selection: 1.8 V global / **LDO**	1-2
JP8	2-pin	Host interface/field programmer selection - **Disabled**	O
JP12	3-pin	OCXO REF Selection OCXO/TCXO	By user clock plan
JP13	3-pin	VDDO4 selection: 1.8 V global / **LDO**	1-2
JP14/JP15	2-pin	OCXO/TCXO power	By user clock plan
JP16	2-pin	Reference XO power supply - **Disconnected**	O
JP18	3-pin	VDDO3 selection: 1.8 V global / **LDO**	1-2
JP19	2-pin	Field Programming - **Disabled**	O
JP21	3-pin	VDDA selection: 1.8 V global / **LDO**	1-2
JP22	3-pin	5V supply: Lab / **5V dc Adapter**	1-2
JP29	3-pin	VDDIN selection: 1.8 V global / **LDO**	1-2
JP30	3-pin	VDDO1 selection: 1.8 V global / **LDO**	1-2
JP31	3-pin	VDDO2 selection: 1.8 V global / **LDO**	1-2
JP32	3-pin	VDDO3 selection: 1.8 V global / **LDO**	1-2
JP44	2-pin	Reset: RSTb	O

1. Default setting in **bold**.
2. I = Installed, O = Open, x-y indicates shunt across pins x and y.

11.2. Oscillators Jumper Settings

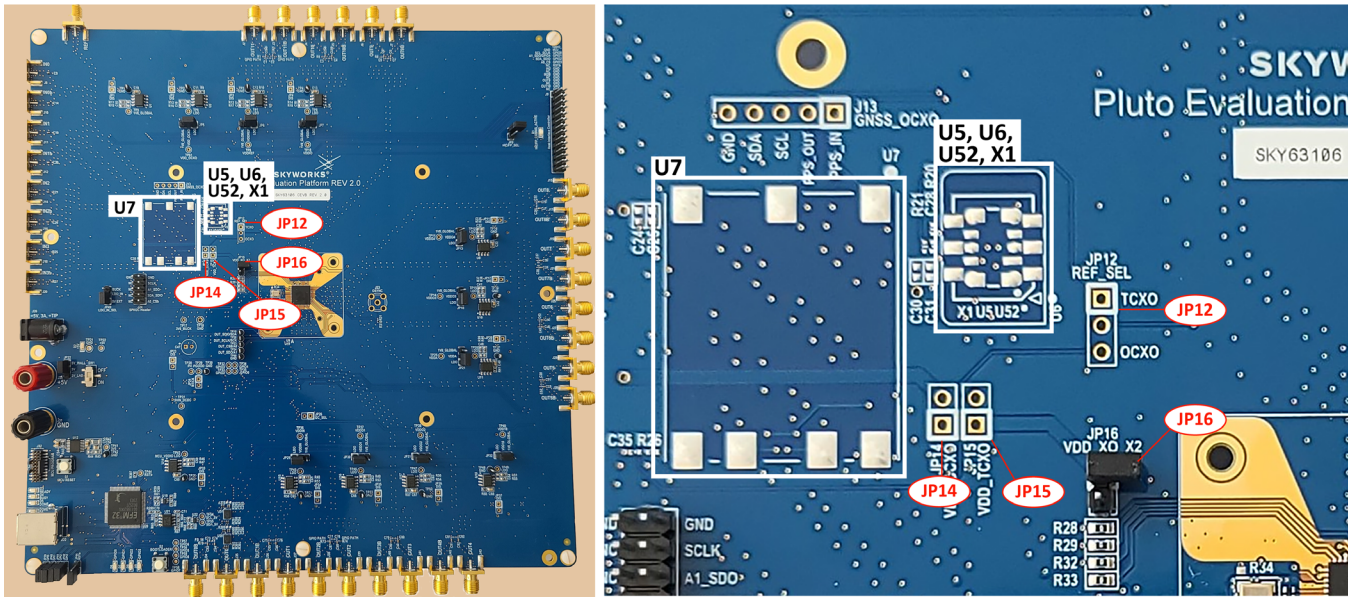

Figure 33. Oscillator and Jumpers

Table 5. Oscillator Jumper Settings

Location	Type	Description of Signal	Jumper Shunt[1]
JP14	2-pin	OCXO (U7) power[2,3]	I
JP15	2-pin	TCXO/OCXO (U5, U6, U27, U52, X1) power	O
JP16	2-pin	XO (X2) power[2]	O
JP12	3-pin	OCXO / TCXO selection to DUT	2-3 (OCXO)

1. I = Installed, O = Open, x-y indicates shunt across pins x and y.
2. Installing the jumper shunt powers on the oscillator. Removing the jumper shunt powers down the oscillator.
3. OCXO only available with the SKY69003 EVB and SKY69102 EVB.

11.3. GPIO and Serial Communication Jumper Settings

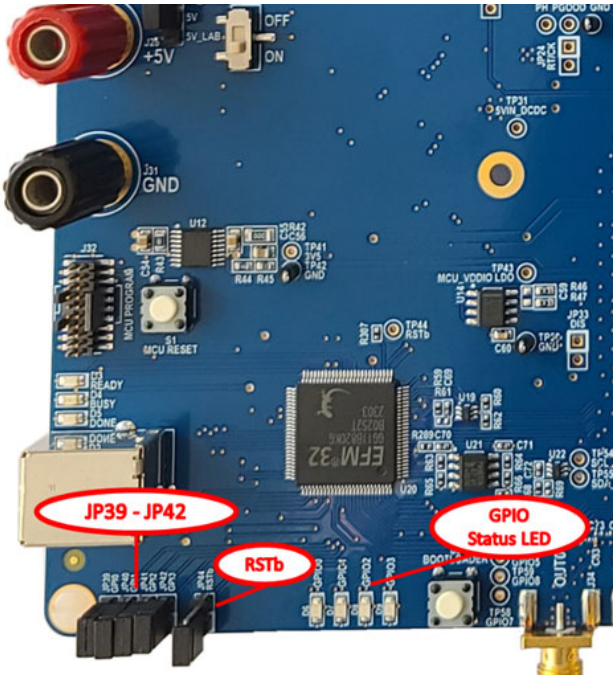

Figure 34. GPIO/RSTb Control Headers

Table 6. GPIO Jumper Settings

Location	Type	Description of Signal	Jumper Shunt[1]
JP39	2-pin	GPI0 toggle[2]	O
JP40	2-pin	GPI1 toggle[2]	O
JP41	2-pin	GPI2 toggle[2]	O
JP42	2-pin	GPI3 toggle[2]	O
JP44	2-pin	RSTb[2]	O

1. I = Installed, O = Open.
2. Install the jumper shunt to assert GPIO Remove the jumper shunt to de-assert GPIO.

Table 7. Serial Communications Jumper Settings

Location	Type	Description of Signal	Jumper Shunt[1]
JP8	2-pin	Host control/field programmer select[2,3]	O

1. I = Installed, O = Open.
2. Install the shunt for DUT connection to the host interface connector (J9). Remove the shunt for DUT to be controlled by the on-board MCU through ClockBuilder Pro via a USB connection. See "8. Serial Communication and Bus Switch" on page 17 for further details.
3. Install the shunt for DUT communication to external location (J24) for field programming or the AccuTime interposer board. Remove this jumper for MCU DUT communication.

11.4. Power Supply Jumper Settings

Figure 35. External Power Supply Selection

Table 8. External Power Jumper Settings

Location	Type	Description of Signal	Jumper Shunt[1]
JP22	3-pin	Host control/field programmer select[2]	1-2

1. I = Installed, O = Open, x-y indicates shunt across pins x and y.
2. Install shunt on position 1-2 for the dc adapter. Install on position 2-3 for banana connectors.

Table 9. LDO Jumper Settings (Figure 2)

Location	Type	Description of Signal	Jumper Shunt[1]
JP5	3-pin	VDD_OCXO selection: 1.8 V global / LDO	1-2
JP6	3-pin	VDDREF selection: 1.8 V global / LDO	1-2
JP7	3-pin	VDDIO selection: 1.8 V global / LDO	1-2
JP13	3-pin	VDDO4 selection: 1.8 V global / LDO	1-2
JP18	3-pin	VDDO3 selection: 1.8 V global / LDO	1-2
JP21	3-pin	VDDA selection: 1.8 V global / LDO	1-2
JP29	3-pin	VDDIN selection: 1.8 V global / LDO	1-2
JP30	3-pin	VDDO1 selection: 1.8 V global / LDO	1-2
JP31	3-pin	VDDO2 selection: 1.8 V global / LDO	1-2
JP32	3-pin	VDDO3 selection: 1.8 V global / LDO	1-2
JP49	3-pin	LDO input selection: BUCK / 5 V dc	1-2

1. I = Installed, O = Open, x-y indicates shunt across pins x and y.

12. Ordering Information

Table 10. Ordering Options

Part Number	Installed Clock Device (DUT)	Clock Device Function	XTAL/XO Reference Included	Holdover OCXO Included
SKY62101AA-EVB	SKY62101	Clock generator	48 MHz	No
SKY63104AA-EVB	SKY63104	Jitter attenuator, DSPLLP	48 MHz	No
SKY63105AA-EVB	SKY63105	Jitter attenuator, DSPLLP/A	48 MHz	No
SKY63106AA-EVB	SKY63106	Jitter attenuator, DSPLLPA/B	48 MHz	No
SKY69003BA-EVB[1]	SKY69003	RFJA, NetSync™	54 MHz	48 MHz
SKY69102BA-EVB	SKY69102	Wireline NetSync	48 MHz	38.88 MHz

1. SKY69003BA-EVB is a shared EVB for SKY69003 and SKY63001 evaluation.

13. Revision History

Revision	Date	Description
A	June 2025	Initial release