USER GUIDE

UG536: Si86P541 Quad Digital Isolator with Integrated Power Transfer Evaluation Board

This evaluation board allows designers to evaluate the Skyworks Si86Pxxx family, which integrates a 500 mW capable isolated dc-dc converter with a two- or four-channel 150 Mbps capable, galvanically isolated digital isolator. The Si86P541-KIT is populated by default with an Si86P541, which can operate from 5.0 V_{TYP} input voltage and has four digital isolation channels in total, where three channels point in the forward direction, and one channel points in the reverse direction.

The Si86P541-KIT is capable of testing all versions of the Si86P family regardless of the total pin count of the selected package or the output voltage. A simple IC change can enable the Si86P541-KIT to test any member of the Si86P family. The desired output voltage can be selected by a simple jumper setting (P36), and the user can configure it by selecting between 3.3 V or 5.0 V. If another output voltage is required, it can be adjusted by changing the output resistor divider.

The Si86P family is designed with enhanced protection features, such as soft-start to limit inrush current at startup, undervoltage lockout, overload and short-circuit protection, overvoltage protection at the output side, and thermal shutdown protection. The board supports the following key features:

- High performance—up to 150 Mbps data rate
- Precise timing—15 ns maximum propagation delay
- SPI isolation naturally (three forward and one reverse channel)
- Compact solution size
- CISPR 32, Class B compliant solution (on four-layer PCB)
- Jumper-selectable output voltage (5 and 3.3 V)
- SOIC20 and SOIC16 packages

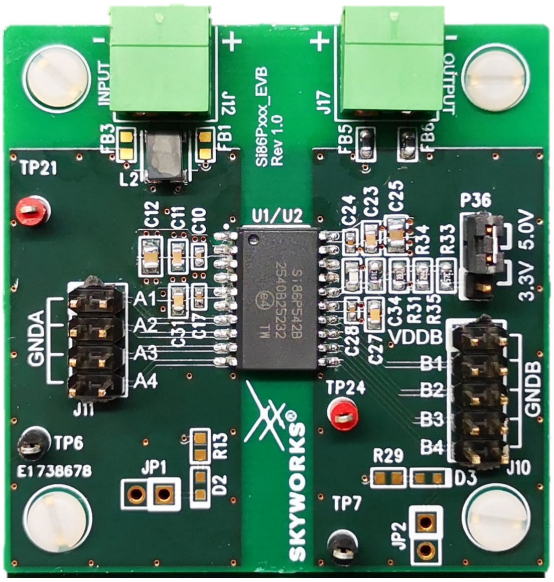


Figure 1. Si86Px Evaluation Board

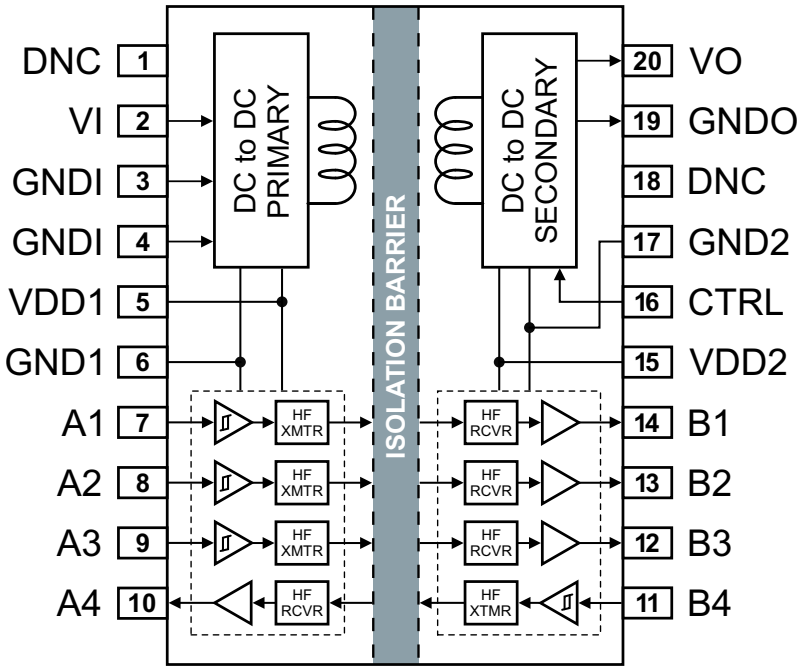


Figure 2. Si86Px41 Pinout

Table 1. SI86Px Evaluation Board Characteristics Using Si86P541

Parameter	Test Condition	Min	Typ	Max	Unit
Input voltage range	P_{LOAD} = 0.5 W	4.75	5.0	5.25	V
Input current at full load	VI = 5.0 V, VO = 5.0 V, IDDO = 100 mA	—	239	—	mA
	VI = 5.0 V, VO = 3.3 V, IDDO = 125 mA	—	243	—	mA
Input current at no load	VI = 5.0 V, VO = 5.0 V, IDDO = 0 mA	—	16	—	mA
	VI = 5.0 V, VO = 3.3 V, IDDO = 0 mA	—	14	—	mA
Load regulation	VI = 5.0 V; VO = 5.0 V; IDDO = 0 to 100 mA (ΔVO (Load) / VO x 100%)	—	0.1	—	%
Line regulation	VI = 4.75 to 5.25 V; IDDO = 100 mA (ΔVO (Line) / ΔVI)	—	5	—	mV/V
Output ripple	VI = 5.0 V; VO = 5.0 V; IDDO = 100 mA C_{OUT} = 0.1 µF || 1 µF || 4.7 µF; BW = 20 MHz	—	48	—	mVpp
	VI = 5.0 V; VO = 3.3 V; IDDO = 125 mA C_{OUT} = 0.1 µF || 1 µF || 4.7 µF; BW = 20 MHz	—	31	—	mVpp
Full load efficiency (DC/DC converter only)	VI = 5.0 V, VO = 5.0 V, IDDO = 100 mA, without EMI Filters	—	43.6	—	%
	VI = 5.0 V, VO = 3.3 V, IDDO = 125 mA, without EMI Filters	—	43.6	—	%
Full load efficiency (end-to-end)	VI = 5.0 V, VO = 5.0 V, IDDO = 100 mA, including EMI Filters	—	42.0	—	%
	VI = 5.0 V, VO = 3.3 V, IDDO = 125 mA, including EMI Filters	—	33.3	—	%
Switching frequency		—	70	—	MHz

1. Schematic

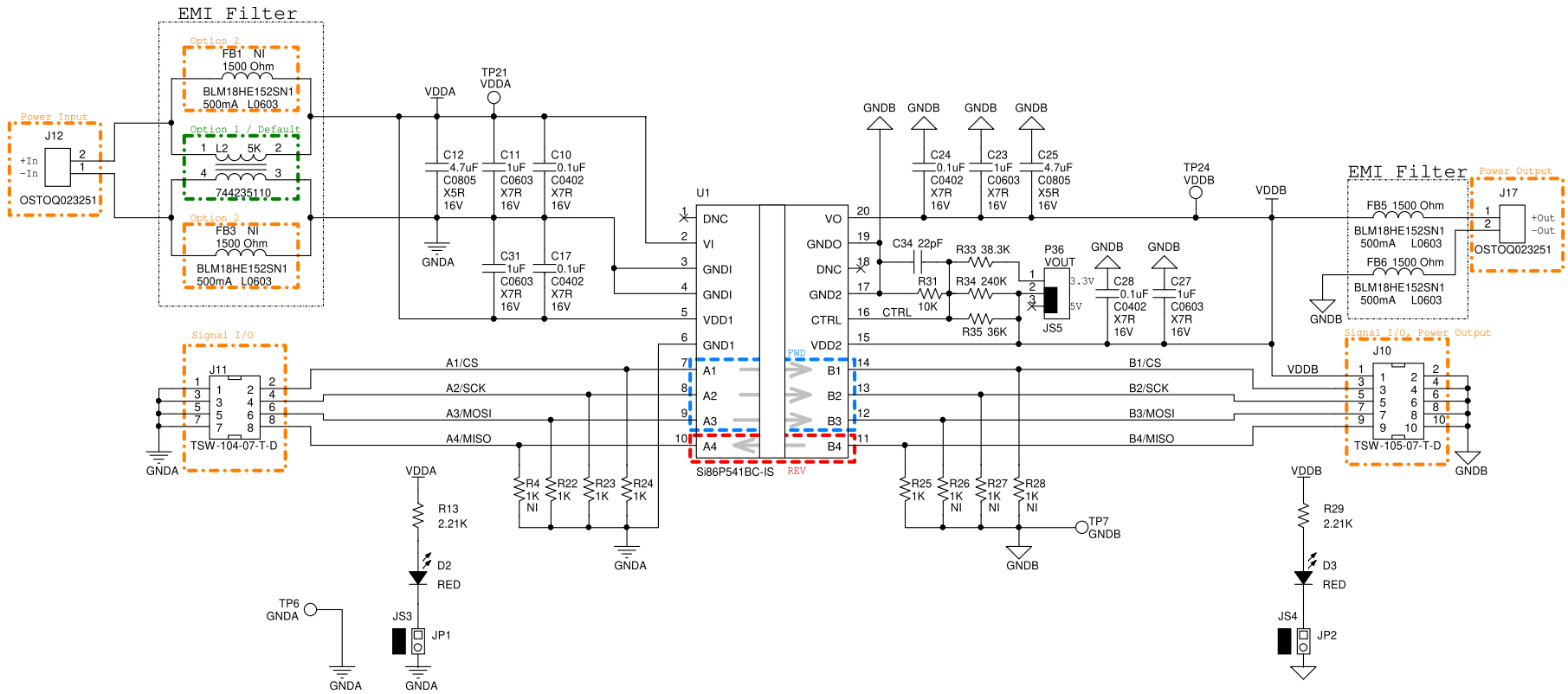
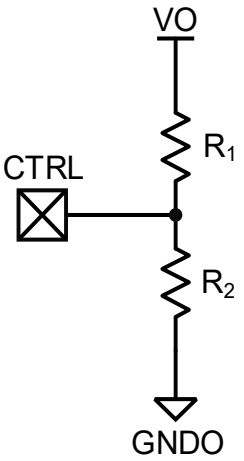


Figure 3. SI86Px Evaluation Board Schematic

2. Output Ripple

The Si86P family uses inherently stable hysteretic control. The on-chip comparator senses the output voltage through the output resistor divider, then compares it against the on-chip reference voltage. If the divided output voltage crosses the lower threshold, the comparator turns on the power transfer from the primary side to the secondary side, so the output voltage starts ramping. Some microseconds later, the ramping output voltage crosses the higher threshold; the comparator turns off the power transfer, and the output voltage starts falling again. This means that the output voltage moves between the lower and higher thresholds at the control frequency. The control frequency is not a fixed frequency but, rather, depends on many variables, such as output capacitance, hysteresis band, and load current. It is normally two orders of magnitude lower than the real switching frequency of the converter, which is 70 MHz. Both output voltage (VO) and hysteresis band (ΔVO) can be adjusted by proper selection of the output resistor divider values.



$$VO = V_{REF} \times \frac{R_1 + R_2}{R_2}$$ (VO can be set in the range of 3.15 V to 5.25 V)

$$\Delta VO = 2 \times I_{HYS} \times (R_1 + R_2)$$

where V_{REF} = 1.21 V, I_{HYS} = 0.5 µA

Figure 4. Output Voltage and Hysteresis Band Calculations

Figure 5 below shows the measured output ripple with 5.0 V input, 5.0 V output, and 50 mA load current. The hysteresis band was set to 41 mV by using R1 = 31.3 kΩ and R2 = 10 kΩ, and the actual measured hysteresis was 48 mV.

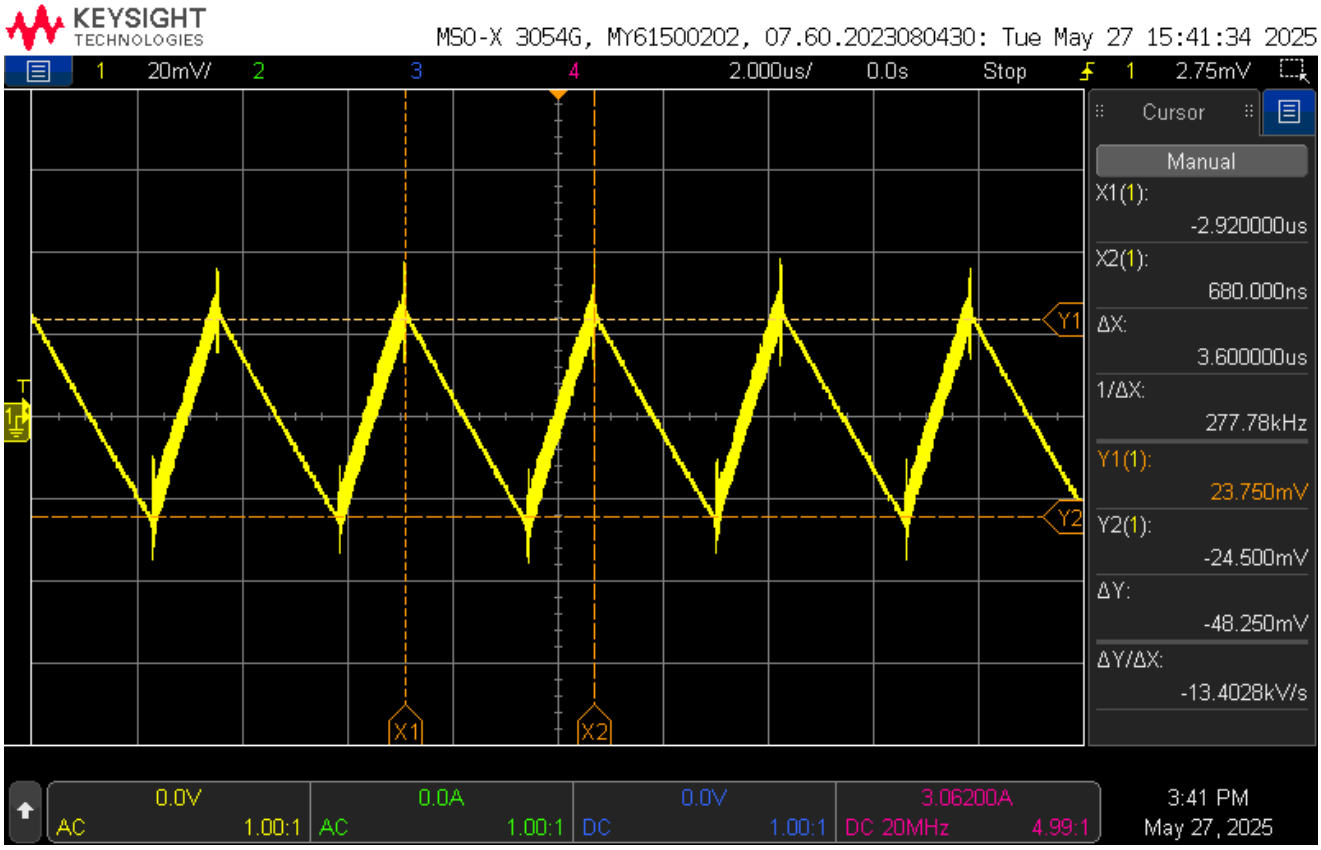


Figure 5. Output Ripple with 5.0 V Input, 5.0 V Output, and 50 mA Load

Figure 6 below shows the measured output ripple with 5.0 V input, 3.3 V output and 62.5 mA load current. The hysteresis band was set to 27 mV by using R_1 = 17.2 kΩ and R_2 = 10 kΩ, and the actual measured hysteresis was 31 mV.

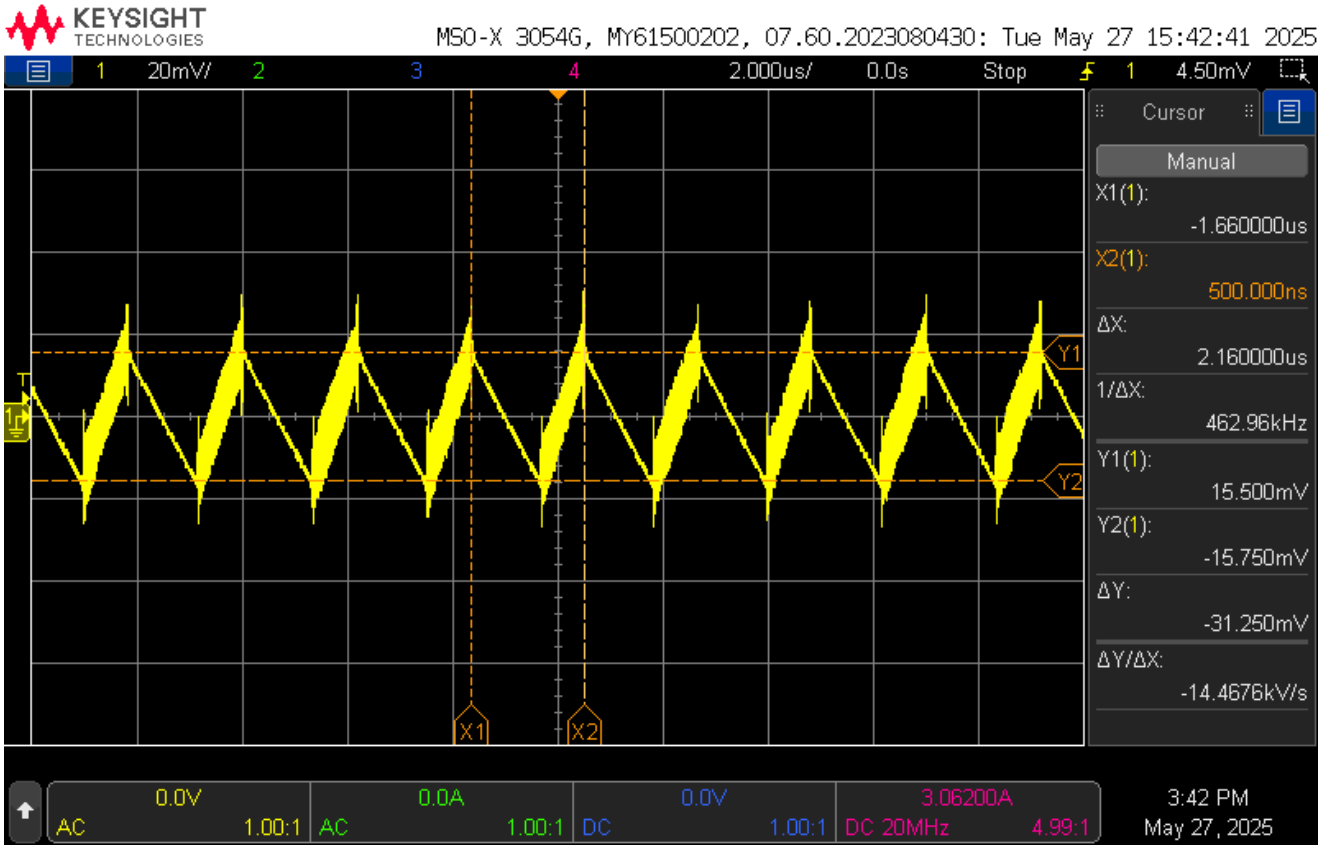


Figure 6. Output Ripple with 5.0 V Input, 3.3 V Output, and 62.5 mA Load

2.1. Proper Measurement of Output Voltage Ripple

The integrated dc-to-dc converter of the Si86P541 operates at a very high switching frequency of 70 MHz, and voltage ripple measurements require careful measurement setup for accurate results. In noisy environments, a common practice is to minimize inserted parasitic loop inductance between the scope and DUT ground by using short “pigtail” connections. This technique yields significant noise attenuation from the switching dc-to-dc converter, but even more attenuation can be achieved if loop inductance is further reduced. One way to accomplish this is to directly solder a short, small-diameter RG-178B coaxial cable to the top of the output bypass capacitor creating an extremely small ground connection loop area and minimizing the main contributor to noise pickup. Furthermore, the measurement signal-to-noise ratio increases by approximately 20 dB due to the lack of a 1:10 divider, which is, by design, part of our commonly used 1:10 scope probes.

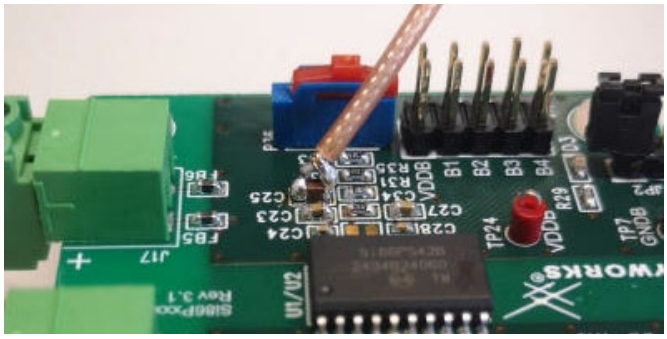


Figure 7. Output Voltage Measurement Using Coaxial Cable Method

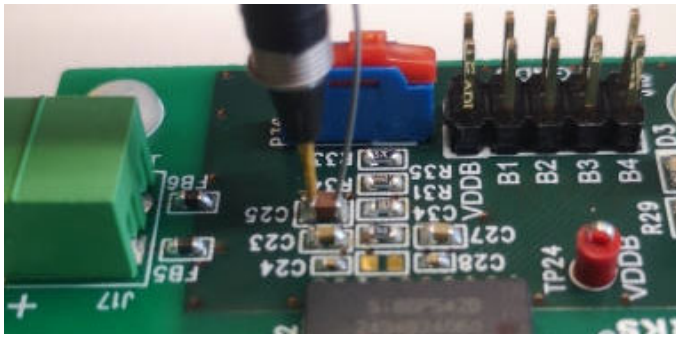


Figure 8. Output Voltage Measurement Using “Pigtail” Connection on 1:10 Scope Probe

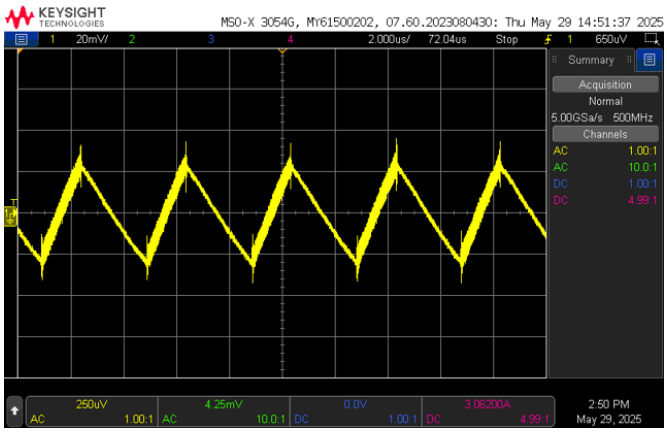


Figure 9. Captured Output Voltage Ripple Using Coaxial Cable Method (Measurement Bandwidth: 200 MHz)

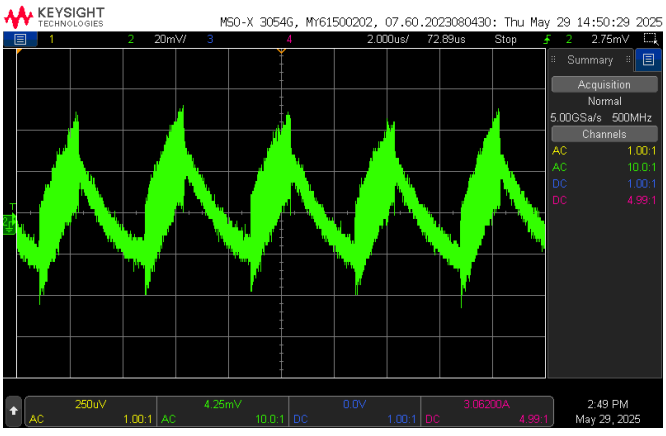


Figure 10. Captured Output Voltage Ripple Using “Pigtail” Connection and 1:10 Scope Probe (Measurement Bandwidth: 200 MHz)

3. Load Regulation

The SI86Px evaluation board shows a typical application circuit and is equipped with EMI filters at the input and output sides. Although the Si86P541 has excellent load regulation capability (around 0.1%), the series resistance of the EMI filters naturally degrades the system load regulation to around 1.71% in the case of 5.0 V input/5.0 V output voltage settings (1.71% equals to 86 mV drop on the output voltage). Figure 11 below shows the SI86Px evaluation board output voltage versus load current curve at 5.0 V input/5.0 V output voltage in two configurations. The red curve shows the true capabilities of the Si86P541 without added EMI filters, while the green curve shows the complete EVB performance including EMI filters. The output-side ferrite bead dc resistance is the main contributor to load regulation degradation. If necessary, load regulation can be improved by selecting other types of ferrite beads with similar impedance curves but less dc resistance. The curves were measured far beyond the 0 to 100 mA recommended operating range of the output current, and they show a sudden fall on the output voltage at around 122/142 mA load current caused by the activated overload/short-circuit protection circuit of the Si86P541.

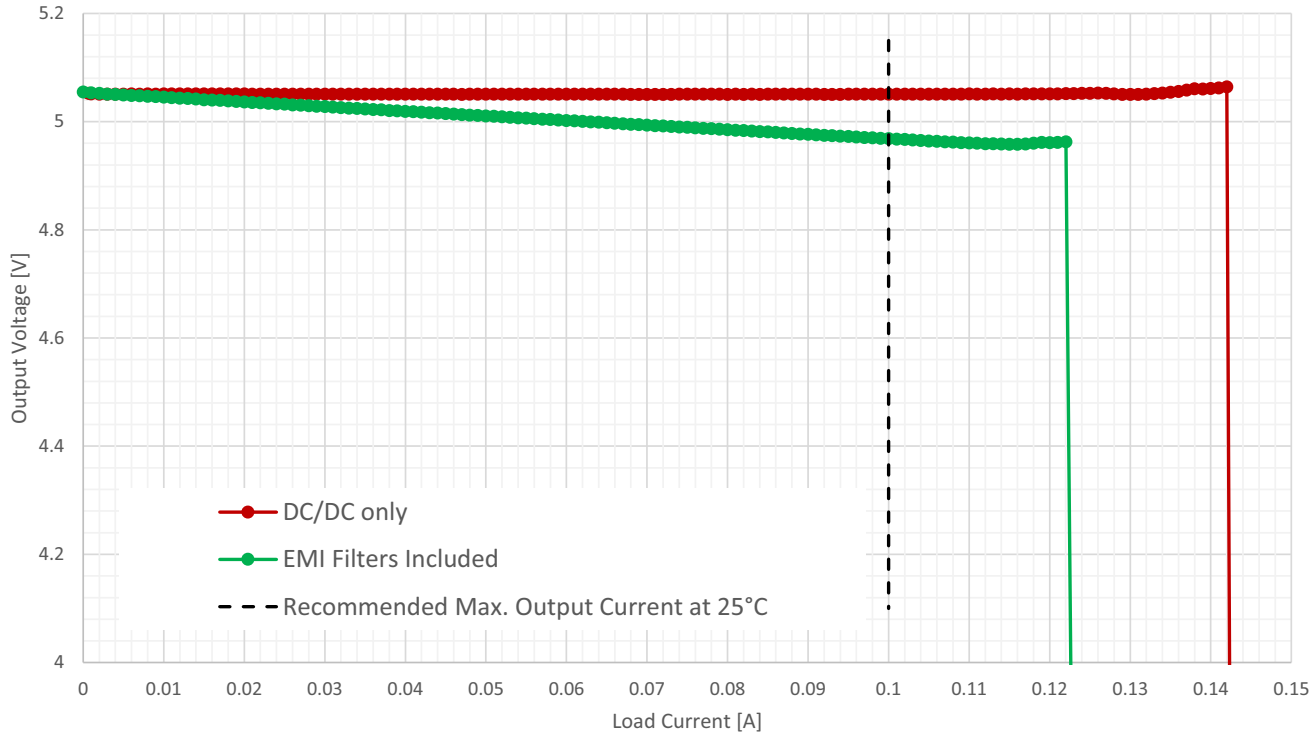


Figure 11. Load Regulation of SI86Px Evaluation Board in 5.0 V Input/5.0 V Output Configuration

The output voltage versus output load curve of 5.0 V input/3.3 V output configuration is shown in Figure 12 below. The red curve still shows excellent load regulation for the Si86P541 itself without EMI filters, while the complete board shows 3.27% load regulation. This is a little bit higher than in the previous case due to the higher output current, which develops higher voltage drop on the EMI filters and the lower output voltage. The recommended output current range is 0 to 125 mA for this configuration.

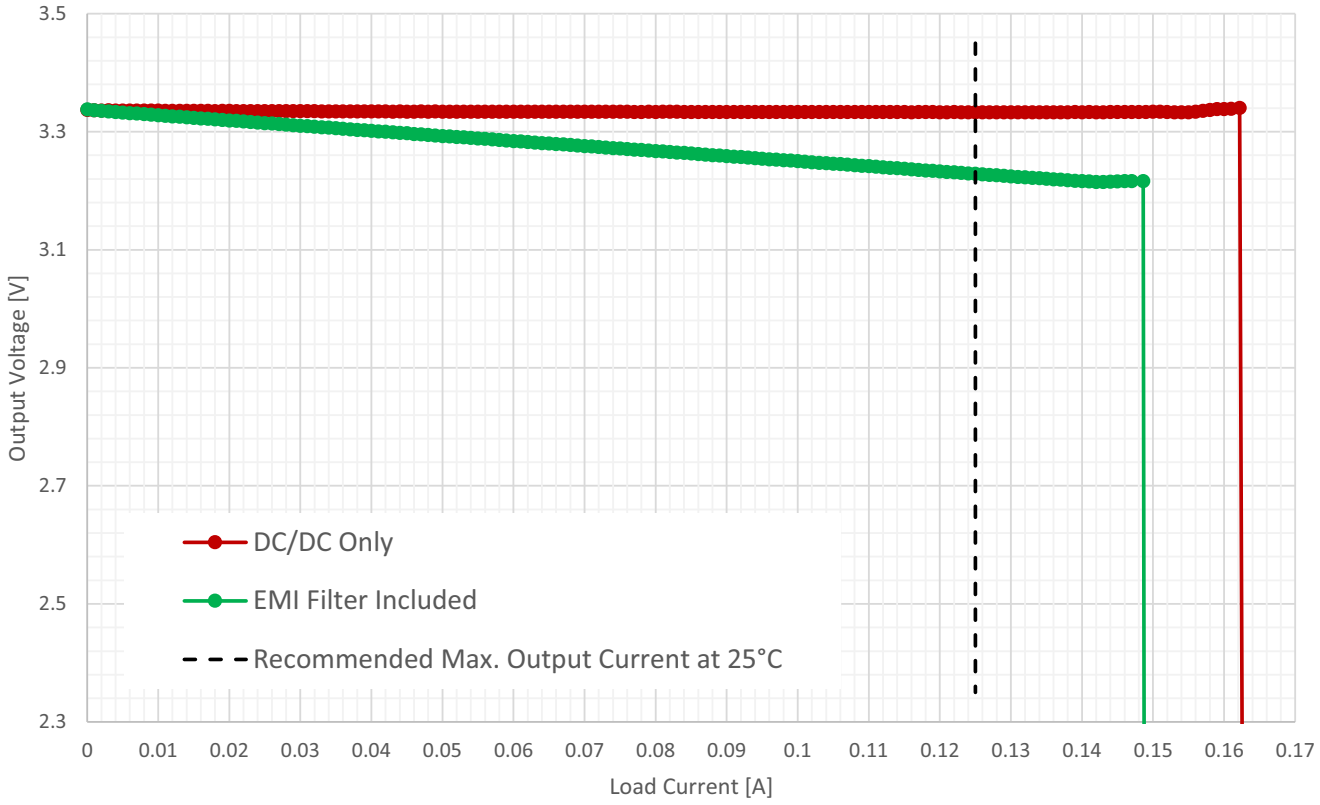


Figure 12. Load Regulation of SI86Px Evaluation Board at 5.0 V Input/3.3 V Output Configuration

4. Line Regulation

The Si86P541 has excellent line regulation capability of less than 5 mV/V. Figure 13 below and Figure 14 on page 11 show the measured results of the SI86Px evaluation board at both 5.0 V and 3.3 V output voltage settings while the input voltage was swept from 4.75 V to 5.25 V. As can be seen in the plots, the change on the output voltage is roughly less than half a vertical division (one vertical division is equal to 5 mV) while the input voltage changes 0.5 V, so the actual line regulation is somewhere below 5 mV/V.

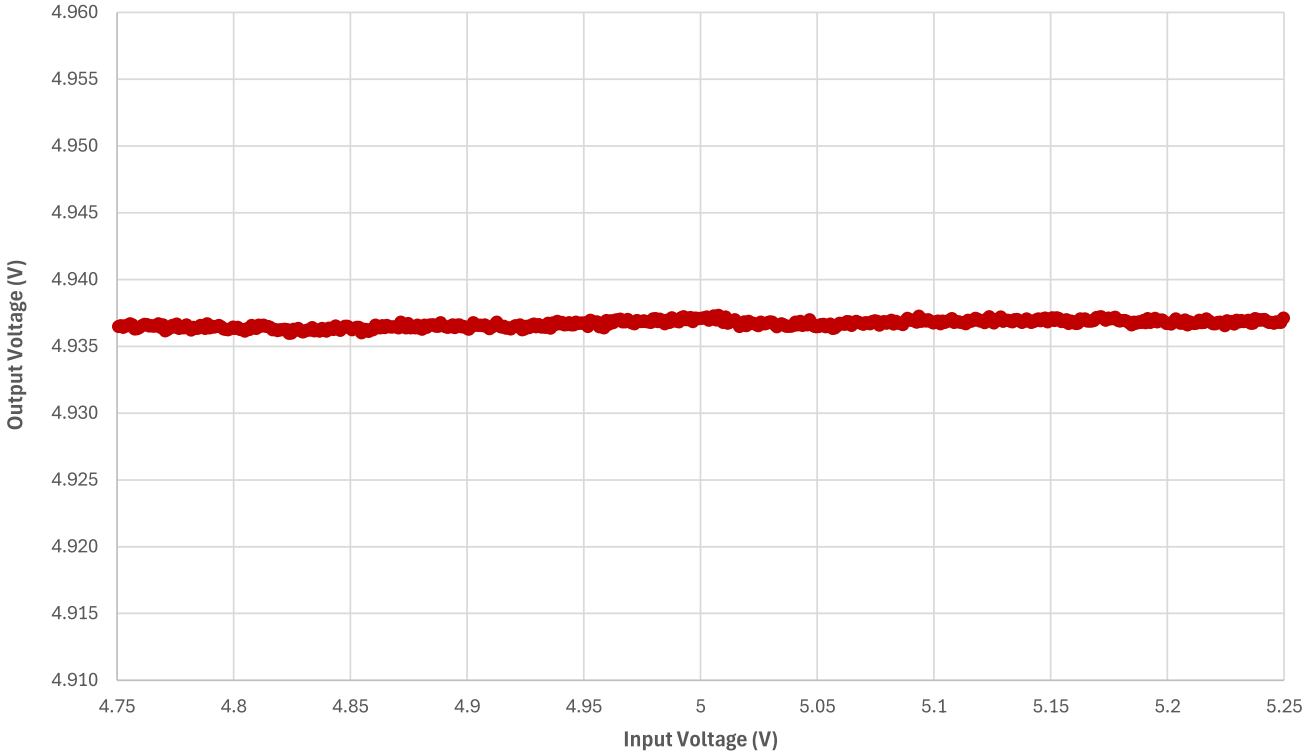


Figure 13. Line Regulation of the SI86Px Evaluation Board at 5.0 V Output Setting (I_{OUT} = 100 mA)

As can be seen below, the SI86Px evaluation board shows even better results at 5 V input/3.3 V output setting.

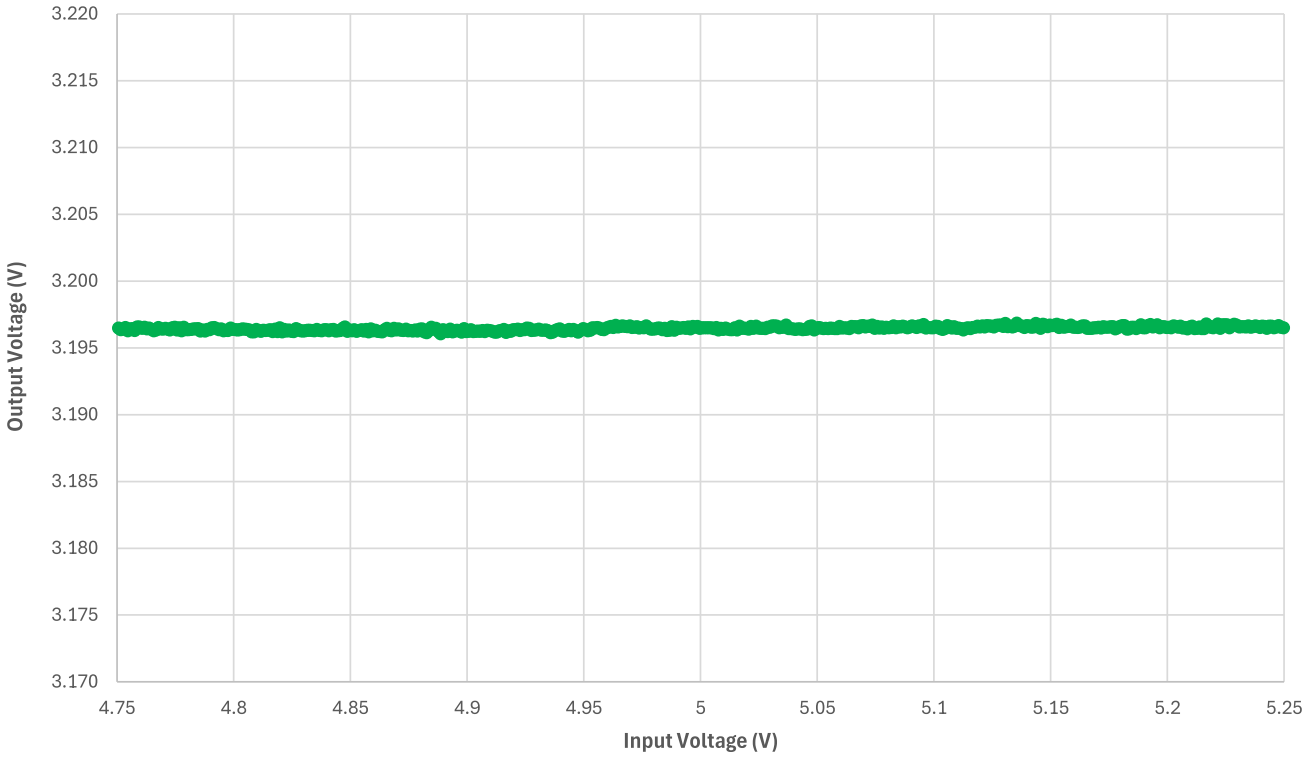


Figure 14. Line Regulation of the SI86Px Evaluation Board at 3.3 V Output Setting (I_{OUT} = 125 mA)

5. Efficiency

Efficiency curves were measured in $5V_{IN}/5V_{OUT}$ and 5 $V_{IN}/3.3V_{OUT}$ configurations. The full board curve shows end-to-end efficiency (from Connector J12 to J17) including the effect of the input and output side EMI filters. DC/DC-only curves were measured directly on the power pins of the Si86P device excluding the extra efficiency drop on the EMI filters.

Table 2. SI86Px Evaluation Board Characteristics Using Si86P541

Configuration	$5V_{IN}/5V_{OUT}$ DC/DC Only	$5V_{IN}/5V_{OUT}$ Full Board	$5V_{IN}/3.3V_{OUT}$ DC/DC Only	$5V_{IN}/3.3V_{OUT}$ Full Board
Peak efficiency	43.6%	42.0%	34.8%	33.3%

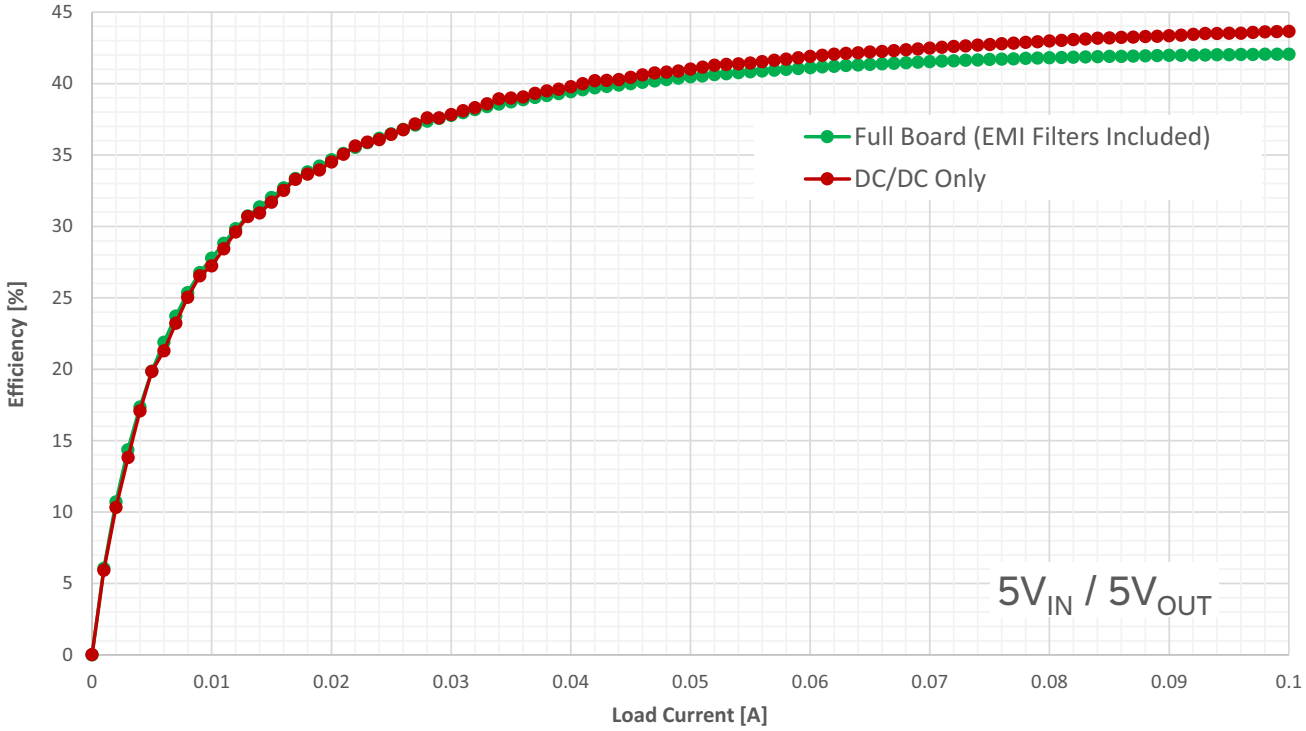


Figure 15. SI86Px Evaluation Board Efficiency Curve at 5.0 V Input/5.0 V Output Configuration

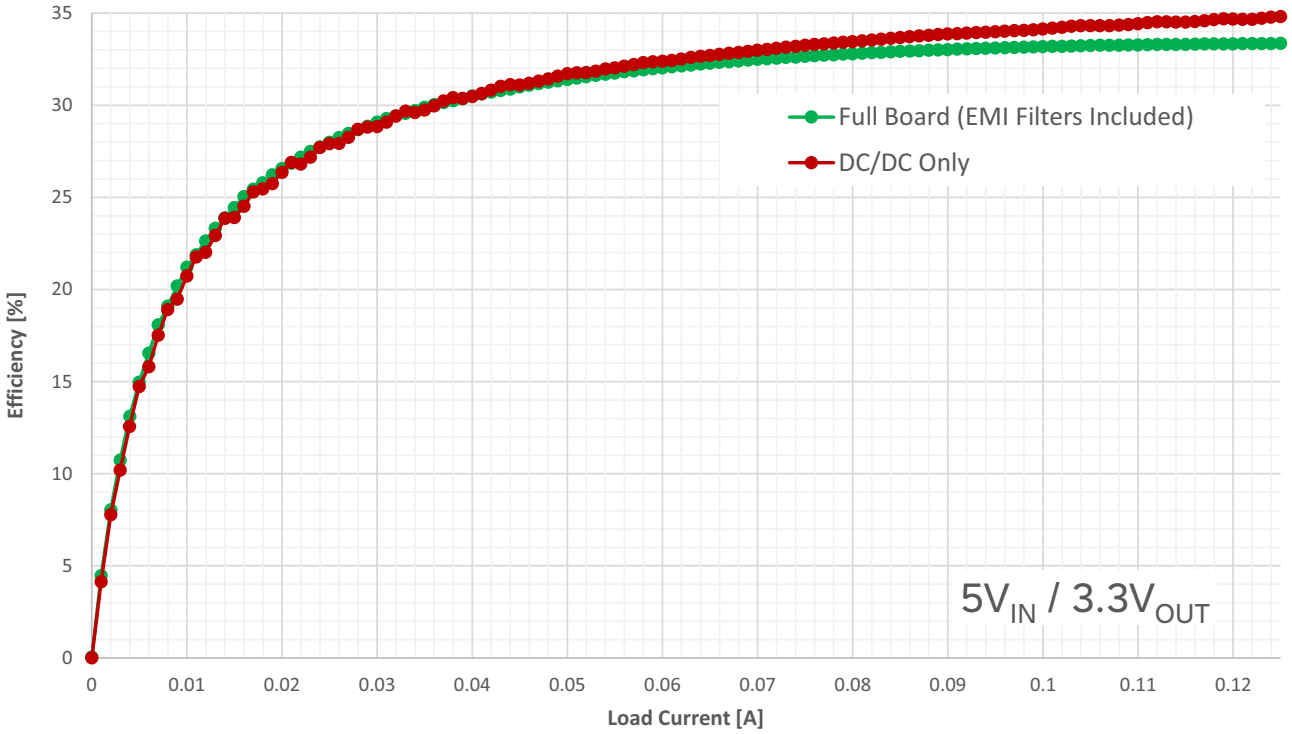


Figure 16. SI86Px Evaluation Board Efficiency Curve at 5.0 V Input/3.3 V Output Configuration

6. Thermal Measurements

IR photos were taken at 25 °C room temperature and full load conditions (100 mA load for 5 V_{IN}/5 V_{OUT} setting and 125 mA for 5 V_{IN}/3.3 V_{OUT} setting). Although the output power is lower in the 3.3 V output case, the junction temperature is still higher here because the effect of its lower efficiency is more pronounced in the IR image than in that of its lower-output power.

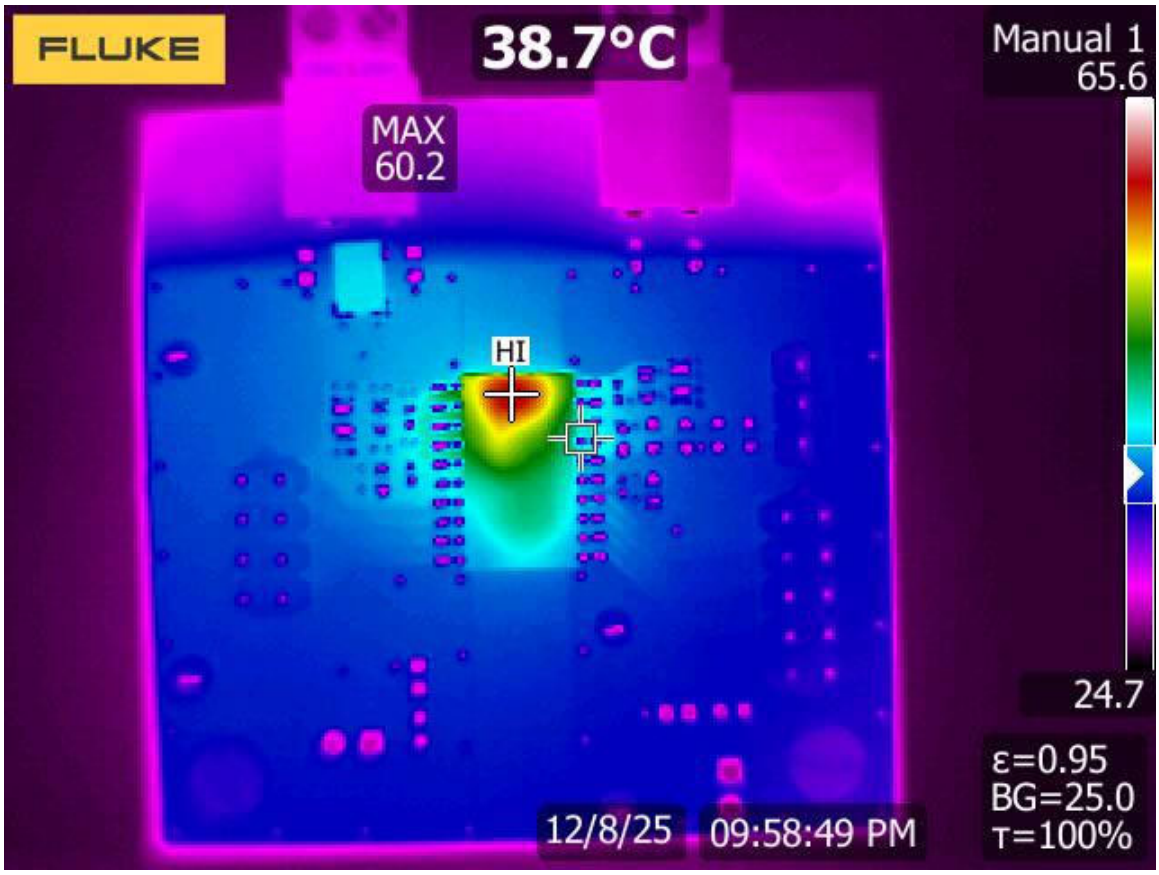


Figure 17. SI86Px Evaluation Board IR Photo in 5.0 V input/5.0 V Output Configuration (100 mA Load) (Max. Device Temperature: 60.2 °C)

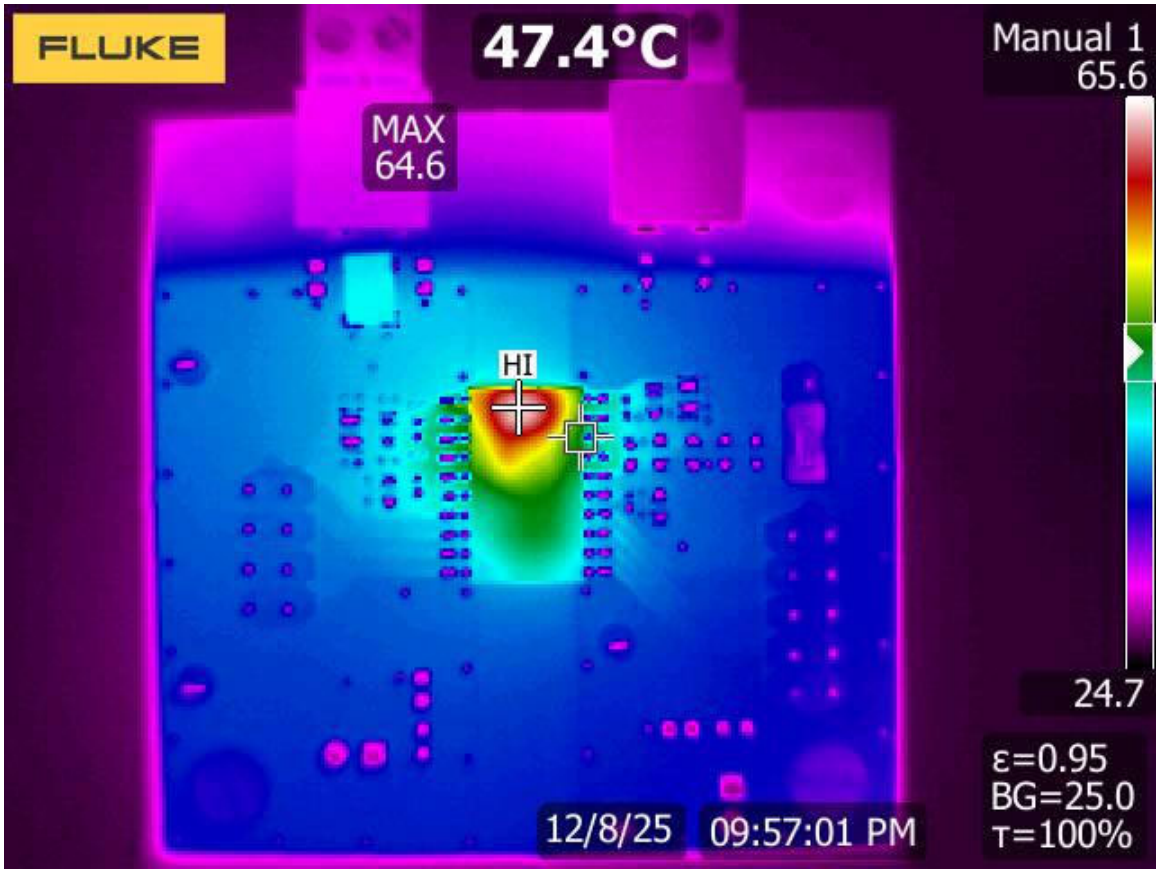


Figure 18. SI86Px Evaluation Board IR Photo in 5.0 V Input/3.3 V Output Configuration (125 mA Load) (Max. Device Temperature: 64.6 °C)

7. Layout

The Si86P family uses integrated miniature transformers for power transfer across the isolation barrier. Miniature transformers require the use of high switching frequencies in order to achieve small footprint and good system efficiency, but they also require more careful EMI radiation reduction techniques to pass EMI tests.

The SI86Px evaluation board employs the following techniques to pass the CISPR 32 Class B test:

- On-chip switching frequency dithering
- Four-layer PCB with interlayer stitching capacitor
- Input side common-mode choke
- Output side ferrite beads

The SI86Px evaluation board passed on CISPR 32/EN 55032, Class B tests. The board was tested in two configurations, and the results for the 5 V input, 3.3 V output configuration can be seen in the plot shown in Figure 19 below. The measurement was taken at full-load condition (125 mA).

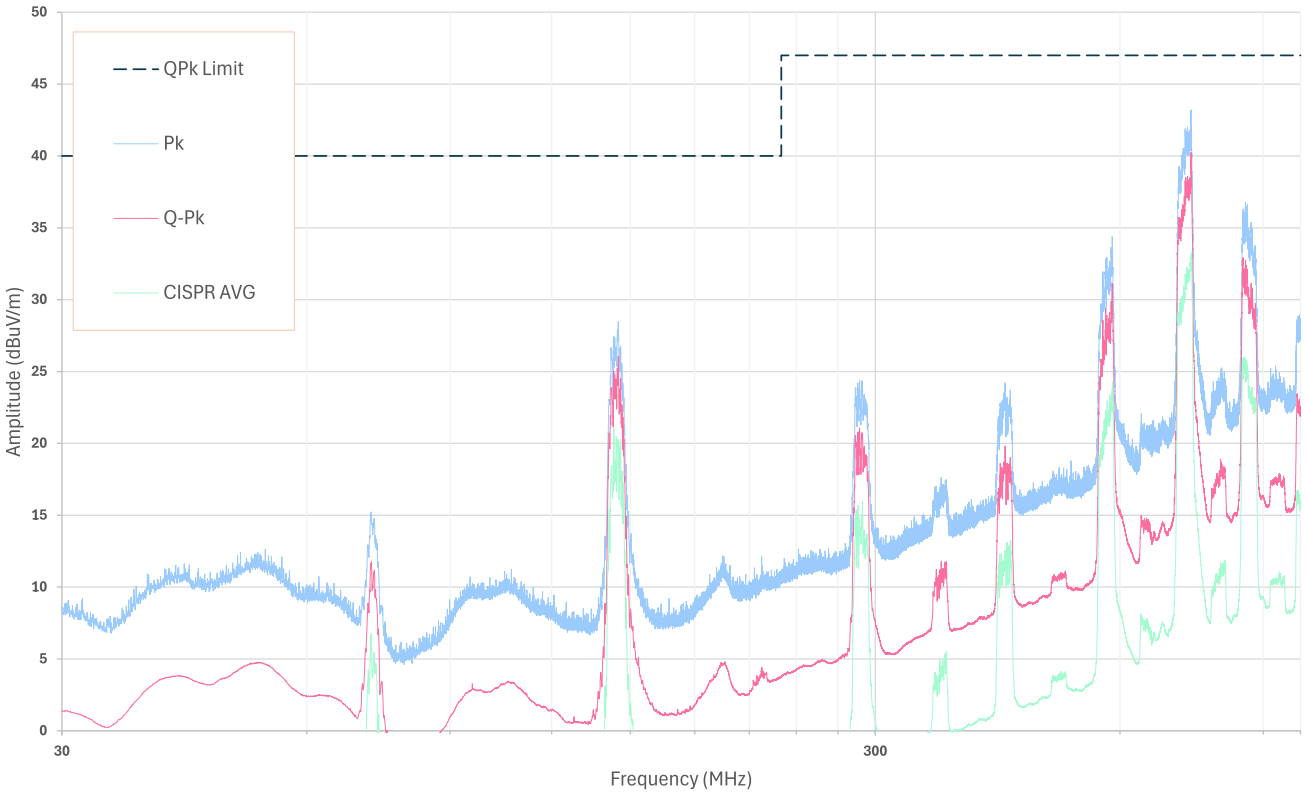


Figure 19. CISPR 32 Test Result of SI86Px Evaluation Board at 5.0 V Input, 3.3 V Output, and Full-Load Condition

Results for the 5.0 V input, 5.0 V output configuration can be seen in Figure 20 below. It was also measured at full-load condition (100 mA).

The test results in Figure 19 above and Figure 20 below show the maximal values from different measurement heights, polarizations, and angles. The blue curve was measured using peak detector, the pink curve with quasi-peak, and the green curve with CISPR AVG. If a result is too close to the limit line, selected frequencies were remeasured with a quasi-peak detector for more accurate results, and those results were shown as Final QPk spots on the plot. To obtain passing results, every point on the quasi-peak curve and every “Final QPk” point should be below the quasi-peak limit line.

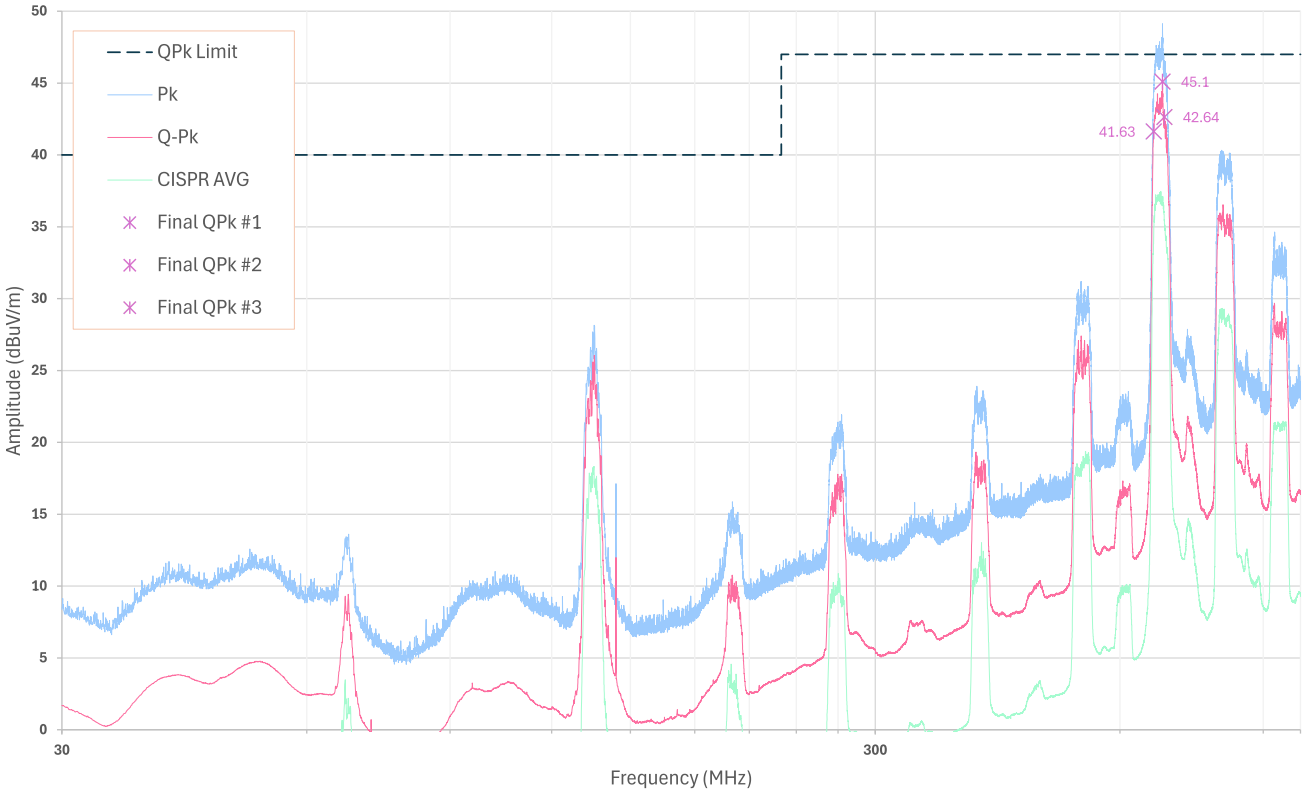


Figure 20. CISPR 32 Test Result of Si86Px Evaluation Board at 5.0 V Input, 5.0 V Output, and Full-Load Condition

7.1. Internal Layer Stitching Capacitor

Common-mode noise current is the major source of EMI in isolated power converters. The high dv/dt of the primary or secondary switch node and the parasitic capacitance of the integrated power transformer create common-mode current through the transformer. This common-mode current can cause unwanted radiated emissions as it takes unintended paths back to its source—typically through external system cabling. Although the generated common-mode current is quite low, the loop area of the current can be quite large, allowing significant radiation to occur. The key to EMI mitigation here is to minimize the loop area of the common-mode current path. Typically, a high-voltage Y2 capacitor is used over the isolation barrier as a local return path for common-mode current, but its lead inductance makes it somewhat ineffective at the high switching frequencies of the Si86P device. An alternative way to create a very low inductance capacitor through the isolation barrier is to overlap the internal PCB layers as shown in the internal layer prints below. Primary side ground on the Internal 1 layer is extended entirely to the secondary side, and the secondary side ground on Internal layer 2 is extended to the primary side while maintaining proper isolation distances on the internal layers. In this way, the FR4 core material acts as a dielectric layer between the capacitor plates formed by the internal layers. The achievable stitching capacitance on a four-layer 50 mm x 50 mm PCB can reach 270 pF.

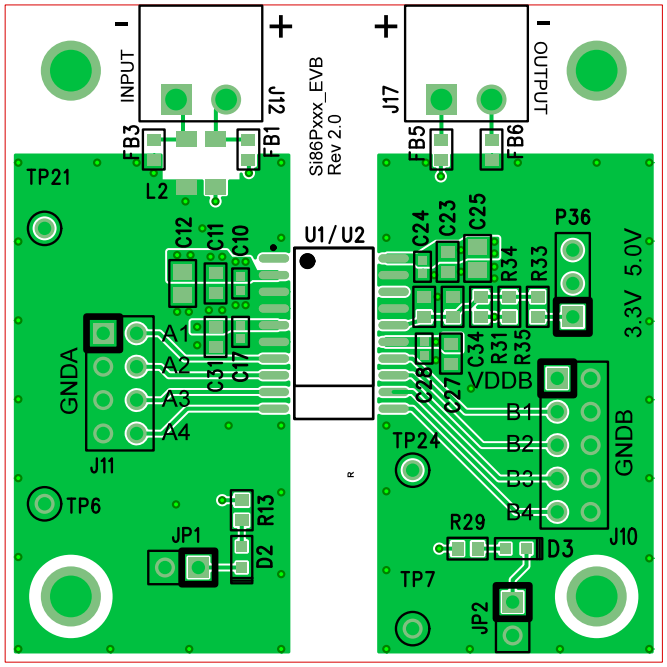


Figure 21. Top Layer of the SI86Pxxx EVB

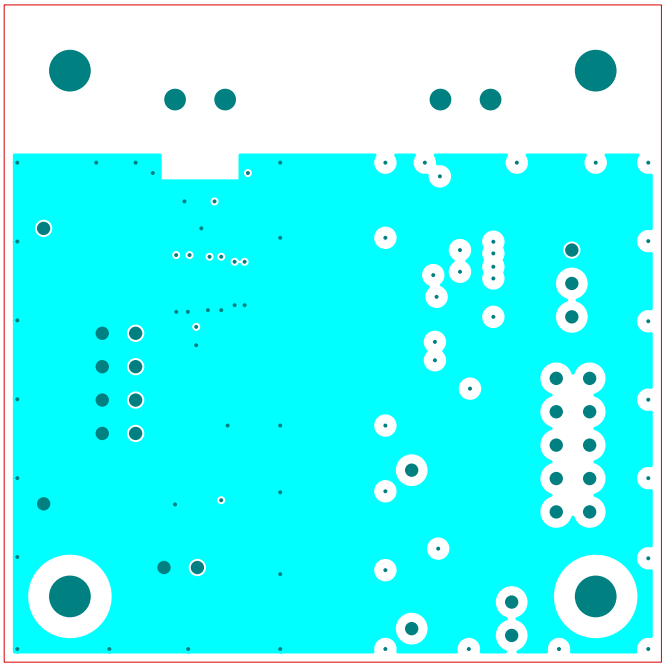


Figure 22. Internal 1 Layer of the SI86Pxxx PCB

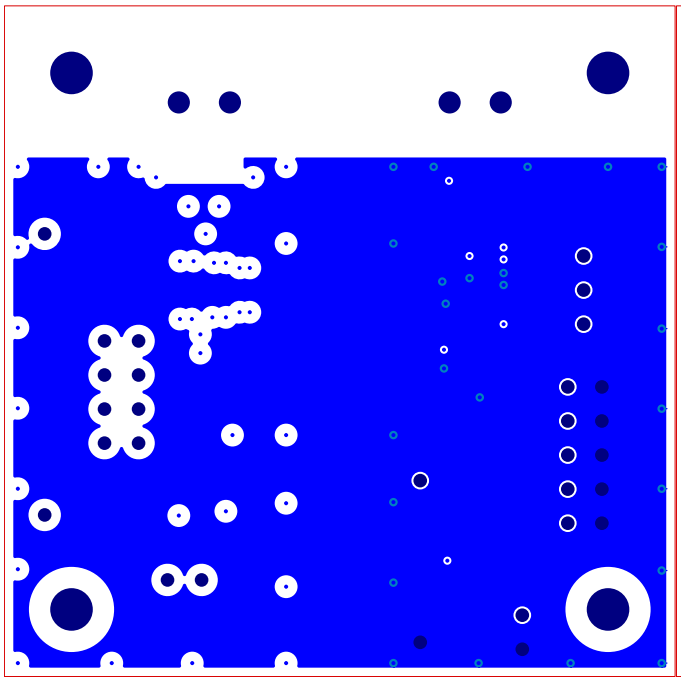


Figure 23. Internal 2 Layer of the SI86Pxxx Evaluation Board PCB

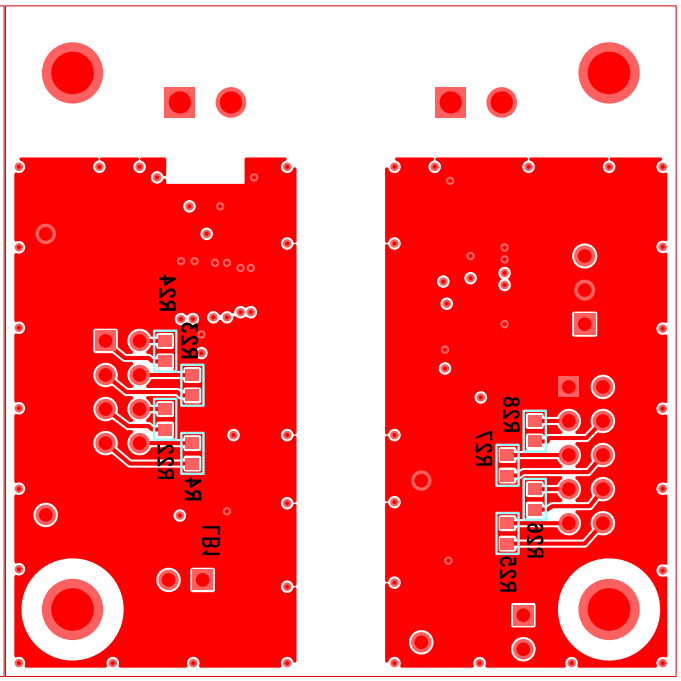


Figure 24. Bottom Layer of the SI86Pxxx Evaluation Board

7.2. Input and Output Side Filtering

While the internal-layer stitching capacitor bypasses common-mode current back to its primary side source locally, further filtering on the input and output sides can prevent the common-mode current from taking undesired paths on the externally attached power wires. Ferrite beads or common-mode chokes can be inserted between the input and output sides of the Si86P related circuits and the rest of the system, preventing the formation of common-mode current loops on the external wiring. The selected common-mode choke (L2) at the input side of the SI86Px evaluation board can block the common-mode current by its 4 kΩ impedance at the most important frequency (the second harmonics of the switching frequency) while the selected ferrite beads (FB5/FB6) on the secondary side can show at least 1.6 kΩ impedance at the same frequency.

7.3. Switching Frequency Dithering

The Si86P uses on-chip switching frequency dithering to reduce its radiated emission level. It uses slightly varying switching frequency, turning sharp, high-amplitude noise peaks on the EMI plot into broader, lower-amplitude, noise-reducing peak emissions.

7.4. Bypass Capacitors

These capacitors have an important function for differential noise filtering. Although differential current loops have much smaller loop area than their common-mode counterparts, they can still cause EMC issues if the bypass capacitors cannot effectively suppress voltage ripple on the input or output sides of the converter. The Si86P family integrates an isolated dc-to-dc converter with high-speed digital isolators, and these two different parts require different bypassing. The dc-to-dc converter operates at much higher instantaneous peak currents; therefore, it requires more robust bypass capacitor banks. For effective filtering, the VI/GNDI pins at the primary side and the VO/GNDO pins at the secondary side require three different capacitors: a 100 nF 0402 sized as close as possible to the supply pins, a larger 1 µF 0603 sized capacitor next to it, and, finally, a minimum 4.7 µF 0805 sized “bulk” capacitor. To achieve the lowest possible trace parasitic inductance, keep these capacitors on the same layer and as close to the Si86P device as possible.

The digital isolator pins (VDD1/GND1 at the primary side and VDD2/GND2 at the secondary side) require less bypassing because they operates at much lower instantaneous peak current. The bypass capacitor bank can only be formed by 100 nF 0402 sized and 1 µF 0603 sized capacitors.

8. Ordering Information

Part Number	Description	Evaluation Board Part Number
Si86P541	Si86P541 Quad Digital Isolator with Integrated Power Transfer	Si86P541EK1