USER GUIDE

UG537: Si82Fx Gate Driver Board (GDB) User Guide

Features

- Two-input, universal gate driver
- User-programmable dead-time
- Overlap protection
- Independent control of turn-on/turn-off timing with Selectable Variable Current Drive (SelVCD™)
- Flexible isolated power supplies
- 6 kV_{RMS} safety-rated isolation
- > 40 kV/µs common-mode transient immunity (CMTI)[1]
- Reverse polarity protection for 12 V input supply
- Differential inputs for increased noise immunity
- Module temperature (NTC) output as frequency modulated digital signal
- Reference design available

Additional System Components

The Si82Fx GDB is highly versatile but must be combined with other components to form a complete system. You can choose various elements to complete your evaluation or prototyping system and tailor it to your specific needs.

For example: Because the Si82Fx requires differential signal inputs, and most lab equipment only provides single ended inputs, it may be helpful to use the Wolfspeed Differential Transceiver Companion Tool, listed below to provide that translation.
Tested components include the following:

- Differential Transceiver Companion Tool
- Wolfspeed™ WolfPACK™ Power Module
- Wolfspeed SpeedVal™ Kit Modular Evaluation Platform

Description

The Si82Fx Gate Driver Board (GDB) is ideal for driving power module solutions and discrete transistors. The two-channel, isolated, current-mode gate driver solution features a differential digital interface and optimized onboard isolated power supply. The output stage features SelVCD™ technology that adjusts output current between eight selectable levels, eliminating the need for gate resistors and clamping any Miller effect currents. Status indicator LEDs and test points make evaluation and prototyping easy.

1.The Si82Fx driver has a common-mode immunity of >200 kV/µs. However, the performance of this board is limited by the Si88421 digital isolator.

1. Electrical Specifications

Table 1. Si82Fx Gate Driver Board Electrical Specifications

Symbol	Parameter	Min	Nominal	Max	Unit
V_{DC}	Supply voltage	10.2	12	13.2	V
V_{IH}	High-level logic input voltage	2.0	—	5.5	V
V_{IL}	Low-level logic input voltage	0	—	0.8	V
f_s	Maximum switching frequency (module/MOSFET dependent, see power estimation section)	—	100	—	kHz
T_{OP}	Ambient operating temperature	–50	—	85	°C
T_{STG}	Storage temperature	–50	—	125	°C

2. Pin Descriptions

Signals and power to the board are provided through J1, a 16-pin connector that provides access to key device signals for evaluation and integration purposes. The footprint for J1 is a 24-pin footprint. However, only 16 of the pins are actively used (and are defined) in this document. The remaining eight pins should be left unconnected in all applications, as driving or loading them may result in undefined behavior or potential damage to the gate driver board.

Table 2. Si82Fx Gate Driver Board Pin Descriptions

Pin Number	Parameter	Description
1	VDC	Power supply input pin (+12 V nominal).
2	Common	Common.
3	HS-P[1]	Positive line of 5 V differential high-side pulse-width modulation (PWM) signal pair. Terminated Into 360 Ω.
4	HS-N[1]	Negative line of 5 V differential high-side PWM signal pair. Terminated Into 360 Ω.
5	LS-P[1]	Positive line of 5 V differential low-side PWM signal pair. Terminated Into 360 Ω.
6	LS-N[1]	Negative line of 5 V differential low-side PWM signal pair. Terminated Into 360 Ω.
7	NC	Not connected.
8	NC	Not connected.
9	RTD-P[1]	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via frequency.
10	RTD-N[1]	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via frequency.
11	NC	Not connected.
12	Common	Common.
13	PWM EN	Pull down or leave floating to disable PWM input logic. Pull up to enable. Gate driver output is held low through turn-off gate resistor if power supplies are enabled.
14	Common	Common.
15	NC	Not connected.
16	Common	Common.

1. Inputs 3 to 6, 9, and 10 are differential pairs.

3. Signal Descriptions

3.1. PWM Signals

High-side and low-side PWM signals are RS-422-compatible differential inputs. The termination impedance of the differential receiver is 360 Ω. Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead-time generator. Programmable dead time is provided by resistor selection. For more information, see “9.1. Dead Time” on page 10.

3.2. Resistance Temperature Detector (RTD) Output with Negative Temperature Coefficient (NTC) Sensors

RTD output is a differential signal that returns the resistance of the temperature sensor (NTC) integrated into some modules. The signal is a frequency-modulated signal that encodes the resistance of the temperature sensor. The approximate temperature of the module can be determined from this resistance.
See “7. Temperature Feedback” on page 8 for further details.

3.3. Pulse-Width Modulation Enable (PWM EN)

This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down or left floating, the isolated drivers for both channels are disabled, and the gates are both pulled low through RG-OFF. All protection circuitry and power supplies continue to operate including the RTD output

3.4. Overvoltage and Reverse Polarity Protection

Power input on Pin 1 of the gate driver board input connector features a power management circuit to protect the gate driver from damage by connecting a power source that exceeds the voltage rating of the gate driver. There is a diode and MOSFET in-line with the power input to protect against connecting a power source with positive and negative polarity reversed.

4. Truth Table

Table 3. Truth Table[1]

PWM-HS	PWM-LS	PWM EN	UVLO[2,3]	HS Gate	LS Gate
H	L	H	NP	H	L
L	H	H	NP	L	H
L	L	H	NP	L	L
H	H	X	NP	L	L
X	X	L or Z	NP	L	L
X	X	X	P	L	L

1. H = High, L = Low, X = Irrelevant, Z = High impedance
2. "Not powered" (NP) state is defined as VDDI < VDDIUV. "Powered" (P) state is defined as VDDI > VDDIUV.
3. "Not powered" (NP) state is defined as VDDA/B < VDDA/BUV. "Powered" (P) state is defined as VDDA/B > VDDA/BUV.

5. Gate Driver Interface

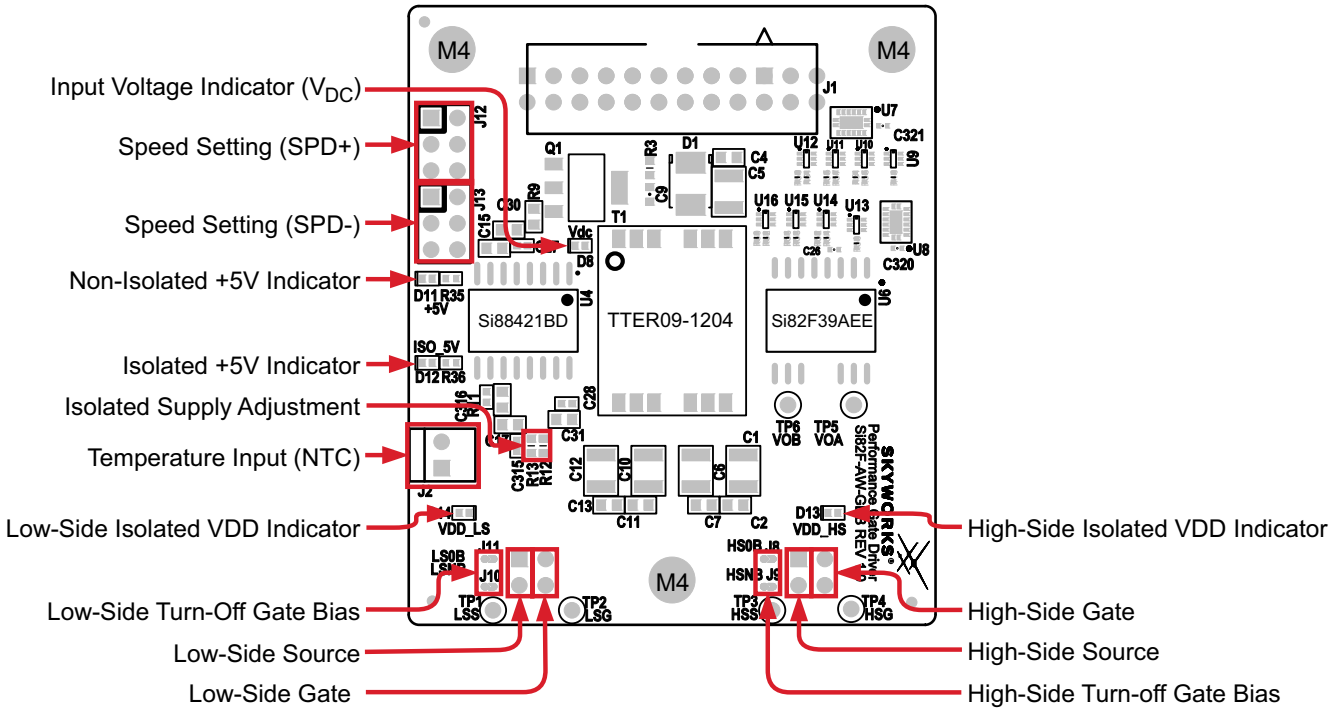

Figure 1. Gate Driver Board (GDB) Top Side

6. Functional Block Diagram

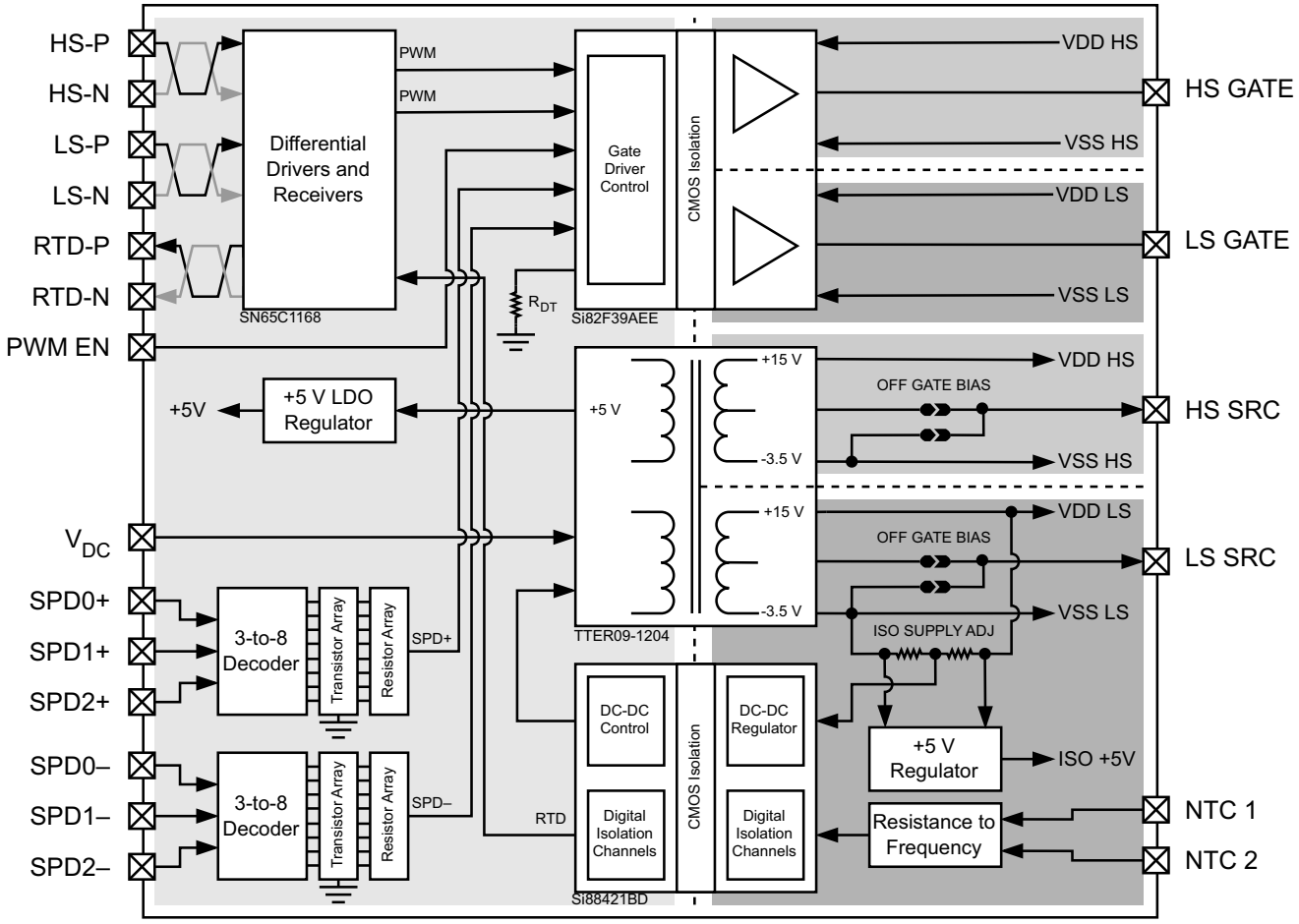

Figure 2. GDB Functional Block Diagram

7. Temperature Feedback

Many power modules use a thermistor to provide temperature feedback of the power switching devices. If a thermistor is provided on the module, it can be connected to the driver board. The resistance of that sensor is converted to a 50% duty cycle square wave with a frequency that varies inversely with the resistance.

The resistance-to-frequency relationship is displayed in Table 4 below. The resistance measurement circuit is located on the low-side gate drive channel, and a digital isolator is used to transmit the frequency-encoded signal back to the primary side of the driver. For this reason, the temperature signal does not need any additional isolation and can be included in the same cable as the rest of the gate driver signals. The temperature reported by the sensor may differ from the junction temperature of the transistors used in the module.

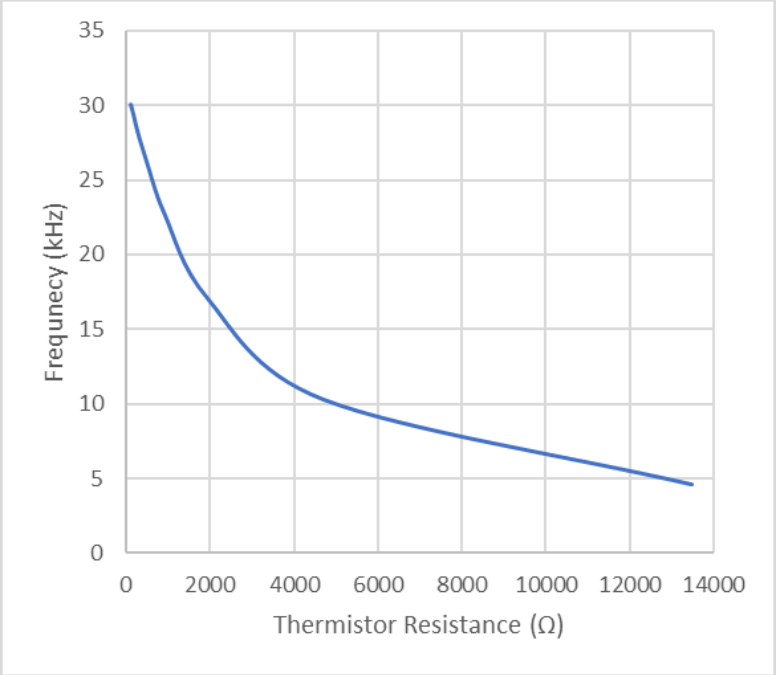

Figure 3. Temperature Sensor Resistance vs. Frequency

Table 4. Thermistor Resistance vs. Frequency Output

Thermistor Resistance (Ω)	Frequency Output (kHz)
13491	4.6
4700	10.3
1928	17.1
898	22.8
464	26.4
260	28.3
156	29.5
99	30.1

8. Connector Information

8.1. Input Connector Information

- 16-position header, 0.100” (2.54 mm) pitch, through-hole, gold (SBH11-PBPC-D08-ST-BK)

8.2. Suggested Mating Parts

- 16-position rectangular header, IDC, gold, 28 AWG (SFH210-PPPC-D08-ID-BK)
- 16-position header, 0.100” (2.54 mm) pitch, through-hole, gold (SFH11-PBPC-D08-RA-BK)
- 16-position header, 0.100” (2.54 mm) pitch, through-hole, right-angle, gold (SFH11-PBPC-D08-RA-BK)

8.3. Output Connector Information

- Four-position header, 0.100" (2.54 mm) pitch, through-hole, gold (Samtec® ESQ-102-33-L-D)

9. User Configurable Options

9.1. Dead Time

Dead time (t_{DT}) is a user-programmable delay between the falling edge of the gate drive signal on one channel and the rising edge of the gate drive signal on the other channel. The value of this delay is programmable through the selection of a dead time resistor (R_{DT}) on the Si82Fx driver. In this application, R_{DT} is R29. The allowed range of R_{DT} is 10 kΩ to 110 kΩ. This provides a range of t_{DT} (typ.) between 20 ns and 200 ns. The relationship between t_{DT} and R_{DT} is described by Equation 1.

$$t_{DT} = 1.73 \times R_{DT} + 5.74$$

Equation 1. Dead Time Calculation

where t_{DT} is in ns and R_{DT} is in kΩ. To change t_{DT} on the GDB, the user would remove R29 and replace it with their calculated resistance value. The standard value of R29 provided with the GDB is 100 kΩ. For additional information about dead time, refer to the Si82Fx Data Sheet.

9.2. Speed Settings and SelVCD™

The Si82Fx utilizes Skyworks SelVCD™ output drive technology. The SelVCD output drive acts as a current source that allows dynamic adjustment of the gate drive strength and the removal of gate drive resistors.

The Si82Fx has eight output drive strength levels for both turn-on and turn-off, controlled by input speed settings pins SPD+ and SPD–, respectively.

The GDB uses three jumpers for each pin that functions as a “3 to 8” decoder for selecting the SPD settings. The jumpers act to pull a given input to ground, and a pull-up resistor pulls the input high when no jumper is present. Thus, having all three jumpers connected results in SPD = 0, while having all three disconnected results in SPD = 7.

For the configured 18 V supply, the highest input setting (SPD = 7) has a typical output drive strength of 4 A, while the lowest input setting (SPD = 0) has a typical output drive strength of 350 mA.

More information about SelVCD and the Si82Fx output current can be found in the Si82Fx Data Sheet.

9.3. Negative Gate Bias

The default configuration of this driver board provides a gate drive signal that swings from +15 V to –3.5 V with respect to the source pin connection.

The user can change this configuration using solder bump jumpers J8 and J9 for the high side and J10 and J11 for the low side. These solder bumps are labeled Turn-Off Gate Bias in Figure 1. By removing solder on J9 and adding solder to J8 for the high side—and also removing solder on J10 and adding solder to J11 for the low side, the output of the driver board swings from +18.5 V to 0 V with respect to the source pin. To reduce the “On” state voltage in this configuration, the user must adjust the output of the isolated power supply converter as described in the next section.

9.4. Isolated Driver Power Supply Voltage

The Si82Fx GDB uses a dc-dc flyback converter integrated into the Si88421 digital isolator. By measuring the output voltage of the low-side secondary winding, the converter regulates both the high-side and low-side windings. The default configuration provides a driver power supply that is regulated to roughly 18.5 V.

The ratio of the transformer windings causes the source pin of each channel to be biased 3.5 V above the converter reference. Thus, the gate sees a voltage swing from +15 V to –3.5 V when measured with respect to the source pin. As mentioned in the previous section, the board can be configured to eliminate the negative bias for the gate voltage by connecting the source pins directly to the converter reference.

However, this causes the gate voltage to swing to +18.5 V with respect to the source pin.

To adjust the output voltage, the user can modify the voltage feedback resistors (R12 and R13, labeled Isolated Supply Feedback Resistors in Figure 1).

The converter expects the feedback divider to provide a sense voltage of 1.05 V on Pin 13 of the Si88421 (VSNS). The output voltage can be approximated using Equation 2.

$$V_{OUT} = \frac{R12 + R13}{R13} \times V_{SNS}$$

Equation 2. Output Voltage Regulation Equation

The standard values of the GDB are R12 = 145 kΩ and R13 = 8.66 kΩ. Using Equation 2, by replacing R13 with a 10.9 kΩ resistor, the converter provides a V_{OUT} of about 15 V. More information about the Si88x2x can be found in the Si88x2x data sheet.

10. Supporting Links and Tools

- Si82Fx Isolated Gate Driver with SelVCD™, Miller Clamp, and Low Channel-to-Channel Skew
- Si88x2x Dual Digital Isolators with DC-DC Converter
- UG542: Si82Fx Gate Driver Board Reference Design
- AN892: Design Guide for Isolated DC-DC Using the Si882xx/883xx
- AN901: Design Guide for Isolated DC-DC Using the Si884xx, Si886xx, or Si8282/84
- AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks Isolators
- AN1167: Safety Considerations for Skyworks Series Capacitive Isolators
- Wolfspeed® Product Links:
  - KIT-CRD-CIL12N-FMA Evaluation Tool
  - CAB011M12FM3, 1200 V, Half-Bridge, SiC Power Module
  - CGD12HB00D Differential Transceiver Daughter Board
  - Wolfspeed SpeedVal™ Kit Modular Evaluation Platform
- PRD-07968: Wolfspeed WolfPACK™ Dynamic Performance App Note
- PRD-08333 Wolfspeed Module CIL Evaluation Kits User Guide

11. Dimensions

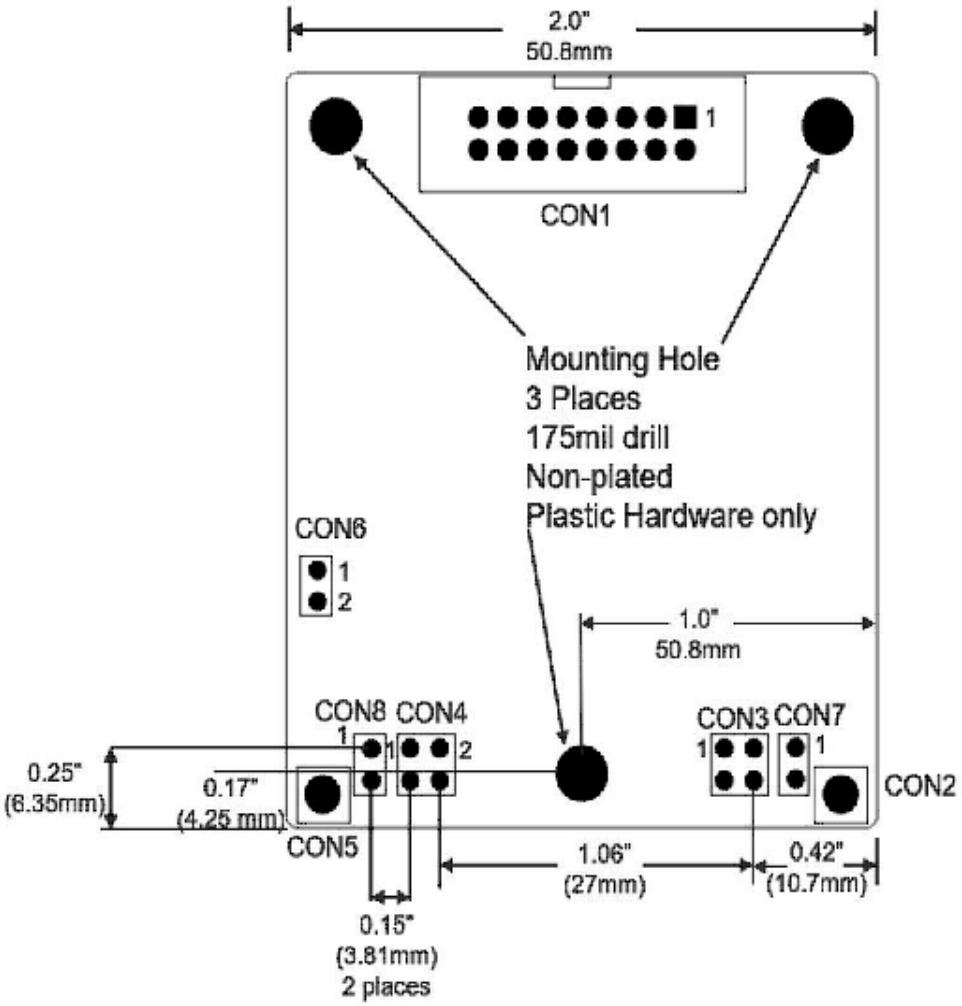

Figure 4. Si82Fx Gate Driver Board (GDB) Dimensions

12. Ordering Information

Part Number	Description	Evaluation Board Part Number
Si82F-ACWA-KIT	Si82Fx Gate Driver Board (GDB)	Si82F-ACWA-GDB