USER GUIDE

UG539: SKY5351x Evaluation Board User Guide

Features

- Ultra-low additive jitter for 10-output clocks
- Powered from universal serial bus (USB), wall-wart, or external supply
- Designed for quick setup and ease-of-use
- Included calibration traces match the input to the device under test (DUT) and output from DUT, trace length, and layout geometry to simplify propagation delay measurements
- Precision 0.1 Ω resistors to simplify supply current measurements
- GPI-configured DUT via eight-position switch (SKY53511-A-EVB)
- I^2C configured DUT (SKY53512-A-EVB and SKY53513-A-EVB)
- Supports the following output formats:
  - SKY53511-A-EVB: LVCMOS
  - SKY53512-A-EVB: HCSL
  - SKY53513-A-EVB: LVDS, LVPECL, LVCMOS
- Plug and play—no software setup is required for SKY53511-A-EVB
- XTAL/external clock input option
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Description

The SKY5351x customer evaluation board (CEVB) can be used to evaluate the SKY535xx family of ultra-low additive jitter clock buffers. This product family consists of GPIO controlled devices (SKY535x0/x1) as well as I^2C controlled devices (SKY535x2/x3). Skyworks offers four orderable CEVB part numbers (one from each of the four SKY535xx product families) to evaluate the 10-output device. Note that the SKY53510 (SKY53510-EVB) is not included in this User Guide; please refer to UG523: SKY53510 Customer Evaluation Board User Guide.

This document is intended to familiarize the user with configuring switches and jumpers (SKY53511-A-EVB), internal registers (SKY53512-A-EVB, SKY53513-A-EVB), and various board features as well as general board setup for measuring supply currents, signal integrity, propagation delay, output-to-output skew, additive jitter, and input multiplexer (MUX) isolation.
Also included are Skyworks web site links to board schematics and bill of materials (BOM).

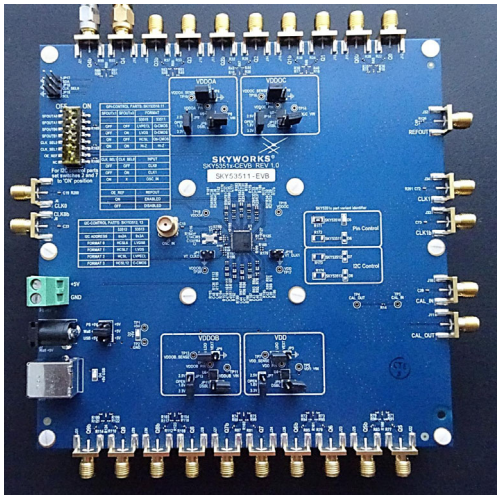

Figure 1. SKY5351x Evaluation Board

1. Functional Block Diagram

Figure 2 below is a functional block diagram of the SKY5351x CEVB while Figure 3 and Figure 4 show functional block diagrams of the DUT. This evaluation board can be powered by connecting to your PC's USB connector or by an external +5 V dc power source (either wall wart or lab supply). Note that V_{DD} should always be selected to be equal to or higher than the highest V_{DDOx} supply voltage.

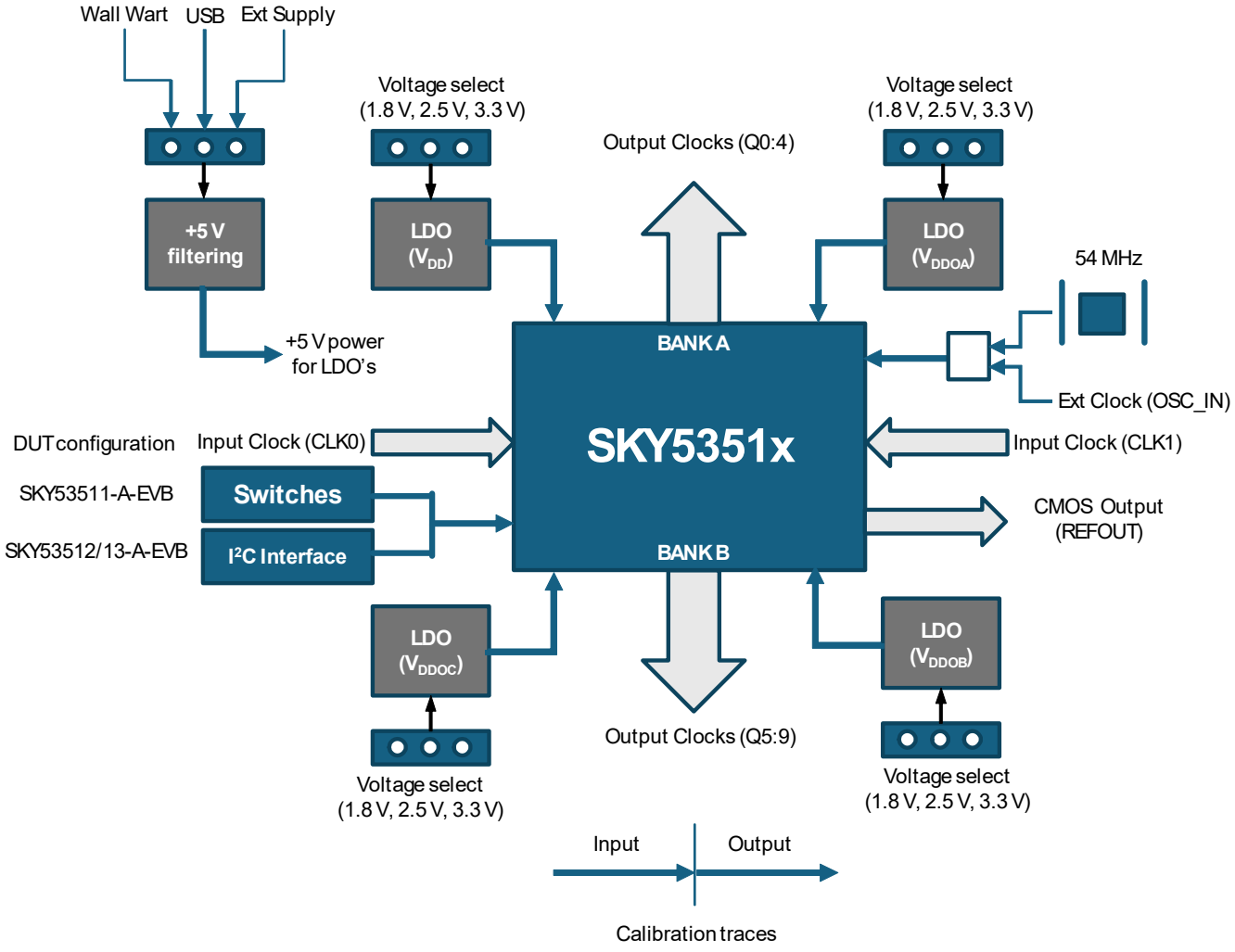

Figure 2. SKY5351x CEVB Functional Block Diagram

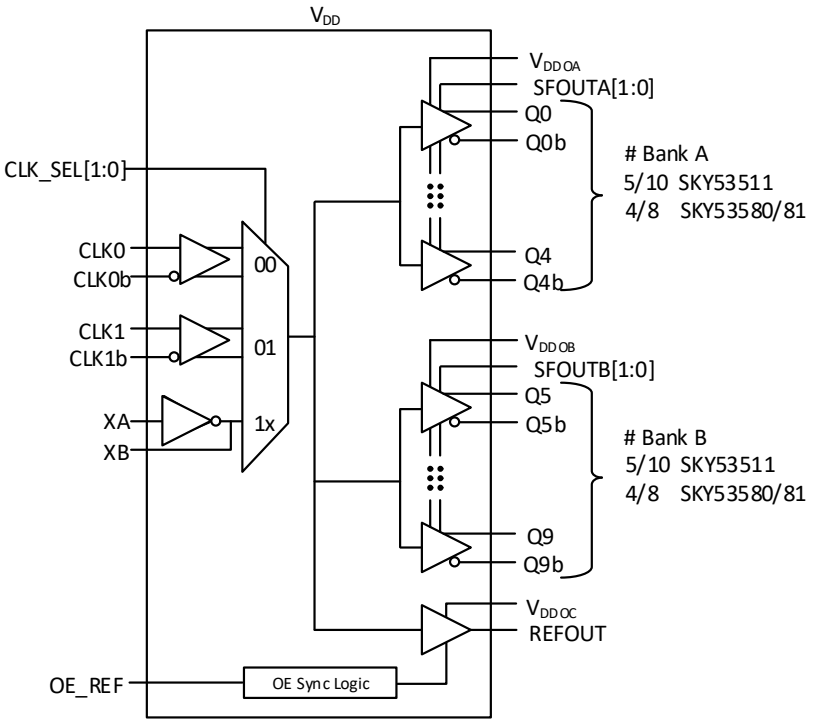

Figure 3. SKY53511 Functional Block Diagram

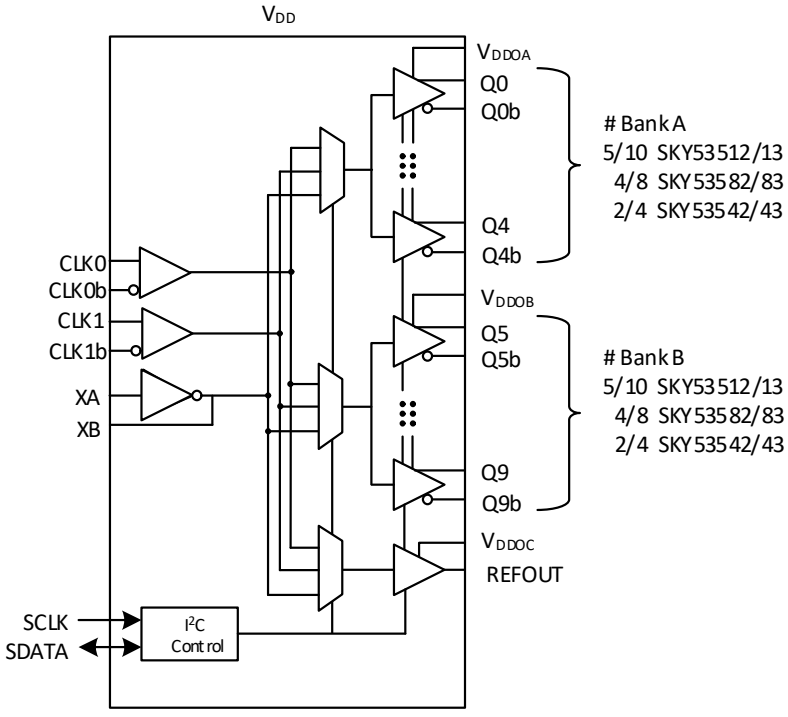

Figure 4. SKY53512/13 Functional Block Diagram

2. Quick Start Guide

Important board jumpers, switches, LEDs, and their locations are shown in Figure 5 below.

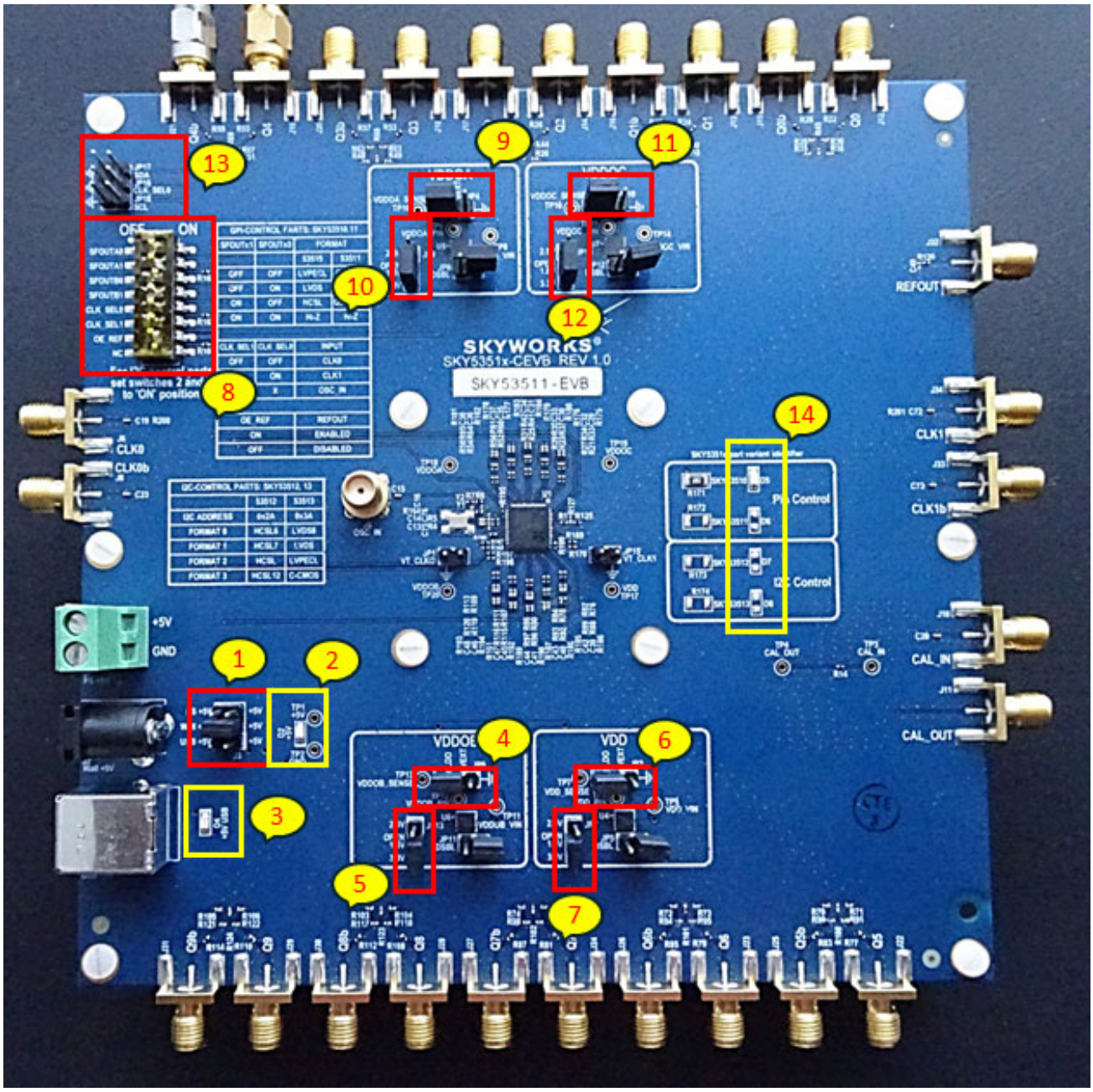

Figure 5. Jumpers, Switches, and LED Locations

The board is shipped with the jumpers in their default configuration: +5 V from USB, LDO power, and +3.3 V for each supply: V_{DD}, V_{DDOA}, V_{DDOB}, and V_{DDOC}. However, it is advised to double-check this. Refer to Table 1 below for a description of each jumper, switch, and LED. Note that Pin 1 of each jumper has a bold outline on the silkscreen.

Table 1. Jumpers, Switches, LED Descriptions and Default Configuration

Callout	Reference Description	Schematic Page	Description	Default Configuration	Options
1	J3	3	External +5 select	USB +5 V	Wall Wart (Wall +5 V) Power Supply (PS +5 V)
2	D2	3	LED green; should illuminate when +5 V source is applied and J3 jumper installed		
3	D4	3	LED blue; should illuminate when USB source is applied		
4	JP9	9	V_{DDOB} source select	LDO (pins 2,3 jumpered)	VEXT: supply on pin 2, Ground on pin 1
5	JP13	9	V_{DDOB} voltage select	+3.3 V (pins 2,3 jumpered)	+2.5 V (pins 1,2 jumpered) +1.8 V (jumper removed)
6	JP3	9	v_{DD} source select	LDO (pins 2,3 jumpered)	VEXT: supply on pin 2, Ground on pin 1
7	JP7	9	V_{DD} voltage select	+3.3 V (pins 2,3 jumpered)	+2.5 V (pins 1,2 jumpered) +1.8 V (jumper removed)
8	SW1	8	DUT configuration select	User defined - refer to table on silkscreen for switch settings	
9	JP4	9	V_{DDOA} source select	LDO (pins 2,3 jumpered)	VEXT: supply on pin 2, Ground on pin 1
10	JP8	9	V_{DDOA} voltage select	+3.3 V (pins 2,3 jumpered)	+2.5 V (pins 1, 2 jumpered) +1.8 V (jumper removed)
11	JP10	9	V_{DDOC} source select	LDO (pins 2,3 jumpered)	VEXT: supply on pin 2, Ground on pin 1
12	JP14	9	V_{DDOC} voltage select	+3.3 V (pins 2,3 jumpered)	+2.5 V (pins 1,2 jumpered) +1.8 V (jumper removed)
13	JP17, JP18	8	I^2C communications access		
14	D5:D8	8	Part variant identifier LEDs	OPN-dependent	
None	JP1, JP5, JP6, JP11, JP12, JP15, JP16, JP17, JP18	5, 8, 9	Various	No jumper installed	JP5, JP6, JP11, JP12 - disables the LDO when installed; JP16, JP17, JP18 - used for measuring startup, enable, and disable times JP1, JP15 - external input bias voltage

The following tasks must be performed before taking measurements:

1. Apply a +5 V source and position the J3 jumper in the corresponding position.
2. Decide whether to source each supply voltage via on-board LDO or externally (callouts 4, 6, 9, and 11).
3. Decide what voltage is desired for each supply (callouts 5, 7, 10, and 12).
4. For SKY53511-A-EVB, configure switch SW1 (callout 8) for Bank A, B output format, Input clock select, and REFOUT enable.
5. For SKY53512/13-A-EVB, set switch SW1 (callout 8) positions 2 and 7 to "ON", connect an I^2C host (e.g., Corelis I^2C Bus Analyzer, Aardvark™ I^2C/SPI Host Adapter, ClockBuilder® Pro (CBPro) Field Programmer) to JP17-pin2 (SDA), JP18-pin2 (SCL) and JP16-pin 1 (ground) and configure the inputs/outputs via I^2C. Note that the voltage used by the I^2C host needs to match the voltage on VDD. "Appendix—Setting up I2C Communication with the DUT Using the Field Programmer Dongle" describes the steps used to set up the CBPro Field Programmer to communicate with the DUT.
6. Apply a differential input to either CLK0 or CLK1 (note, on the SKY53511-A-EVB, CLK0 should be a single-ended LVCMOS signal, but CLK1 is still differential), or choose the on-board XTAL (54 MHz).
7. Connect an output to your test equipment and start taking measurements.

3. Signal Path and Configuration Settings (SW1, I²C)

The SKY5351x supports both single-ended and differential input clocks (CLK0, CLK1) along with an external fundamental-mode crystal (the CEVB is populated with a 54 MHz crystal), which can be bypassed via minor board modification to allow the input to be driven by an external single-ended clock (OSC_IN). For SKY53511-A-EVB, the selection of the input clock is pin-controlled via switch SW1 according to Table 2. For SKY53512/13-A-EVB, the selection of the input clock is I²C-controlled according to Table 3.

Table 2. Configuration of Switch SW1 for Input Clock Selection (SKY53511-A-EVB Only)

CLK_SEL1 SW1 Pos. 6	CLK_SEL0 SW1 Pos. 5	Input
Off	Off	CLK0
Off	On	CLK1
On	X	XTAL/OSC_IN

Table 3. Internal Register Configuration for Input Clock Selection (SKY53512/13-A-EVB Only)

Bank A REG ADDR: 0x013F[1:0]	Bank B REG ADDR: 0x013F[4:3]	REFOUT REG ADDR; 0x013F[7:6]	Selected Input
00[1]	00[1]	00[1]	CLK0[1]
01	01	01	CLK1
10	10	10	XA/XB
11	11	11	XA/XB

1. Default setting.

Refer to 6. “Crystal Oscillator Interface” for instructions on how to modify the board to accept an external single-ended clock.

The board provides access to ten of the SKY5351x device's differential outputs. Note that these outputs are single-ended LVCMOS on the SKY53511-A-EVB. There are five differential outputs assigned to Bank A (Q0:Q4) and five assigned to Bank B (Q5:Q9). Note that on the SKY53511, since the outputs are single-ended, there are 10 outputs on each bank. The five differential outputs on each bank can be configured for the following formats: LVCMOS or Hi-Z on the SKY53511-A-EVB; HCSL (multiple swings) on the SKY53512-A-EVB; LVDS (multiple swings), LVPECL, or LVCMOS on the SKY53513-A-EVB. On the SKY53511-A-EVB, the selection of output clock format is pin-controlled via switch SW1 as shown in Table 4. On the SKY53512/13-A-EVB, the selection of the output clock format is I²C-controlled as shown in Table 5. Table 6 provides a description of the naming convention used with the SKY535xx output formats.

Table 4. Configuration of Switch SW1 for Output Clock Format Selection (SKY53511 Only)

SFOUTA1 SW1 Pos. 2	SFOUTA0 SW1 Pos. 1	SFOUTB1 SW1 Pos. 4	SFOUTB0 SW1 Pos. 3	SKY53511 Format
Bank A		Bank B		
OFF	OFF	OFF	OFF	Q-CMOS
OFF	ON	OFF	ON	D-CMOS
ON	OFF	ON	OFF	Qb-CMOS
ON	ON	ON	ON	Hi-Z

Table 5. Configuration of Internal Registers for Output Clock Format Selection (SKY53512/13 Only)

BANK A REG ADDR: 0x013B[7:6]	BANK B REG ADDR: 0x013C[7:6]	Format	
		SKY53512 I^2C ADDR: 0x02A	SKY53513 I^2C ADDR: 0x03A
00[1]	00[1]	HCSL6[1]	LVDS8[1]
01	01	HCSL7	LVDS
10	10	HCSL	LVPECL
11	11	HCSL12	C-CMOS

1. Default setting.

Table 6. Description of Output Format Name Convention Used on SKY535xx

Output Format	Description
Q-CMOS	Non-inverted LVCMOS (Qn/Hi-Z)
D-CMOS	Dual in-phase LVCMOS (Qn/Qnb)
Qb-CMOS	Non-inverted LVCMOS (Hi-Z/Qnb)
C-CMOS	Complementary LVCMOS
HCSL6	600 mV swing
HCSL7	700 mV swing
HCSL	800 mV swing
HCSL12	1200 mV swing
LVDS8	800 mV LVDS

An additional LVCMOS output is assigned to REFOUT which can be enabled or disabled via pin-control of switch SW1 for the SKY53511-A-EVB according to Table 7 or via I^2C-control according to Table 8 for the SKY53512/13-A-EVB.

Table 7. Configuration of Switch SW1 for Enabling REFOUT (SKY53511 Only)

OE_REF SW1 Pos 7	REFOUT
ON	Enabled
OFF	Disabled

Table 8. Configuration of Internal Registers to Control REFOUT (SKY53512/13 Only)

EN_REF, REF_PWR REG ADDR: 0x013E[1:0]	REFOUT State[1]
00	Powered down
01	Powered up/disabled
10	Powered down
11	Powered up/enabled

1. To enable REFOUT, it should first be powered up (0x013E[1:0] = 01) and then enabled (0x013E[1:0] = 11).

4. External Power and Voltage Supply Circuits

The power supply section of the CEVB provides flexibility to apply +5 V power to the board via three optional sources: (1) USB, (2) wall-wart, (3) lab dc power supply. Figure 6 shows the connectors for these three power sources and the power selection jumper (J3). Refer to Schematic page 3 (see 9. “Schematics and BOM” on page 33 for URL).

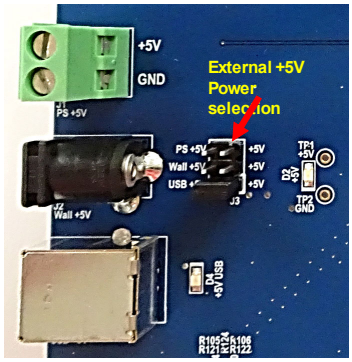

Figure 6. External +5 V Power and Selection Circuit

There are four LDO circuits on-board that take the selected +5 V supply and regulate it to either +3.3 V, +2.5 V, or +1.8 V that sources different circuits of the SKY5351x buffer. The voltage to each of these buffer circuits is jumper controlled independently for V_{DD} (JP7), V_{DDOA} (JP8), V_{DDOB} (JP13), and V_{DDOC} (JP14). Each LDO circuit includes a jumper that when installed, disables the LDO (JP5, JP6, JP11, and JP12 for V_{DD}, V_{DDOA}, V_{DDOB}, and V_{DDOC}, respectively). The LDO can also be bypassed and the buffer circuit sourced externally via jumpers JP3 (V_{DD}), JP4 (V_{DDOA}), JP9 (V_{DDOB}), and JP10 (V_{DDOC}) by applying a dc voltage to jumper pin 2 and ground to jumper pin 1. Figure 7 shows these four LDO circuits. Refer to Schematic page 9 (see 9. “Schematics and BOM” on page 33 for URL).

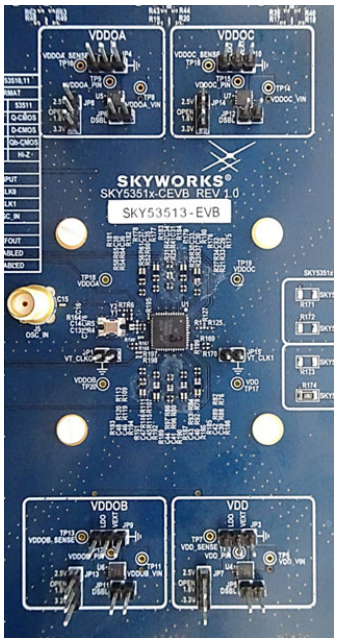

Figure 7. LDO Circuits

5. Clock Inputs

The SMA inputs (CLK0/0b and CLK1/1b) can be configured to accept a differential or single-ended clock. Best phase noise performance is achieved with a low-noise, differential input clock (default configuration for both inputs except for SKY53511-A-EVB which defaults CLK0 as single-ended) with a high input slew rate. Although most applications use ac-coupled, differential inputs and thus not require any board modifications, for other input termination options, refer to Table 9 for component and termination voltage changes.

Table 9. Input Termination Component Map

Input Type	CLK0					CLK1					VT_CLKx JP1, JP15
	C19/R200	C23	R8	R12	C21	C72/R201	C73	R160	R161	C74	
AC-coupled, differential[1]	0.1 µF	0.1µF	49.9 Ω	49.9 Ω	0.1 µF	0.1 µF	0.1 µF	49.9 Ω	49.9 Ω	0.1 µF	N/C
DC-coupled, LVPECL	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0.1 µF	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0.1 µF	VDD-2 V
DC-coupled, LVDS	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0.1 µF	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0.1 µF	N/C
DC-coupled HCSL (source)	0 Ω	0 Ω	Remove	Remove	0.1 µF	0 Ω	0 Ω	Remove	Remove	0.1 µF	N/C
DC-coupled HCSL (end)	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0 Ω	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0 Ω	N/C
DC-coupled LVCMOS[2]	0 Ω	Remove	Remove	0 Ω	0.1 µF	0 Ω	Remove	Remove	0 Ω	0.1 µF	N/C
AC-coupled LVCMOS	0.1 µF	Remove	Remove	0 Ω	0.1 µF	0.1 µF	Remove	Remove	0 Ω	0.1 µF	N/C

1. Default configuration (SKY53512 and 13) SKY53511 for CLK1 only.
2. Default configuration (SKY53511 for CLK0 only).

To apply an input termination voltage (only needed for dc-coupled LVPECL) connect a dc supply to pin 2 of headers JP1 (CLK0) and/or JP15 (CLK1). Figure 8 shows their location.

Two calibration traces are provided to simplify propagation delay and output-to-output skew measurements. The trace connected to the CAL_IN SMA is an exact match in length and trace geometry to the input traces (CLK0/0b, CLK1/1b). The trace connected to the CAL_OUT SMA is an exact match in length and trace geometry to the output traces (Q0/0b:Q9/9b). Details on the recommended methodology for making these measurements is provided in Section 8. Refer to schematic page 5 (see 9. “Schematics and BOM” on page 33 for URL).

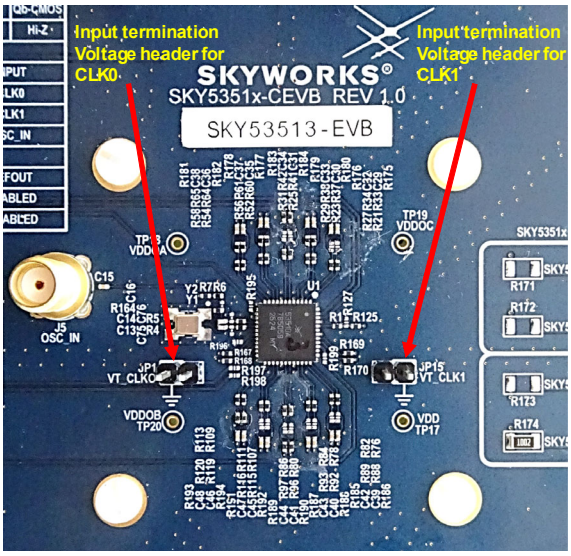

Figure 8. Location of Headers for External Input Termination Voltages

6. Crystal Oscillator Interface

The SKY5351x has an integrated crystal oscillator interface (XA/XB) that supports a fundamental mode crystal ranging from 24 to 54 MHz. If the crystal input is selected (refer to Table 2 for SKY53511-A-EVB or Table 3 for SKY53512/13-A-EVB), the on-board crystal on either footprint Y1 or Y2 starts up, and the oscillator clock can be measured on any enabled output. The board default configuration includes a 3.2 x 2.5 mm 54 MHz crystal on Y1. Alternatively, a 5.0 x 3.2 mm crystal can be populated on Y2 on a merged footprint with Y1.

The crystal shunt caps (C13 = 8 pF and C14 = 6.8 pF) and the series resistor (R4 = 316 Ω) are specifically chosen for optimal performance of the TXC 7M54072001 54 MHz crystal. Note that other crystal vendors or frequencies may require different values of R4.

To configure a single-ended external clock input on OSC_IN (J5), remove the 0 Ω resistor R164 and install a 0.1 µF capacitor at C16. Note that these components share a common pad; therefore, only one can be installed at a time. See Figure 9 below for the location of those components.

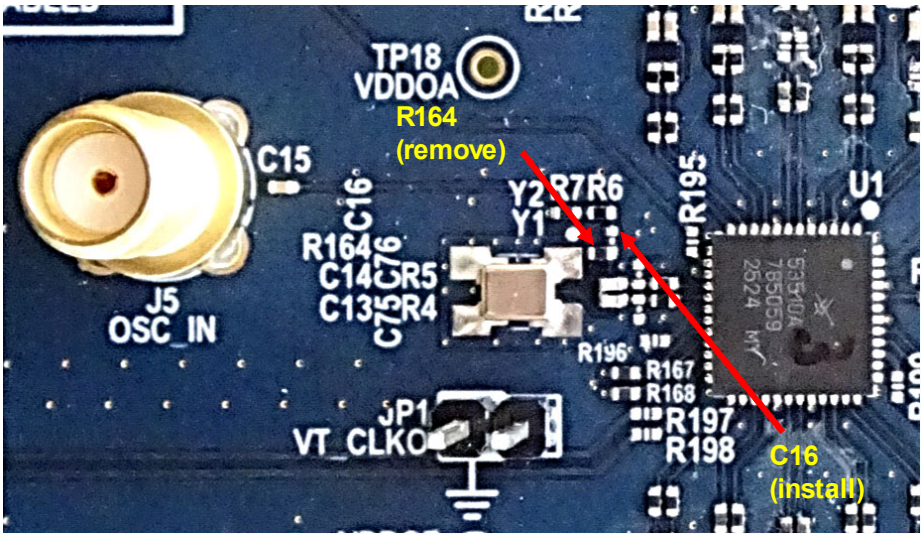

Figure 9. Component Location to Change from the Crystal to a Single-Ended External Clock (OSC_IN) on Input XA

7. Clock Outputs

Since each OPN supports different output formats, each board has different default output terminations. In general, the CEVB was designed to support taking measurements of the most common output terminations via coax cables between the CEVB and either a scope or Phase Noise Analyzer (PNA) with 50 Ω input terminations. This section describes the default configuration of each Orderable Part Number (OPN) (good for measuring phase noise, input mux isolation, duty cycle, amplitude, rise and fall times, propagation delay, and skew), and Table 10 identifies what component modifications would be necessary to configure the output for measuring dc voltage levels (e.g., V_{CM}, V_{OH}, V_{OL}) to compare against data sheet specifications. Note that in Table 10, the components listed (R1:R7) are generic terms shown in red font on schematic pages 6 and 7. Note also that these termination configurations are intended for observing signal quality and making measurements with test equipment terminated with 50 Ω to ground. They are not necessarily the recommended part-to-part interconnect one would use when designing a board using the SKY5351x. Refer to the data sheet for in-system termination recommendations. The following sections describe the default configuration of each of the OPNs.

7.1. SKY53511-A-EVB

By default, Bank A outputs are configured for ac-coupled LVCMOS format and source terminated with an in-line 27 Ω resistor (R7 in Table 10). These outputs go to SMA connectors labeled Q0/0b:Q4/4b. Bank B outputs are configured for dc-coupled LVCMOS format and source-terminated with an in-line 27 Ω resistor (R7 in Table 10). These outputs go to SMA connectors labeled Q5/5b:Q9/9b. REFOUT is an LVCMOS output and is dc-coupled and source-terminated with an in-line 27 Ω resistor to its SMA connector.

7.2. SKY53512-A-EVB

By default, both Bank A and Bank B outputs are configured for dc-coupled, end-terminated HCSL format. All outputs have no pull-up or pull-down resistors and have 0 Ω resistance to SMA connectors labeled Q0/0b:Q9/9b. The test equipment provides the 50 Ω to ground end termination needed for this format. REFOUT is an LVCMOS output and is dc-coupled and source terminated with an in-line 27 Ω resistor to its SMA connector.

7.3. SKY53513-A-EVB

By default, both Bank A and Bank B outputs are configured for ac-coupled LVDS format. All outputs have no pull-up or pull-down resistors and have 0 Ω resistance to SMA connectors labeled Q0/0b:Q9/9b. The test equipment provides the 50 Ω to ground end termination needed for this format. Note that the proper end termination for LVDS is differential 100 Ω, so there is a small dc current draw that causes a small attenuation of the amplitude when this configuration is used. Table 10 provides the component changes necessary to measure the signal integrity of these outputs using a 100 Ω differential termination and a 20:1 probe. REFOUT is an LVCMOS output and is dc-coupled and source-terminated with an in-line 27 Ω resistor to its SMA connector.

Table 10. Output Termination Configuration for All Formats, Voltages, Couplings, and Terminations

Format	Measurement	R1	R2	R3	R4	R5	R6	R7
3.3 V AC-LVPECL	Phase noise, Signal integrity	130 Ω	0.1 µF	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
2.5 V AC-LVPECL	Phase noise, Signal integrity	91 Ω	0.1 µF	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
3.3 V DC-LVPECL	Signal integrity	NOPOP	0 Ω	127 Ω	82 Ω	953 Ω[1]	0 Ω	0 Ω
2.5 V DC-LVPECL	Signal integrity	NOPOP	0 Ω	250 Ω	62 Ω	953 Ω[1]	0 Ω	0 Ω
AC-LVDS AC-HCSL (end-term)[2]	Phase noise, Signal integrity	NOPOP	0.1 µF	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
AC-LVDS	Signal integrity	NOPOP	0.1 µF	NOPOP	50 Ω	953 Ω[1]	0.1 µF	0 Ω
DC-LVDS	Signal integrity	NOPOP	0 Ω	NOPOP	50 Ω	953 Ω[1]	0.1 µF	0 Ω
DC-HCSL (SRC-term)	Signal integrity	50 Ω	0 Ω	NOPOP	NOPOP	0 Ω	NOPOP	33 Ω
DC-HCSL (end-term)[3]	Phase noise, Signal integrity	NOPOP	0 Ω	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
AC-LVCMOS[4]	Phase noise	NOPOP	0.1 µF	NOPOP	NOPOP	0 Ω	NOPOP	27 Ω
DC-LVCMOS[5]	Signal integrity	NOPOP	0 Ω	NOPOP	NOPOP	0 Ω[6]	NOPOP	27 Ω

1. This value in conjunction with 50 Ω internal scope termination creates a 20:1 probe.
2. Default configuration banks A and B (SKY53513).
3. Default configuration banks A and B (SKY53512.)
4. Default configuration bank A (SKY53511).
5. Default configuration bank B (SKY53511).
6. 0 Ω can be used if scope has Hi-Z input option; otherwise, use the 20:1 probe (953 Ω).

8. Making Measurements

There are many ways various measurements can be made; this section describes recommendations on how to take advantage of some of the built-in features of the CEVB and how to configure the test setup for optimal measurements.

8.1. Supply Current

The SKY5351x Evaluation Board includes a 0.1 Ω precision in-line resistor on each voltage supply so measuring the supply current is simply a matter of measuring the voltage drop across this resistor for the given supply and applying the following equation to determine the current: $I_{DD(Ox)} = 10 \times V_{measured}$. Figure 10 and Figure 11 show the test points where each supply current can be measured.

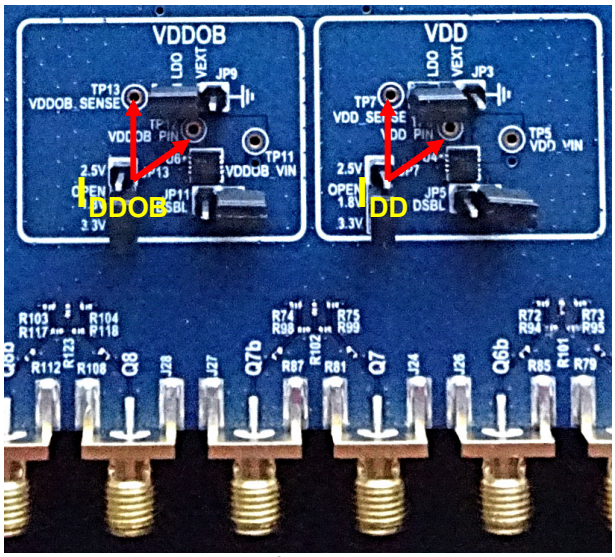

Figure 10. Test Points for Measuring I_{DD} and I_{DDOB}

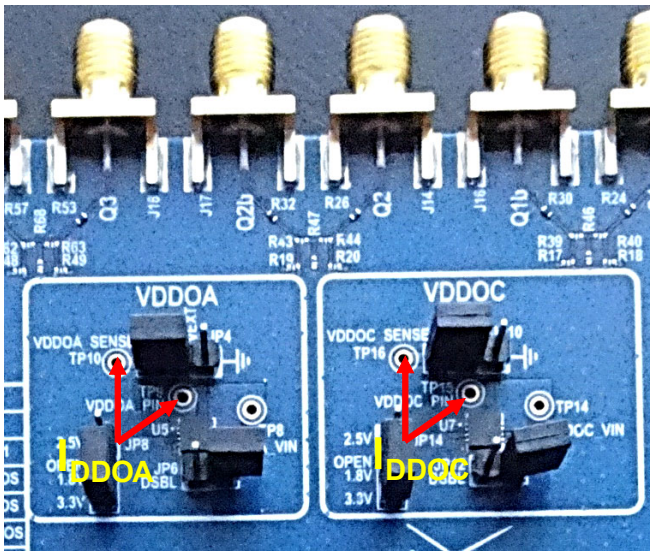

Figure 11. Test Points for Measuring I_{DDOA} and I_{DDOC}

8.2. Propagation Delay and Skew

Figure 12 shows a block diagram for measuring propagation delay and skew.

The SKY5351x evaluation board includes calibration traces (CAL_IN, CAL_OUT), which match the length and geometry of the SMA-to-DUT (input) and DUT-to-SMA (output) traces. The user can take advantage of these traces to simplify measuring the propagation delay and output-to-output skew.

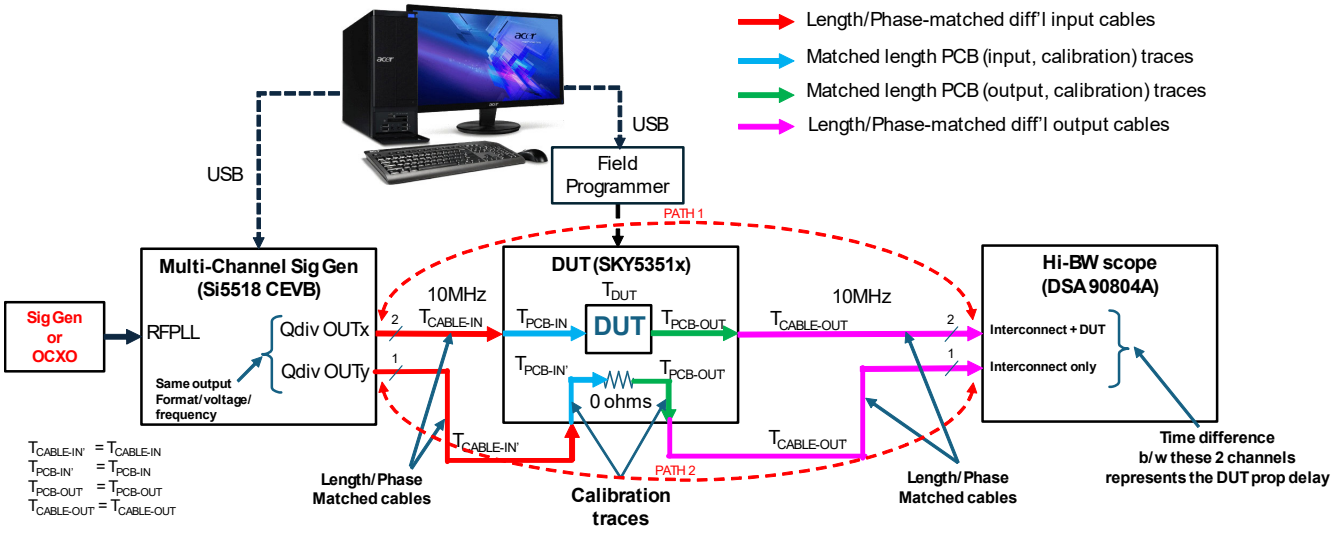

Figure 12. Block Diagram of Setup Used to Measure Propagation Delay and Skew

To make this measurement, a signal generator with multiple matched outputs can be used or one of Skyworks Clock Generators, Jitter Attenuators, or Network Synthesizers can be used as they have multiple matched outputs. For the measurements in this Guide, the Si5518 CEVB was used which provides a matched phase relationship on two Q divider LVDS outputs. Using two sets of length/phase matched coax cables, connect one differential pair to CLK0 (CABLE-IN in Figure 12) and a single cable (this can be another differential coax cable using only one leg of the differential pair) to CAL_IN (CABLE-IN' in Figure 12). Terminate the unused LVDS output leg (on Si5518 CEVB) with 50 Ω-to-ground. Similarly, using two sets of length/phase matched differential coax cables, connect one pair from the Qx and Qxb output (on the SKY5351x CEVB) to two scope channels (CABLE-OUT in Figure 12) and the other cable from CAL_OUT (on the SKY5351x CEVB) to a third scope channel (CABLE-OUT' in Figure 12) again, only one leg of the differential cable pair is connected. Trigger the scope on this third channel. The interconnect component of delay of Path 1 should now be equally matched on Path 2 (assuming the phase difference between the cables and calibration traces is negligible); so, measuring the time delta between the crossing point of the differential pair ("Output" in the figures below) and the midpoint of the transition edge of the calibration trace ("Input" in the figures below) yields the input to output propagation delay of the DUT. Figures 13 through 16 show a sample propagation delay for an LVPECL, LVDS, HCSL, and LVCMOS output, respectively.

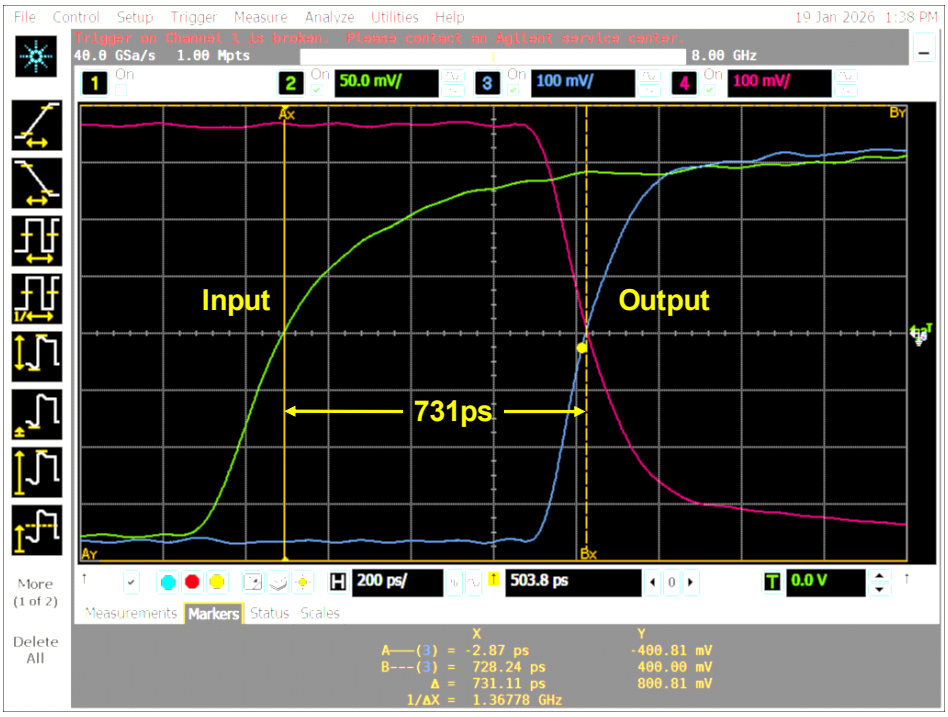

Figure 13. Sample Propagation Delay for LVPECL Output

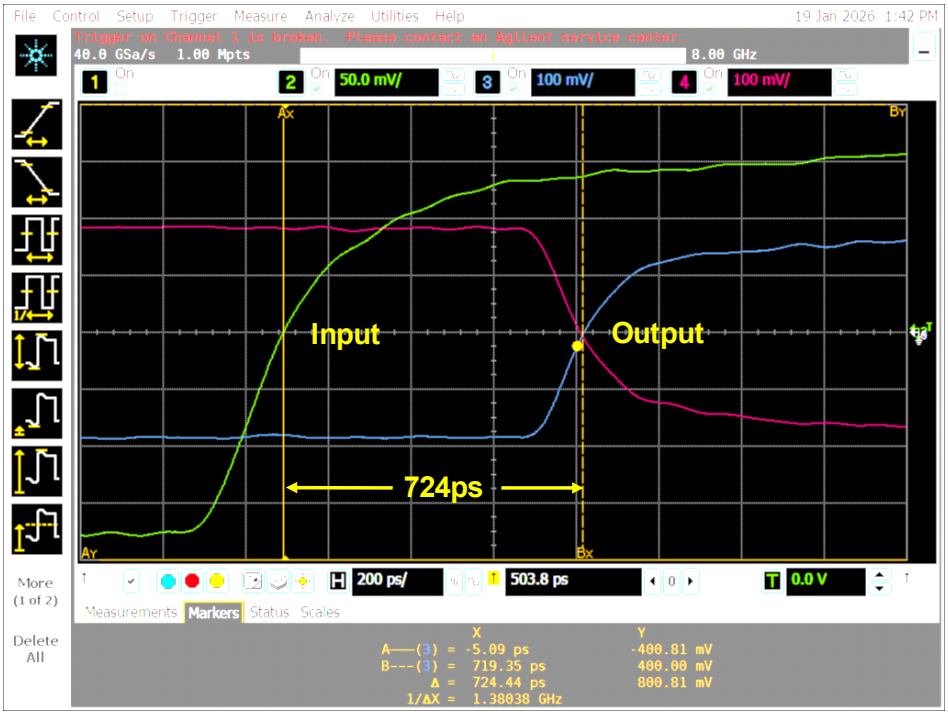

Figure 14. Sample Propagation Delay for LVDS Output

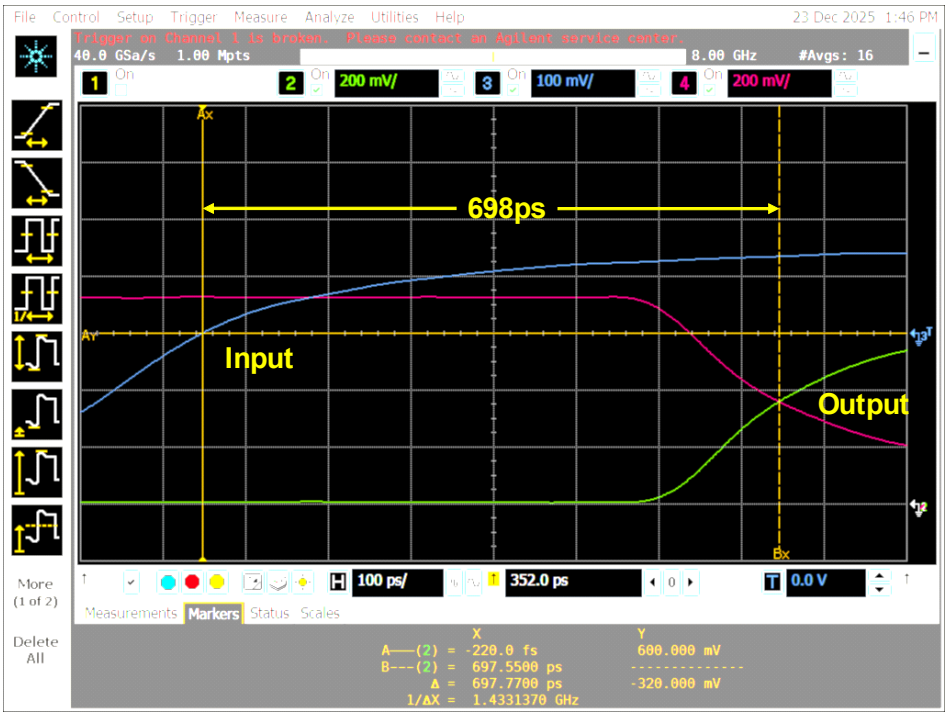

Figure 15. Sample Propagation Delay for HCSL Output

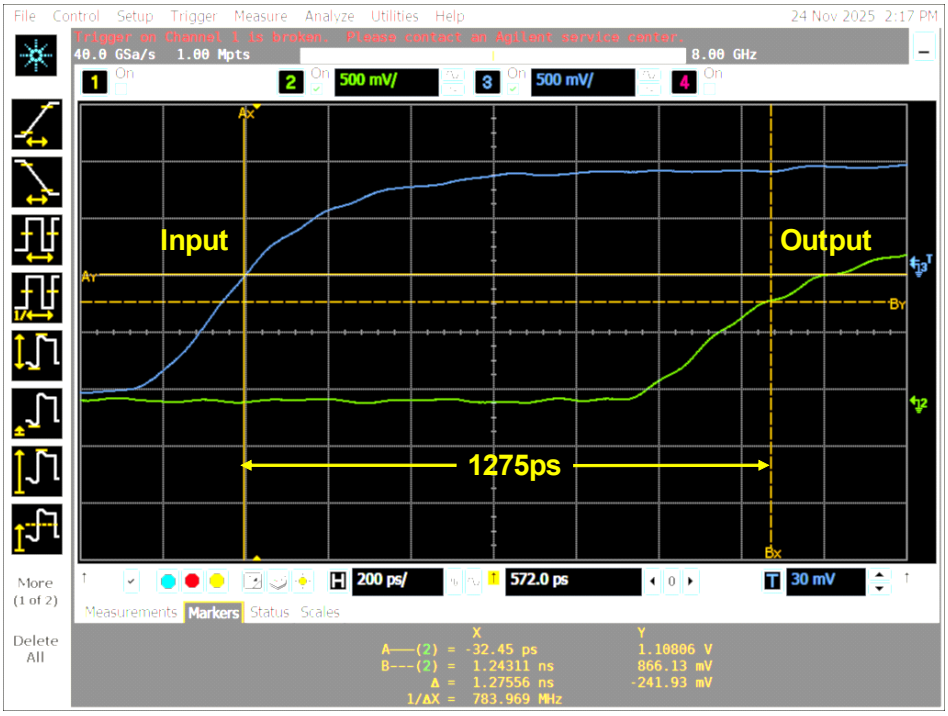

Figure 16. Sample Propagation Delay for LVCMOS Output

Next, to measure output-to-output skew, use a scope function that subtracts the two differential scope inputs on Path 1 and expand the vertical scale of the scope to around 5 mV/division to ensure a very sharp rising edge of this differential voltage. Turn on averaging to minimize jitter, and, using a scope cursor, place it on the rising edge of the Path 1 function channel. Next, move the differential cable to the next Qx/Qxb output and again place a cursor on the rising edge of the scope function channel. Continue in this way for all ten outputs, keeping one cursor on the earliest rising edge and one on the latest rising edge (make sure that both banks use the same output termination configuration (as outlined in Table 10) and both use the same output format (SFOUTA[1:0] = SFOUTB[1:0]). The worst-case output-to-output skew is then the time delta between the earliest cursor placement and the latest cursor placement. Figures 16 and 17 show a sample output-to-output skew for an LVPECL and LVDS output, respectively.

Figure 17. Sample Output-to-Output Skew for LVPECL Output

Figure 18. Sample Output-to-Output Skew for LVDS Output

8.3. Signal Integrity

This section includes example scope plots of signal integrity measurements (e.g., duty cycle, rise and fall time, and peak-to-peak amplitude) of four output formats (ac-coupled 3.3 V LVPECL, LVDS, HCSL, and LVCMOS) at two frequencies (100 MHz and 500 MHz) for the differential formats and 200 MHz for LVCMOS using the default board configuration (refer to Table 10). Other available formats (LVDS8, HCSL6, HCSL7, and HCSL12) can also be easily measured without board modification through register settings on the SKY53512-A-EVB and SKY53513-A-EVB.

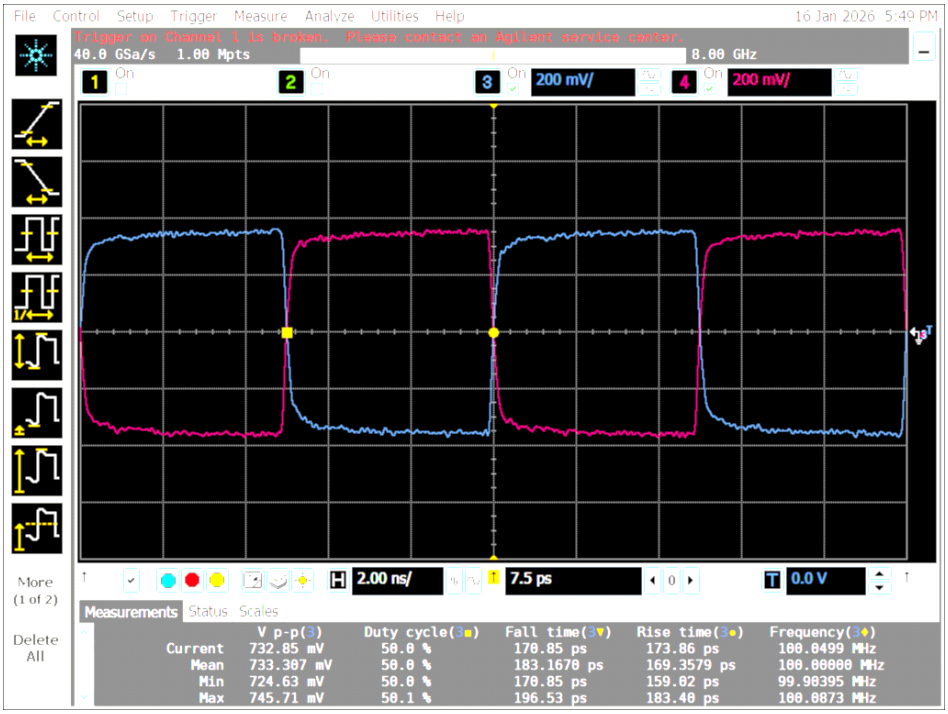

Figure 19. Sample Signal Integrity for LVPECL @100 MHz

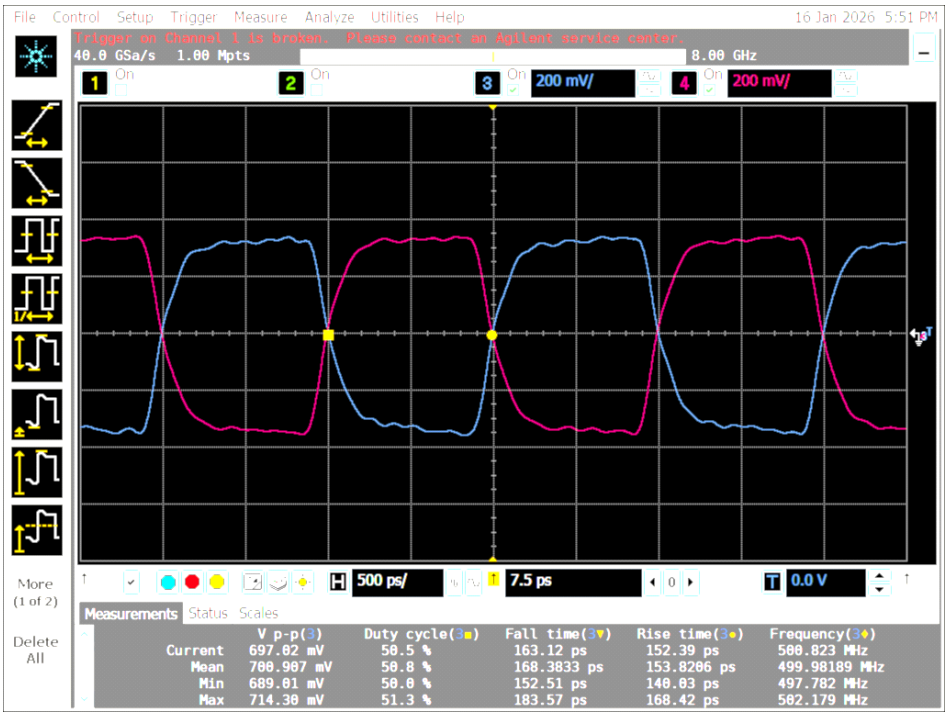

Figure 20. Sample Signal Integrity for LVPECL @500 MHz

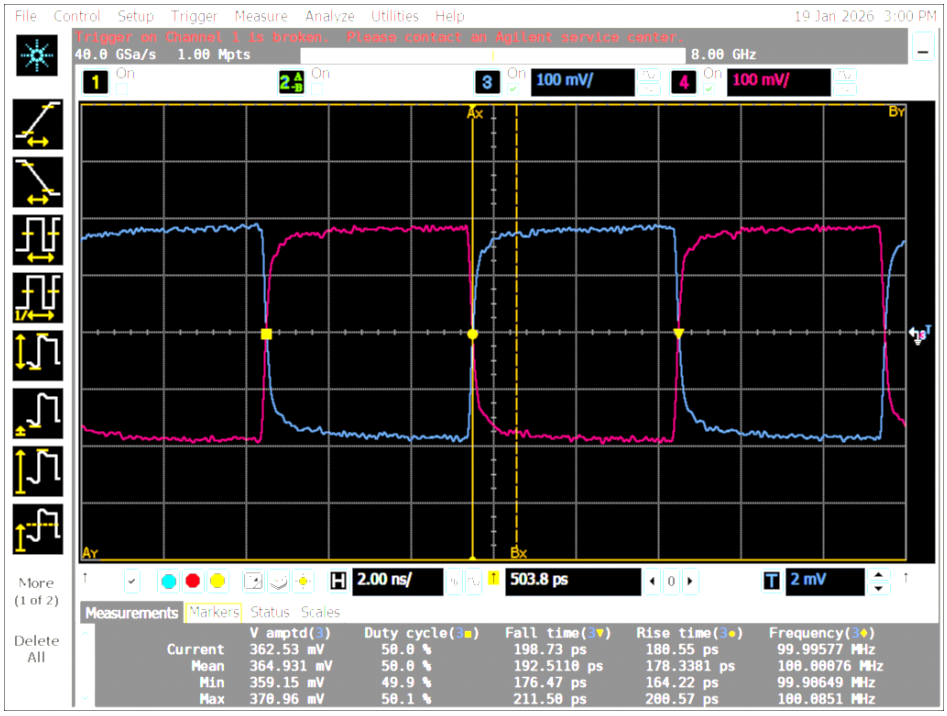

Figure 21. Sample Signal Integrity for LVDS @100 MHz

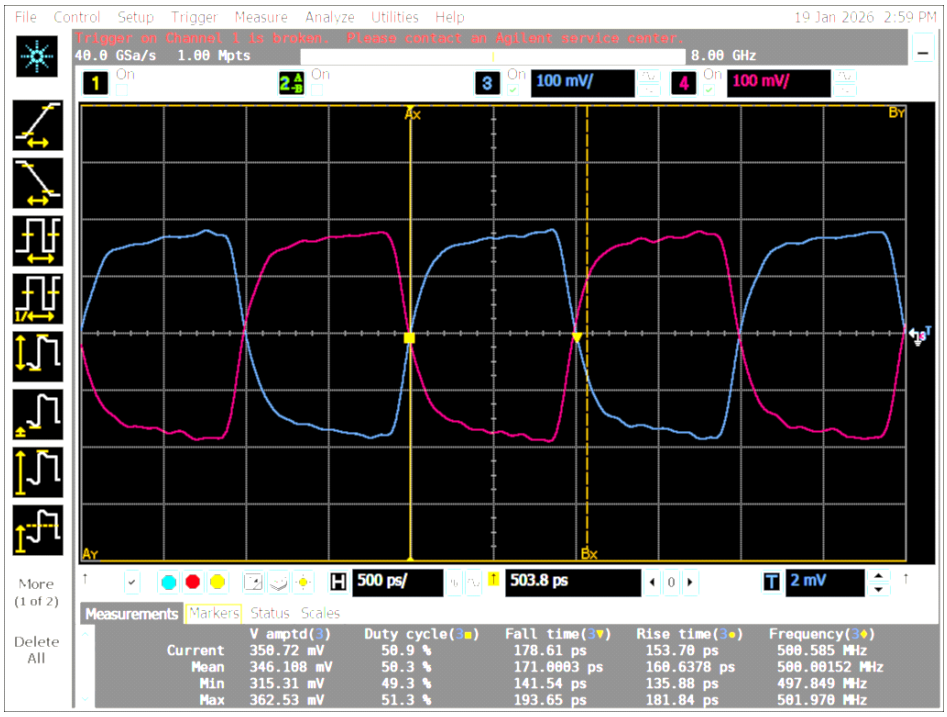

Figure 22. Sample Signal Integrity for LVDS @500 MHz

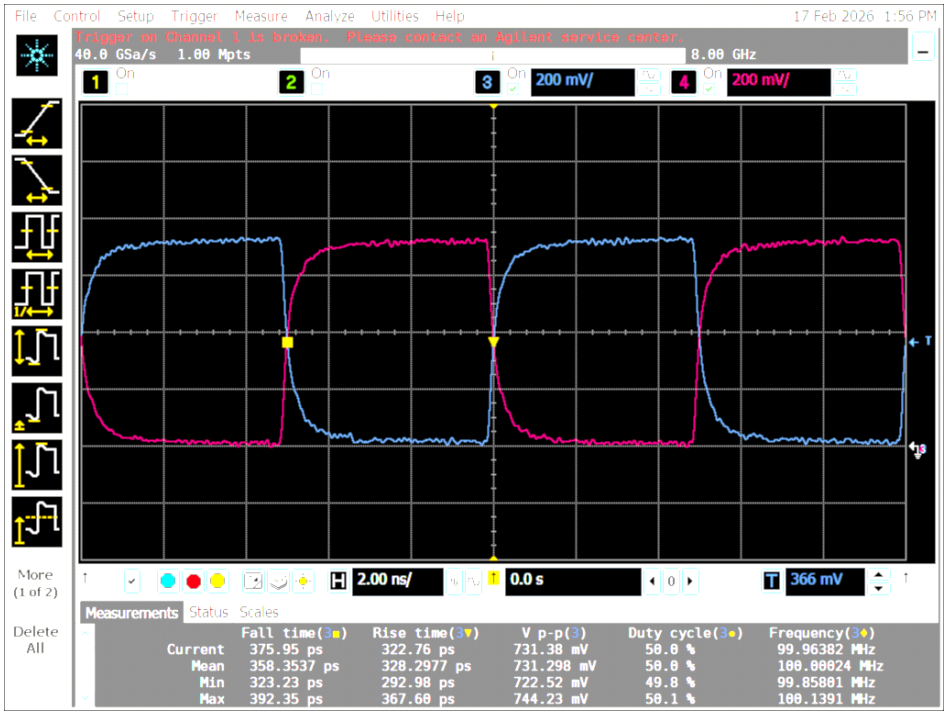

Figure 23. Sample Signal Integrity for HCSL @100 MHz

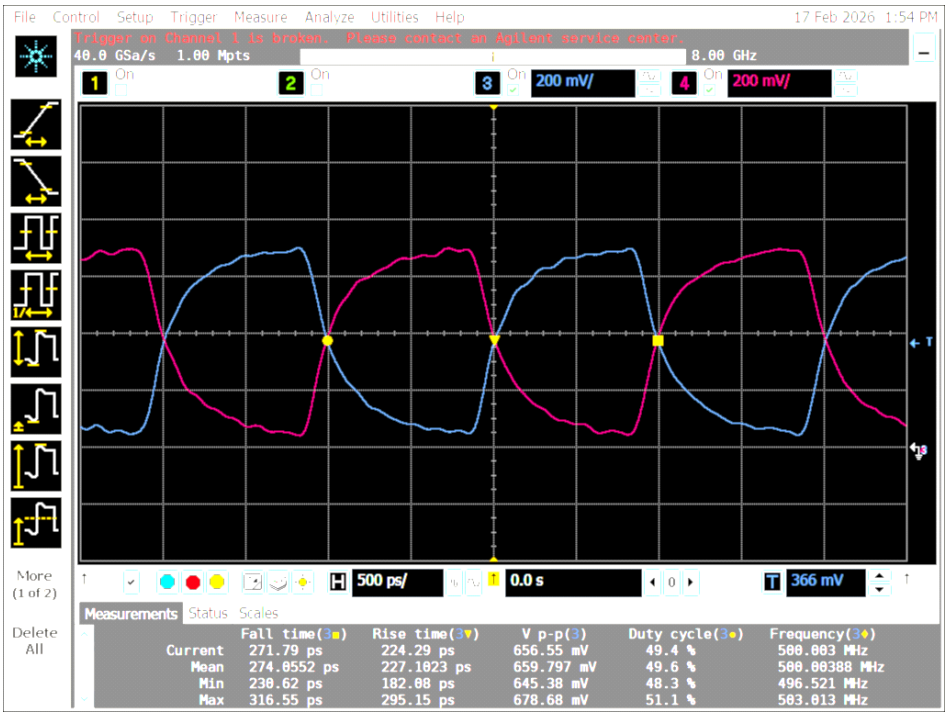

Figure 24. Sample Signal Integrity for HCSL @500 MHz

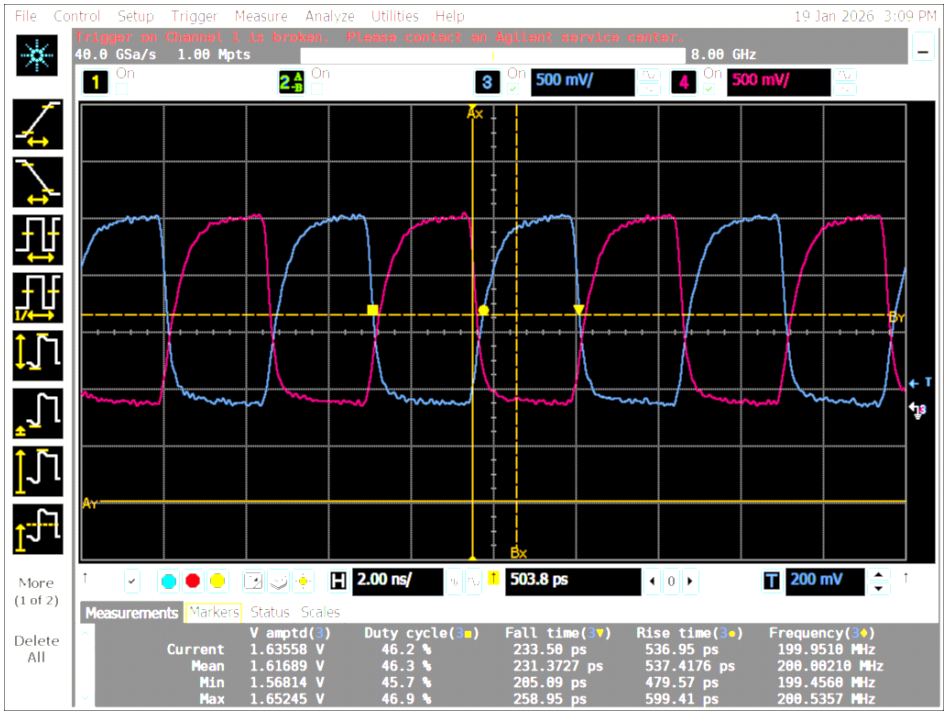

Figure 25. Sample Signal Integrity for C-CMOS @200 MHz (Terminated 50 Ω to Ground at Scope)

8.4. Additive Jitter

Additive jitter is dependent on several parameters of the input clock: frequency, slew rate, and input rms jitter. To achieve the most accurate additive jitter measurement, the source jitter must be much smaller (ideally, 50% or less) than the jitter contribution of the buffer itself. Note that when the source jitter is equal or greater than the additive jitter of the buffer, the measured additive jitter can be overly optimistic.

Figure 26 shows a block diagram of the setup used for measuring additive jitter. The board's default configuration (refer to Table 10) is the configuration needed for making phase noise measurements, so no alteration of the board is needed to perform these measurements.

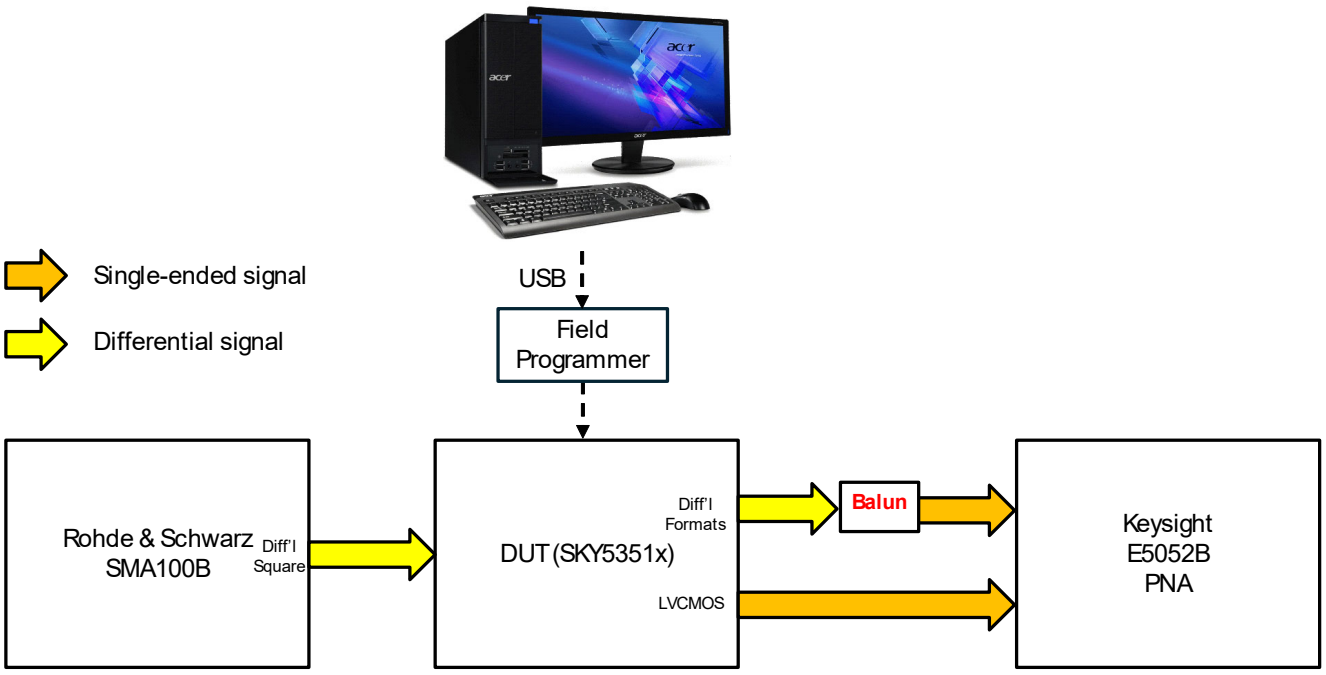

Figure 26. Additive Jitter Measurement Setup Block Diagram

The following figures provide examples of additive jitter for LVPECL, LVDS, HCSL at both 156.25 MHz and 625 MHz, and LVCMOS at 156.25 MHz (differential and single-ended input clock). The additive jitter was calculated by measuring the total rms jitter (source + buffer) and subtracting the source rms jitter (SMA100B) using the root sum of squares (RSS) technique over an integrated bandwidth of 12 kHz to 20 MHz.

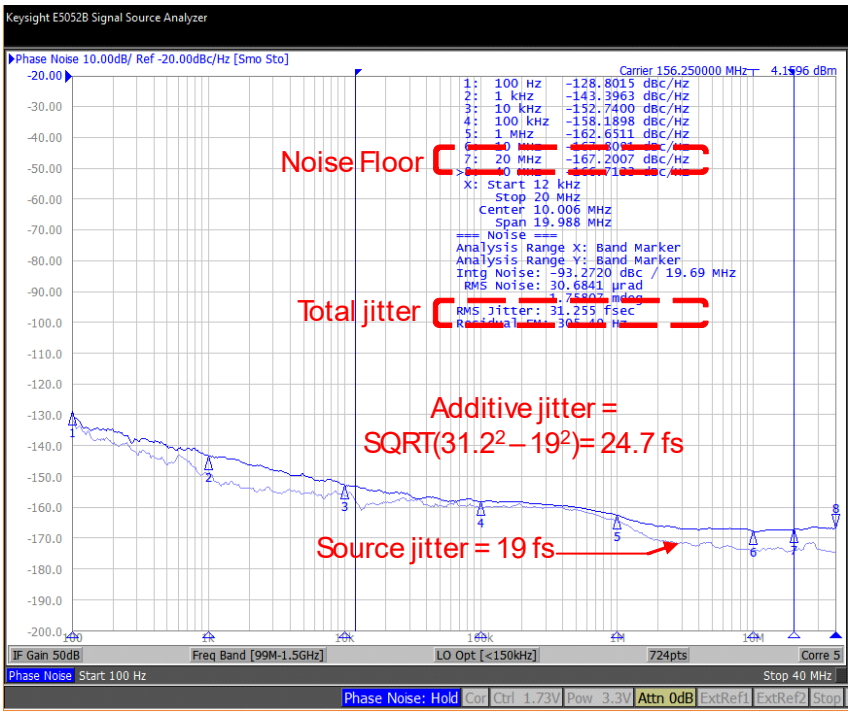

Figure 27. Sample PN Plot for 156.25 MHz LVPECL Output

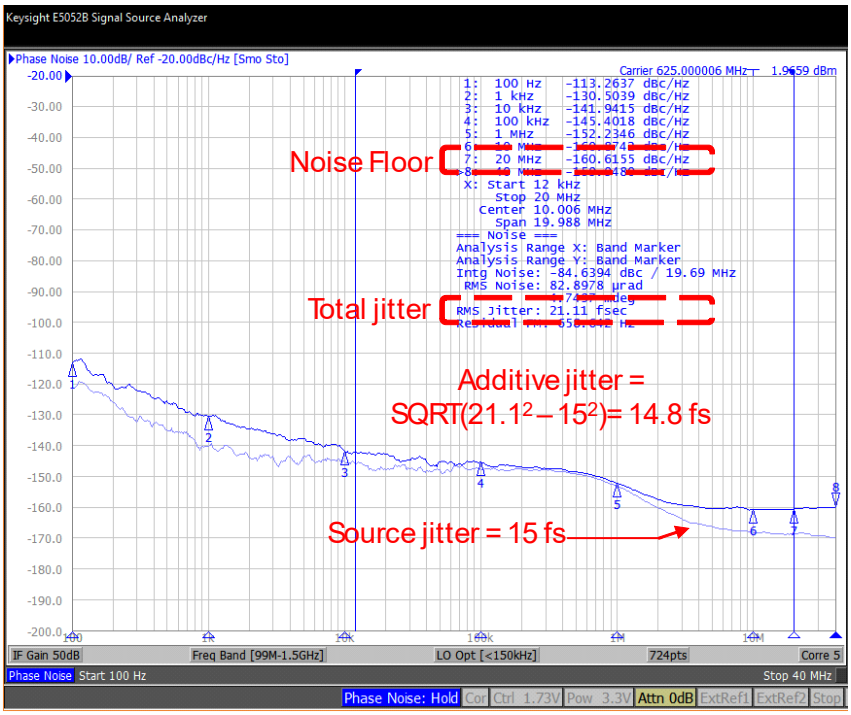

Figure 28. Sample PN Plot for 625 MHz LVPECL Output

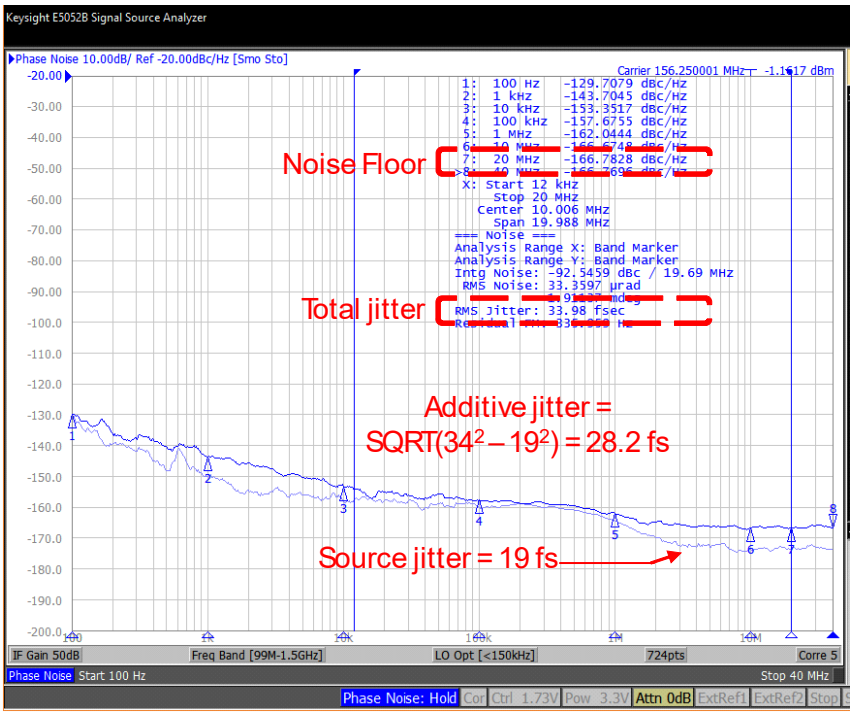

Figure 29. Sample PN Plot for 156.25 MHz LVDS Output

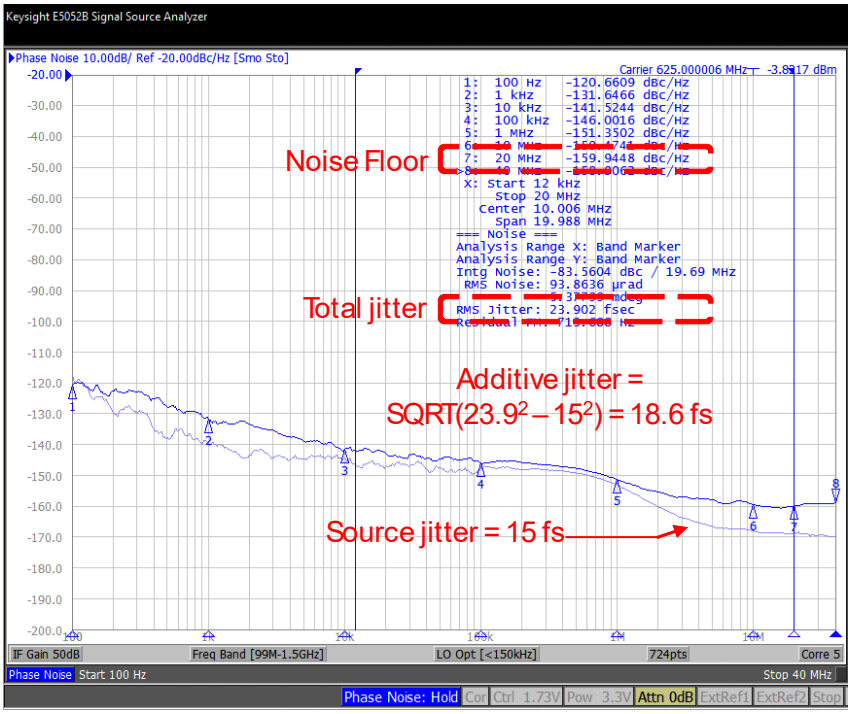

Figure 30. Sample PN Plot for 625 MHz LVDS Output

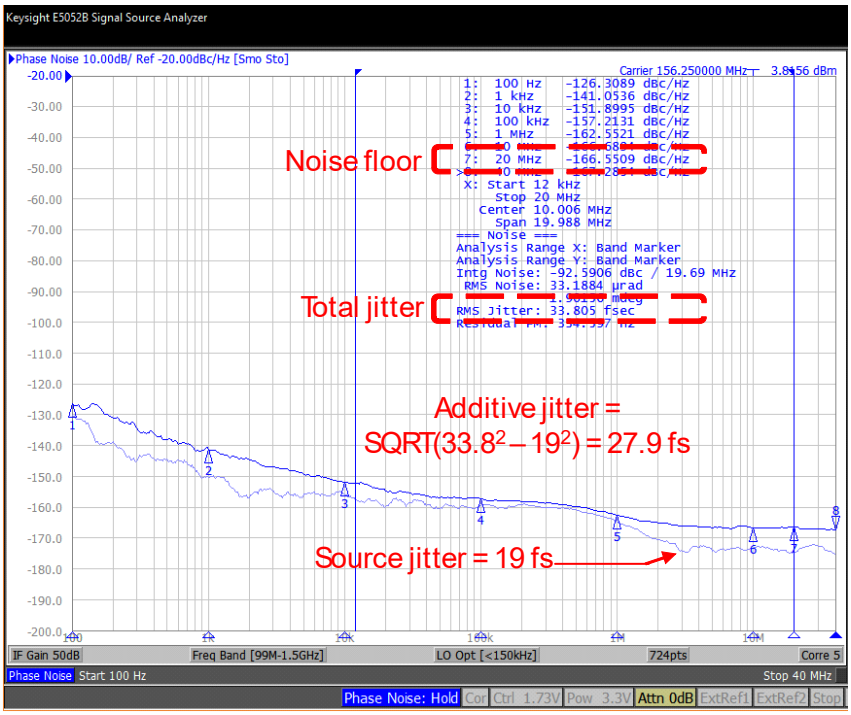

Figure 31. Sample PN Plot for 156.25 MHz HCSL Output

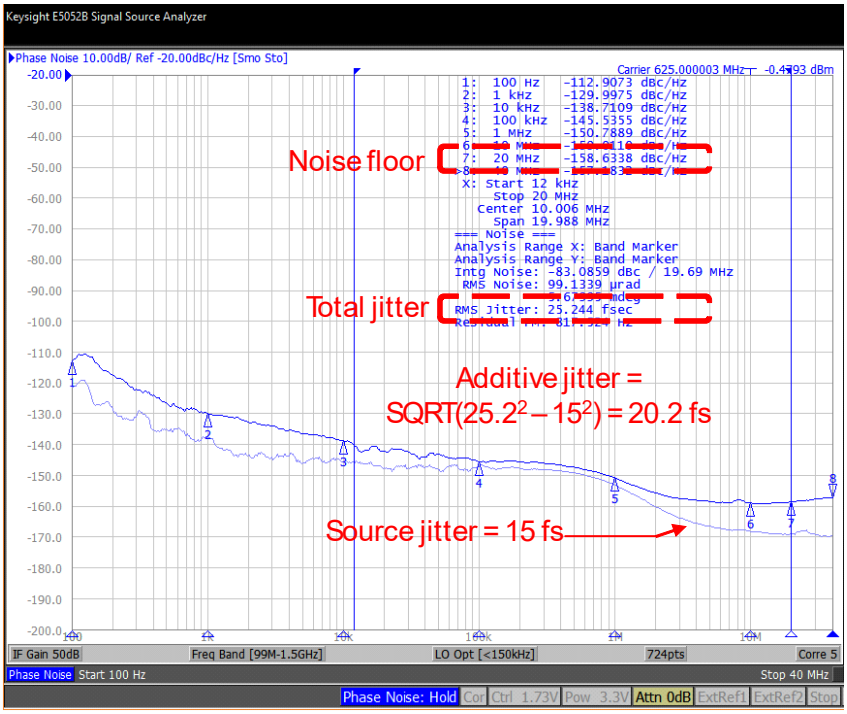

Figure 32. Sample PN Plot for 625 MHz HCSL Output

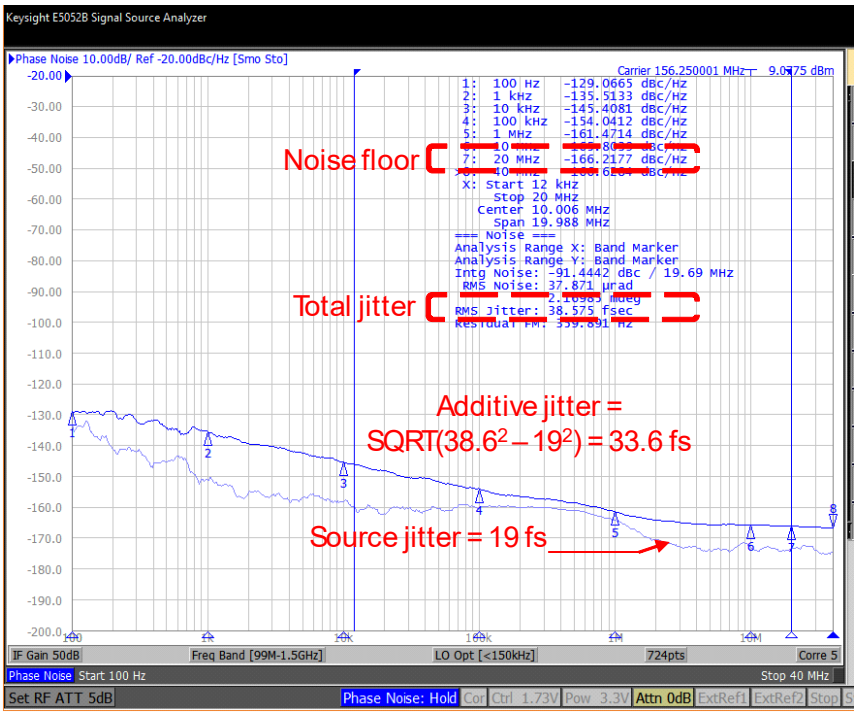

Figure 33. Sample PN Plot for 156.25 MHz LVCMOS Output (Differential Input Clock)

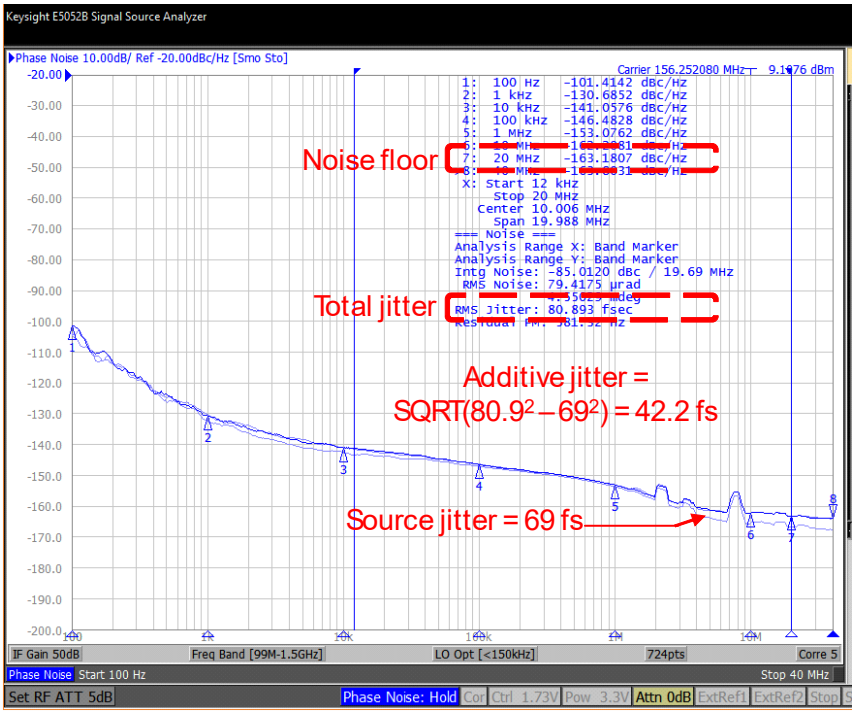

Figure 34. Sample PN Plot for 156.25 MHz LVCMOS Output (Single-Ended Input Clock)

8.5. Input Mux Isolation

Figure 35 shows a block diagram of the setup used for measuring input mux isolation. A 156.25 MHz LVPECL carrier is applied to CLKIN0 by Q-divider output of Si5518 CEVB. An interfering tone at 156.25 MHz + offset freq (offsets of 10 kHz, 100 kHz, 500 kHz, and 10 MHz were used) is applied to CLKIN1 by N-divider LVPECL output of the Si5518 CEVB. The amplitude of the spur at the offset frequency applied to CLKIN1 was measured on the PNA.

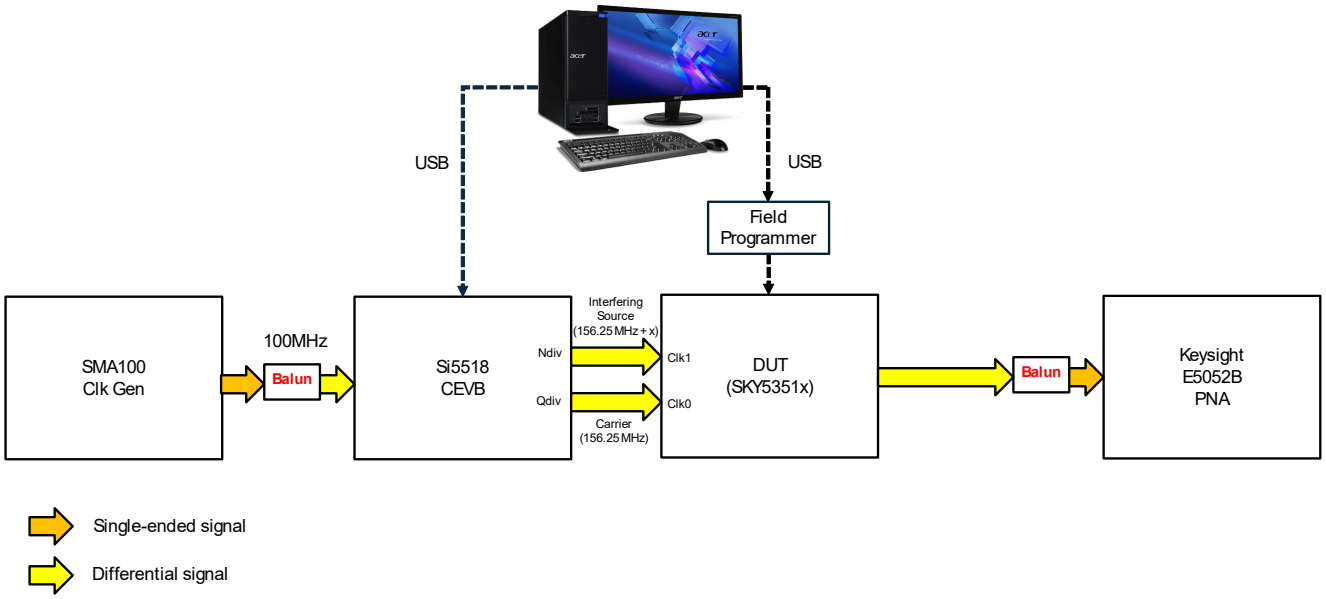

Figure 35. Block Diagram of Setup Used to Measure Input Mux Isolation

The following figures provide the PNA plots for the four offset noise frequencies mentioned above using the setup shown in Figure 35.

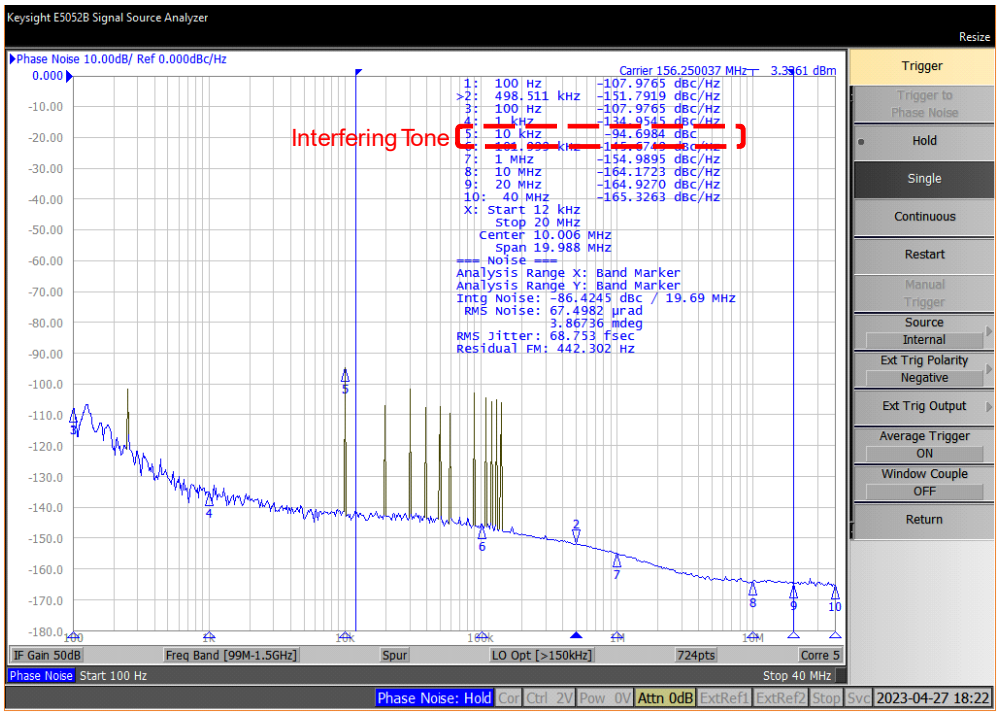

Figure 36. Sample PN Plot for Noise Source Offset = 10 kHz

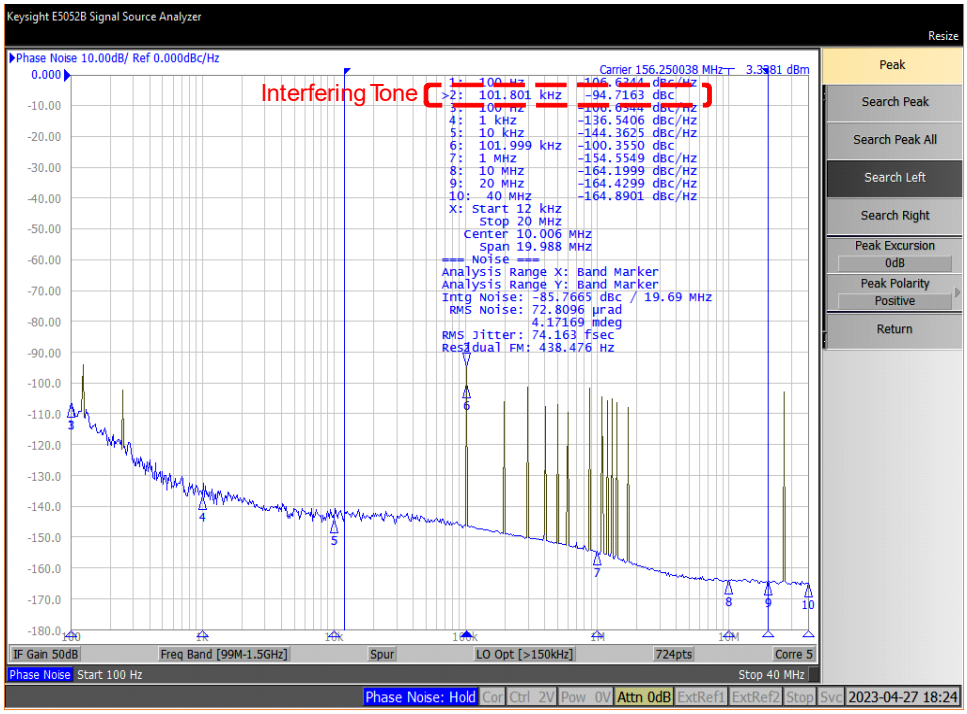

Figure 37. Sample PN Plot for Noise Source Offset = 100 kHz

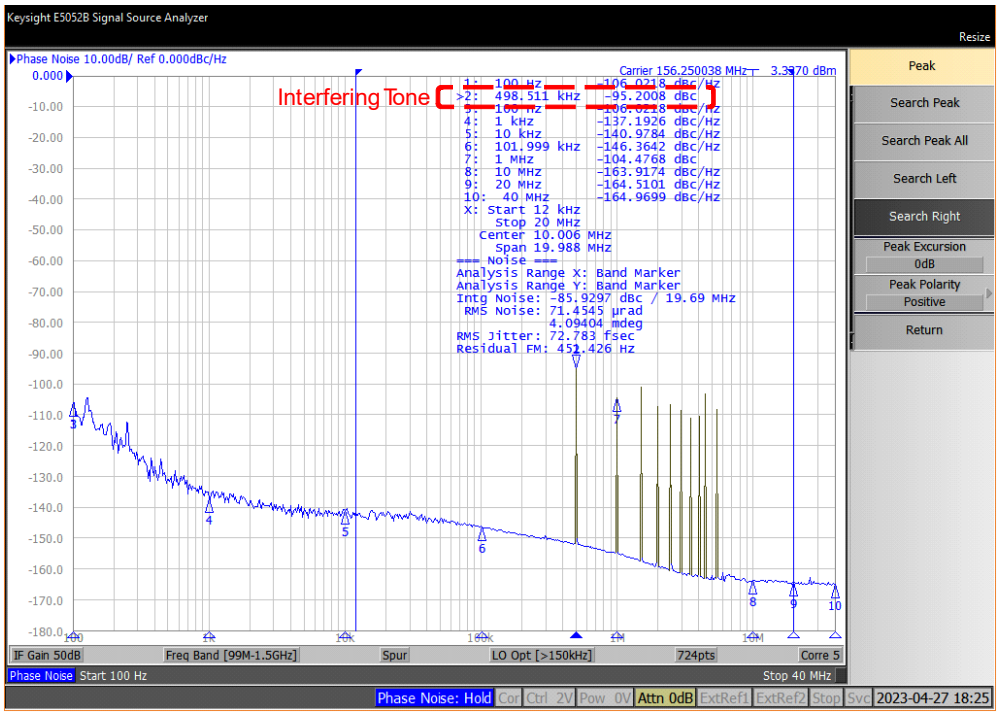

Figure 38. Sample PN Plot for Noise Source Offset = 500 kHz

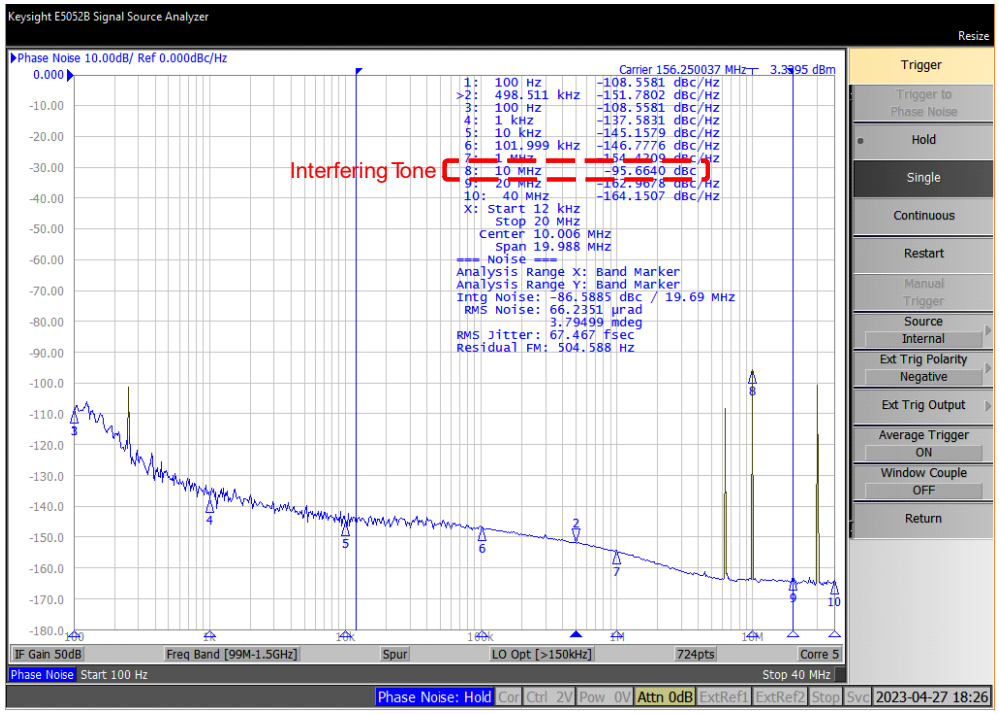

Figure 39. Sample PN Plot for Noise Source Offset = 10 MHz

9. Schematics and BOM

The schematics and BOMs for all four OPNs can be found on the Skyworks web site:
Skyworks/Evaluation Kit Specification - SKY53511-A-EVB

10. Appendix—Setting up I²C Communication with the DUT Using the Field Programmer Dongle

For OPNs SKY53512-A-EVB and SKY53513-A-EVB, the DUT is configured via I²C control (rather than via switch S1). Perform the following steps to set up the Field Programmer dongle to communicate with the DUT:

1. Download CBPro software by going to the following link: Skyworks | Timing - Clockbuilder Pro Software (CBPro) and clicking on the “installer” link shown in Figure 40 below.

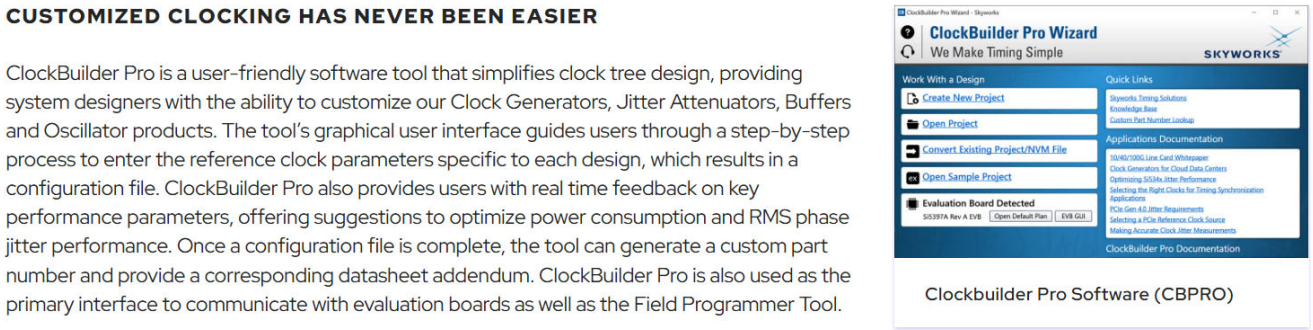

Figure 40. CBPro Installer Link

2. Connect the Field Programmer Dongle to the CEVB as shown in Figure 41 and Table 11 below.

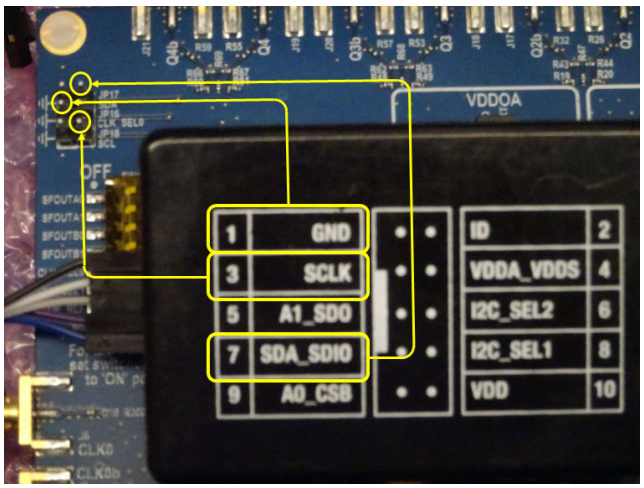

Figure 41. Connecting the Field Programmer Dongle to the CEVB

Table 11. Dongle to CEVB Connections

Dongle Pin	CEVB Pin
1 (GND)	JP16 pin 1 (GND)
3 (SCLK)	JP18 pin 2 (SCL)
7 (SDA_SDIO)	JP17 pin 2 (SDA)

3. When the CBPro Wizard opens, click on the EVB GUI button shown in Figure 42:

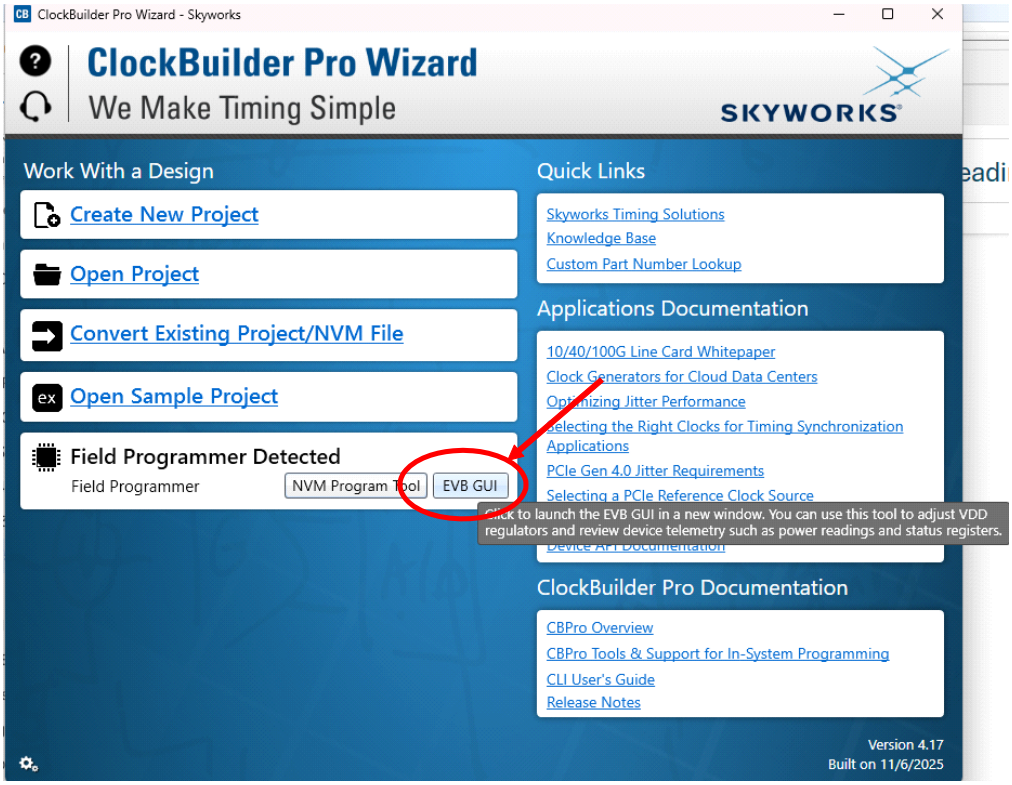

Figure 42. EVB GUI Button

4. When the GUI opens, click the “Config” button and in the “Device Family” pull-down menu, select “Si5338/56”. For “I/O Voltage” select 3.3 V and for the “I^{2}C Address” choose “0x2A” for the SKY53512-A-EVB OPN or “0x3A” for the SKY53513-A-EVB OPN.

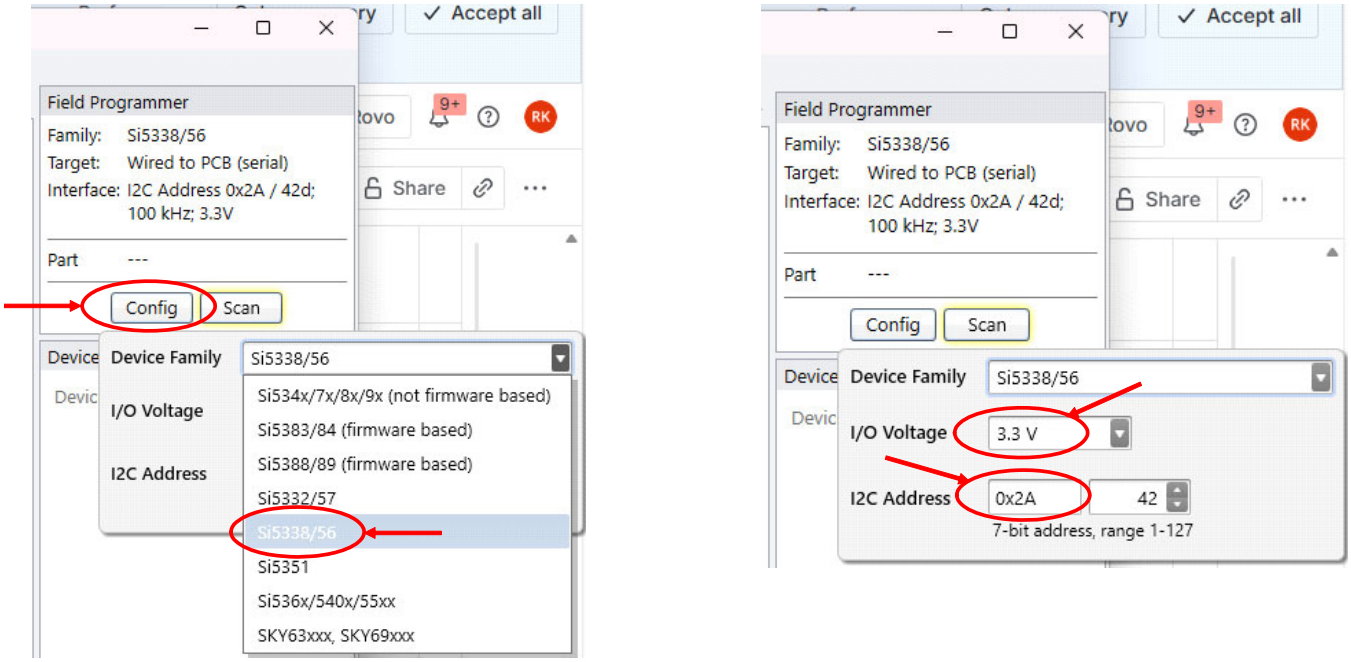

Figure 43. Config Button and Device Family Pull-Down

5. Now, make sure that Switches 2 and 7 on SW1 are in the “ON” position.
6. Click “Scan” and you should see the following screen below. “Part” should be “Si5338”. If you get an error, check the connections from Step 2, remove the USB cable from the dongle and re-insert, make sure you used the correct I^{2}C address for the OPN being tested, and as a last resort, restart your computer.

   In the tabs on the left screen, click “DUT Register Editor” and it should appear as shown below:

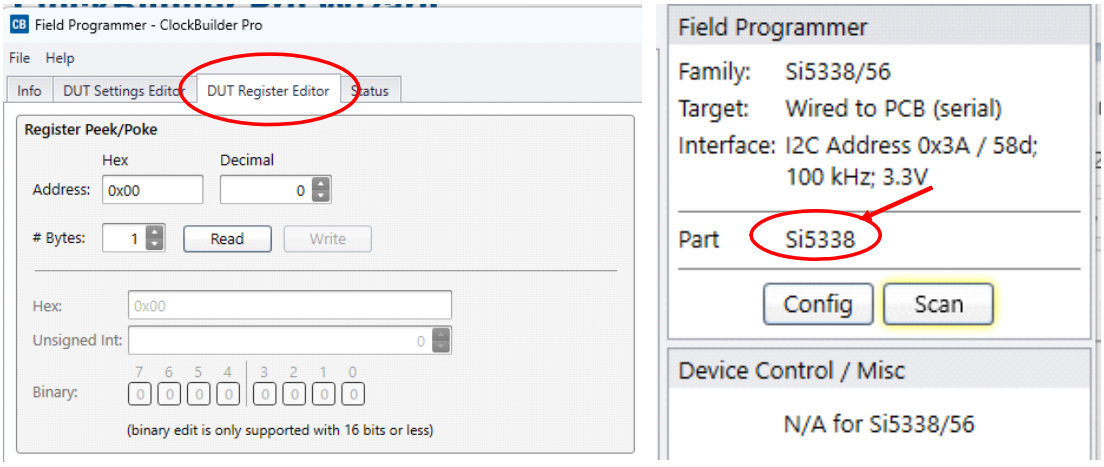

Figure 44. DUT Register Editor

7. By default, all the outputs (Q0:Q9) are disabled and therefore need to be enabled by selecting the appropriate address in the “Register Peak/Poke” section and setting the OEx bit (bit 0). Note, do not change any other bits in these registers. The complete Register Map for the SKY5351x is shown below:

7x7 10-Out SKY53513/12 User Register Map

SKY5351x - 10 Out - 7x7									
addr	***Hex***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
3	0003	0	0	0	0	0	**0**	**0**	**RESET**
315	013B	**FORMAT_A**		0	**1**	0	0	0	0
316	013C	**FORMAT_B**		0	**1**	0	0	0	0
318	013E	**1**	**1**	**1**	0	0	**1**	**EN_REF**	**REF_PWR**
319	013F	**INSEL_REFOUT**		0	**INSEL_B**		0	**INSEL_A**	
321	0141	0	0	**0**	0	0	0	**1**	**OE0**
325	0145	0	0	**0**	0	0	0	**1**	**OE1**
329	0149	0	0	**0**	0	0	0	**1**	**OE2**
333	014D	0	0	**0**	0	0	0	**1**	**OE3**
337	0151	0	0	**0**	0	0	0	**1**	**OE4**
341	0155	0	0	**0**	0	0	0	**1**	**OE5**
345	0159	0	0	**0**	0	0	0	**1**	**OE6**
349	015D	0	0	**0**	0	0	0	**1**	**OE7**
353	0161	0	0	**0**	0	0	0	**1**	**OE8**
357	0165	0	0	**0**	0	0	0	**1**	**OE9**
376	0178	0	0	0	0	**IN0_DIS**	0	0	**0**
379	017B	0	0	0	0	**IN1_DIS**	0	0	**0**

Figure 45. SKY5351x Register Map

For example, to enable output Q6, enter Hex address 0x0159 and click “Read” - it should return as 0x02 in the Hex box. Set bit 0 to a “1” as shown below and click the “Write” button. Q6 should now be enabled. Continue in like manner until all desired outputs have been enabled.

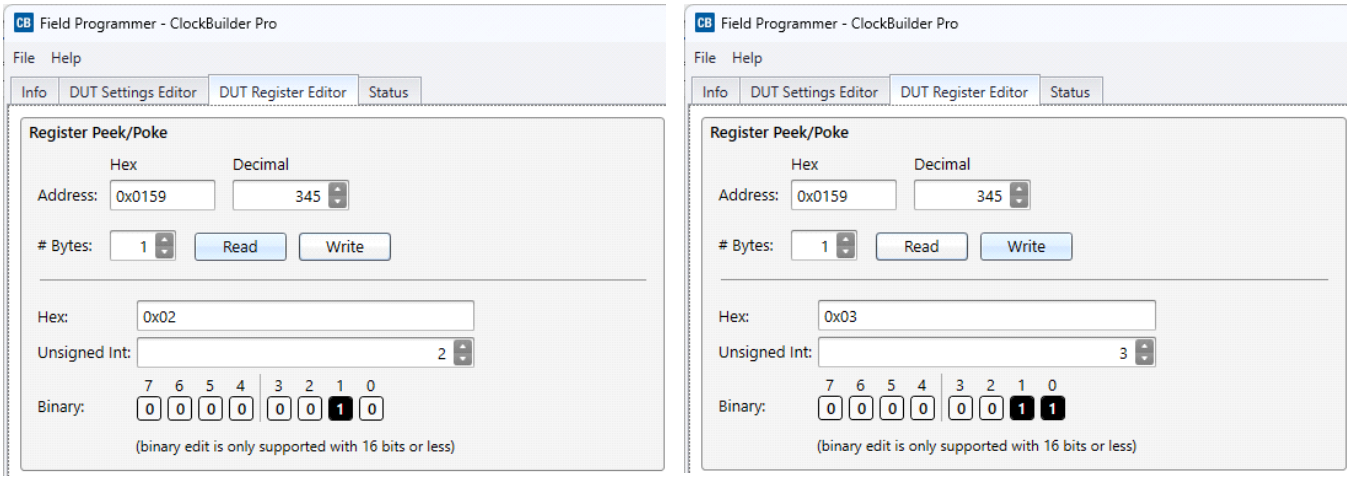

Figure 46. Enabling Outputs Example

To enable the REFOUT output, set bits 0 and 1 of register 0x013E (EN_REF, REF_PWR) to a “1”, and click “Write”. Do not change any other bits in this register.

11. Revision History

Revision	Date	Description
A	April, 2026	Initial release.