USER GUIDE

UG541: Skyworks Neptune and Triton Evaluation Platforms

Features

- Evaluation platforms powered by the 5 V wall adapter included in the kit or an external 5 V lab supply
- Flexible power supply tree allows evaluation of NetSync™ performance with both low dropout regulators (LDOs) and switching regulators
- LDO voltages programmable to 3.3/2.5/1.8 V using the Skyworks ClockBuilder® Pro (CBPro) evaluation board (EVB) GUI
- Current, voltage, and power sensing per LDO
- Onboard oven-controlled crystal oscillator (OCXO) and temperature-compensated crystal oscillator (TCXO)
- SMA connectors for clock inputs and outputs
- Status LEDs for general-purpose input/output (GPIO) status pins
- Header pins for GPIO control pins
- Host interface connector allows evaluation platforms to be used in conjunction with a third-party CPU for AccuTime™ + NetSync evaluation boards

Description

The Neptune evaluation platform is used to evaluate the 144-pin BGA SKY69110, SKY69120, and SKY69115 NetSync network synchronizers.

The Triton evaluation platform is used to evaluate the 64-pin quad flat no-lead (QFN) SKY69112, SKY69116, and SKY69122 NetSync network synchronizers.

The network synchronizers are used in Synchronous Ethernet (SyncE) and IEEE 1588 precision time protocol (PTP) applications. These devices combine the low-bandwidth operation and digitally controlled oscillator functionality needed for ITU-T G.8262/8262.1 SyncE and IEEE 1588 support with ultra-low-jitter outputs that allow clocking of 224G SerDes without a separate jitter attenuator.

These devices can also be used in distributed timing systems with redundant timing cards and line cards, where each device holds the time of day. The Neptune and Triton evaluation platforms are designed to be used in conjunction with CBPro software.

This document is intended to be used with both 144-pin ball grid array (BGA) and 64-pin QFN NetSync devices. The exact device and revision is distinguished by a white label underneath the silkscreen name on the board. Strictly for ordering purposes, the terms “EB” and “EVB” refer to the board and kit, respectively. In this document, the terms are synonymous.

1. Functional Block Diagram

The block diagrams for the Neptune and Triton evaluation platforms are shown in Figure 1 and Figure 2. The Skyworks NetSync is shown in the blue block.

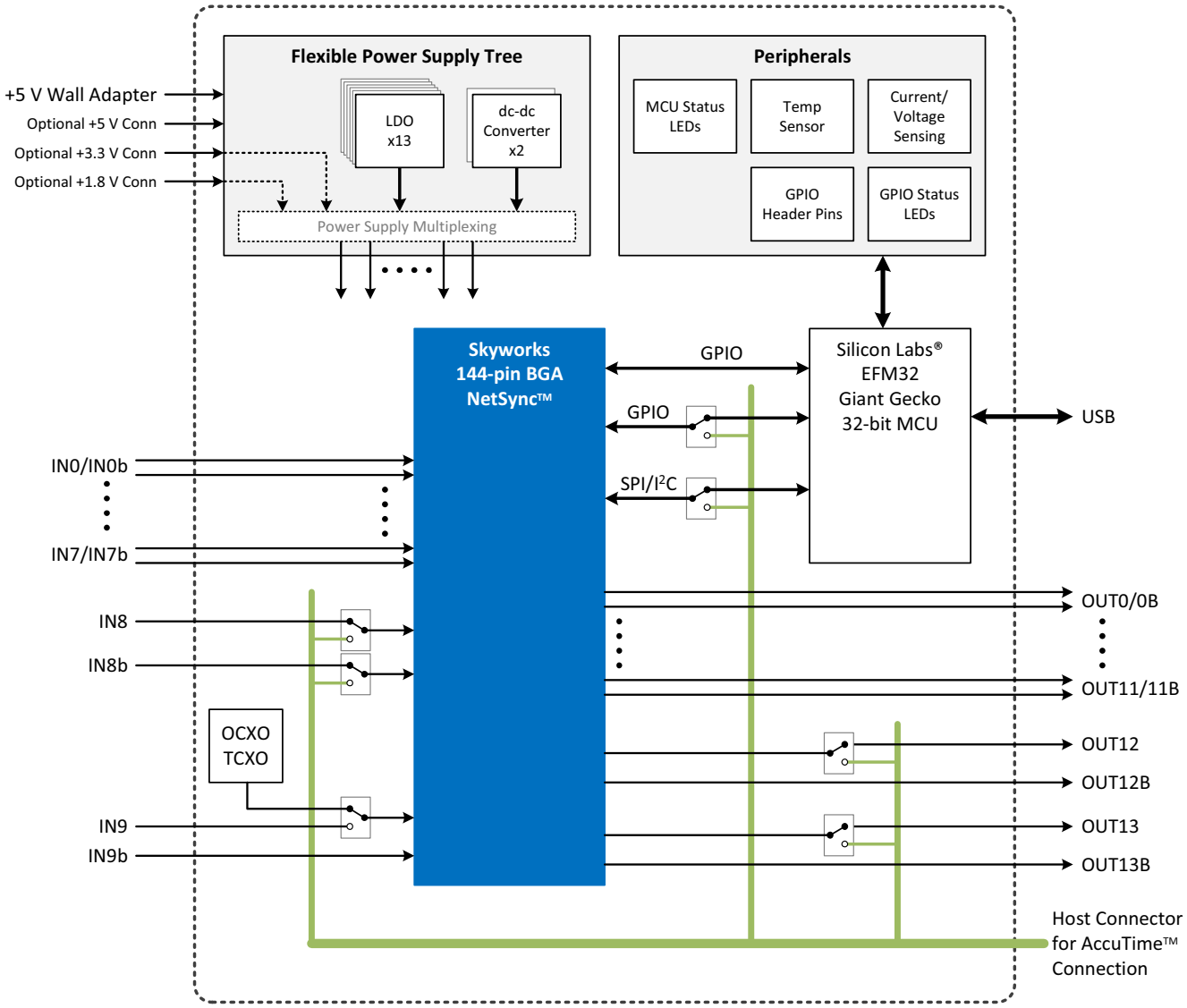

Figure 1. Neptune Evaluation Board Block Diagram

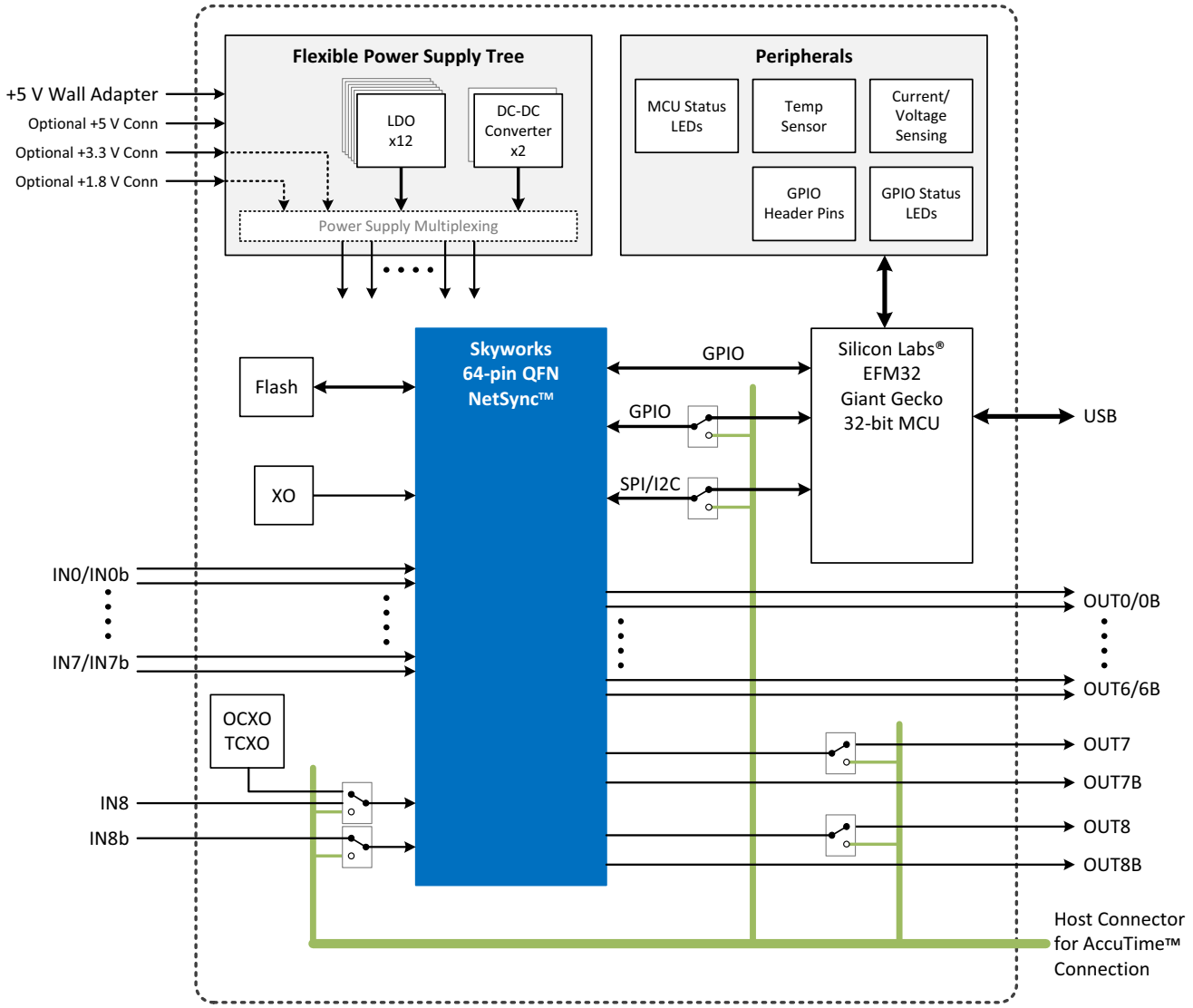

Figure 2. Triton Evaluation Board Block Diagram

2. Quick Start Guide

When first receiving the EVB, perform the following steps to ensure that the device under test (DUT) receives power and signal communications. Figure 3 shows the jumpers that need to be installed/uninstalled to get the board up and running. The TCXO/OCXO jumpers may not apply if that feature is not being used. Similar jumper settings should be applied for either Neptune or Triton evaluation platforms.

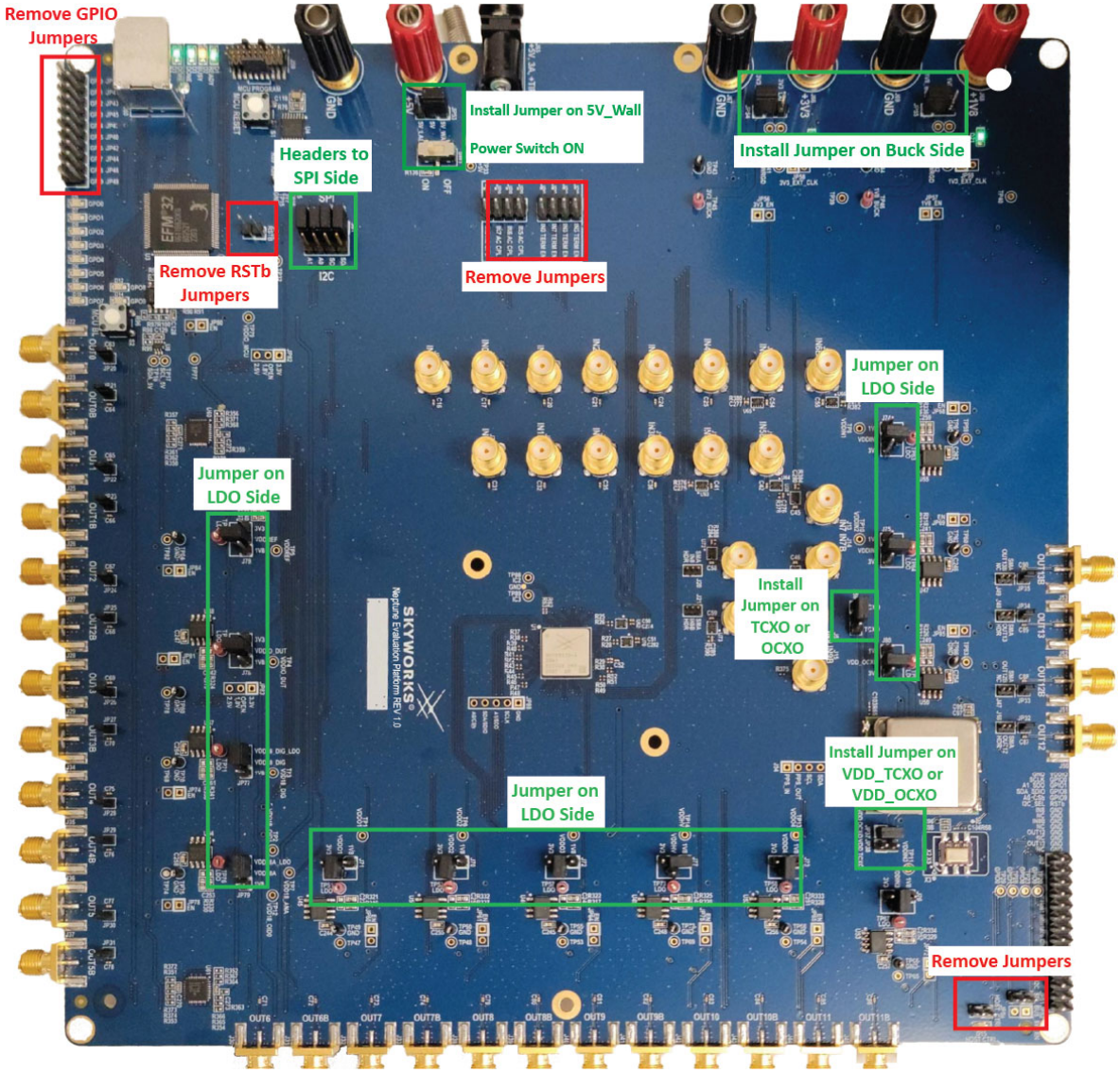

Figure 3. Evaluation Board Quick Start Jumper Settings

After the jumpers are installed, plug the 5 V dc adapter included in the EVB kit into the J65 barrel plug. Then, plug in the included USB cable and turn SW1 to “ON.”

After using the power switch (down-right from the power barrel jack) to turn the board on, a frequency plan may be written to the DUT. The next section briefly covers using ClockBuilder Pro with the EVB as a quick start guide. For more guidance on using CBPro and creating a frequency plan, see the reference manual.

3. Using ClockBuilder® Pro with the EVB

The evaluation platforms are designed to work with CBPro to streamline the development process. To get started with a sample frequency plan, open CBPro and select “Open Sample Project.” If you have an existing project file, you may select “Open Project” instead and skip to the end of this section.

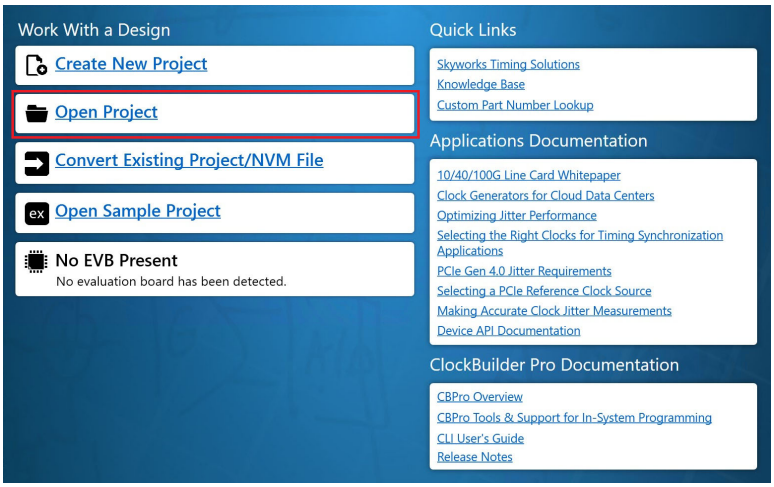

Figure 4. Opening a Sample Project in ClockBuilder® Pro

If the EVB is plugged into USB and has power, it appears under “Evaluation Board Detected.” The opened frequency plan can then be written to the DUT by clicking **Write Design to EVB.** The write process takes roughly 30 seconds, with CBPro reporting the status of any write processes as well as any errors that occur.

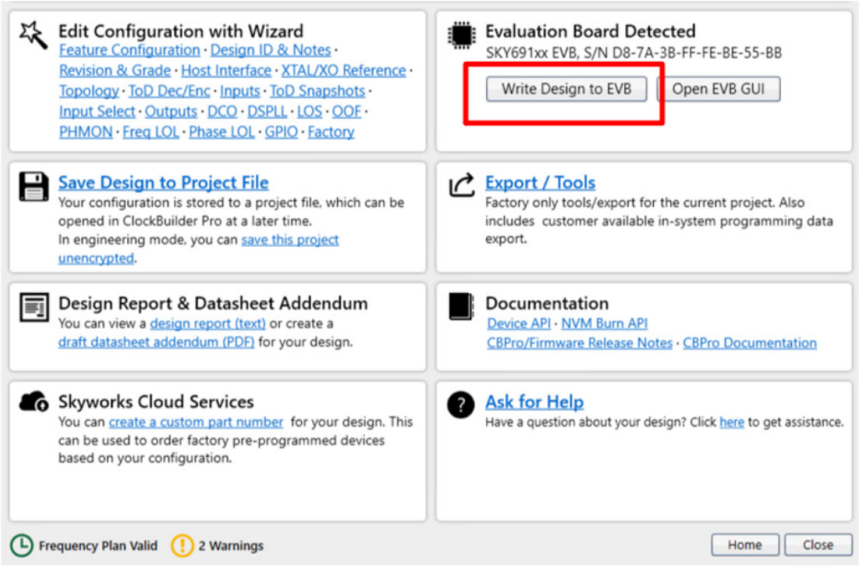

Figure 5. Writing a Frequency Plan to the EVB in ClockBuilder Pro

Click **Open EVB GUI** to read information about the device, interact with the device through the API, look at voltage and current readings, set/read GPIO information, and monitor statuses such as PLL lock and input clock state.

4. EVB Overview

Figure 6 and Figure 7 show overhead pictures of the EVBs, highlighting the main areas the user may reconfigure to meet application needs. The NetSync DUT is in the middle of the board, with clock outputs on the left, bottom, and right sides of the board. An OCXO and TCXO option are available for the network synchronizer board variants.

The host interface connector is used to interface with the DUT with an external processor, but this is typically not needed for most evaluations. The input clock vertical SMAs are in the center of the board. The MCU is responsible for communicating with the DUT, host PC, and peripherals. The GPIO header bank is used for GPIs, and the LED bank is used for GPOs. The power supply region to generate the main power planes is located on the upper side of the board. LDOs around the DUT supply the individual VDD pins of the DUT.

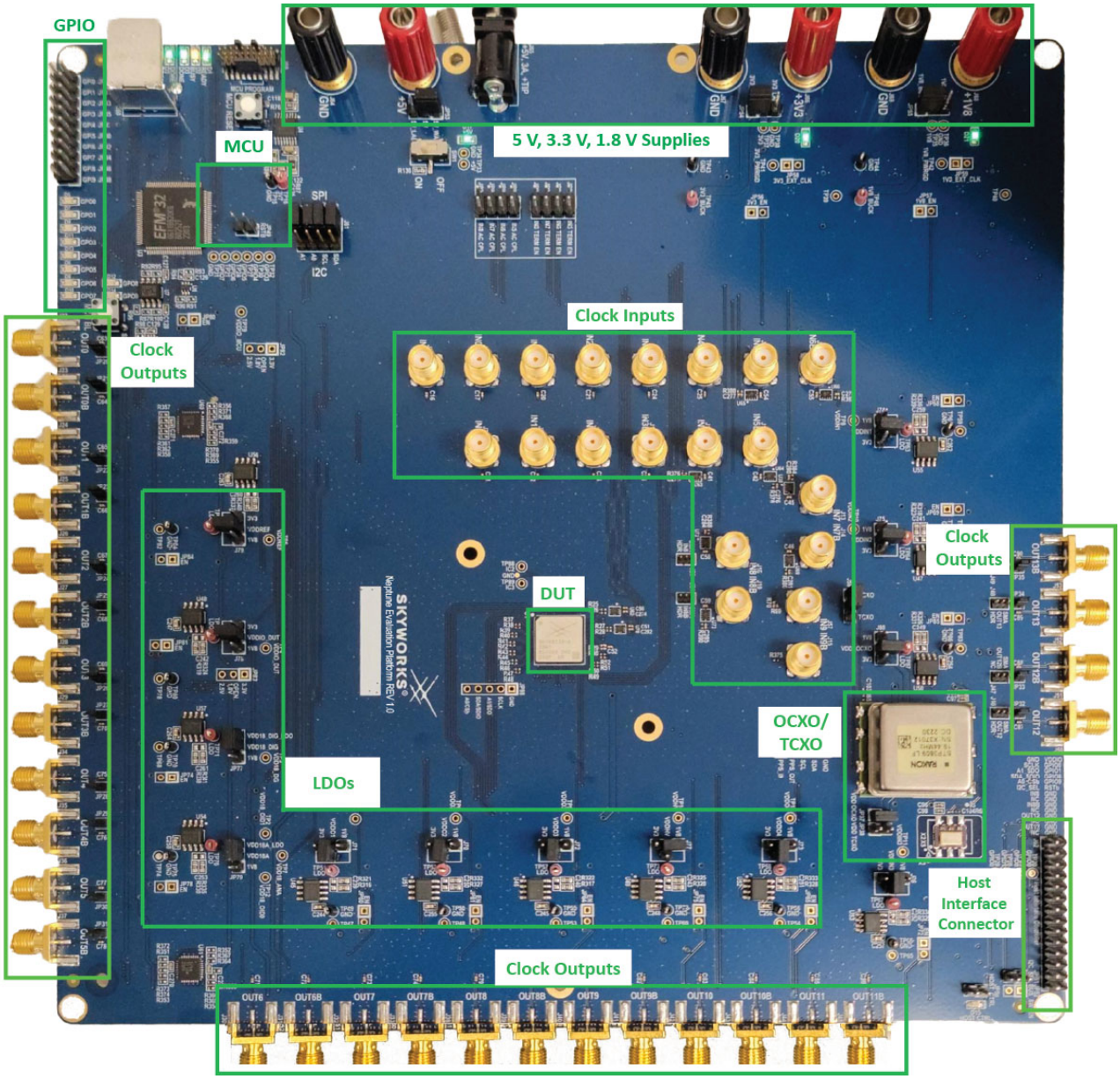

Figure 6. Neptune Evaluation Board Overview

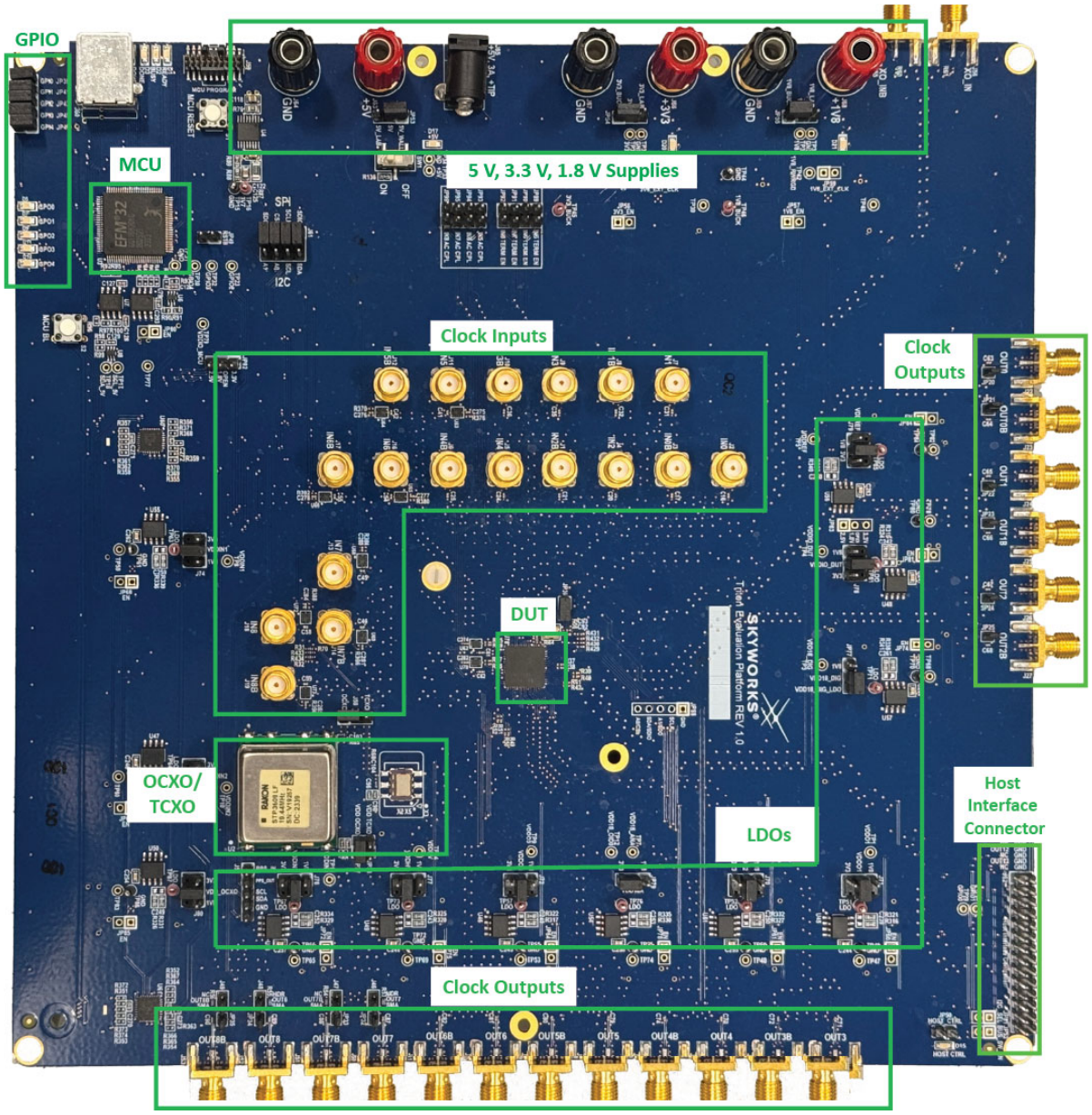

Figure 7. Triton Evaluation Board Overview

5. Jumper Defaults

The default jumper settings related to the input clocks are shown in Table 1. For most applications, the default jumper settings are the optimal settings. For further details and jumper locations on the board, see "8.2. Flexible Clock Inputs [IN5-IN8]" on page 26 and "8.3. Clock Inputs from Host Connector [IN8/IN8b]" on page 28.

Table 1. Clock Input Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP89	JP89	2-pin	Enables split termination for IN5[1]	Open
JP90	JP90	2-pin	Enables split termination for IN6[1]	Open
JP91	JP91	2-pin	Enables split termination for IN7[1]	Open
JP92	JP92	2-pin	Enables split termination for IN8[1]	Open
JP93	JP93	2-pin	Enables ac coupling for IN5[1]	Open
JP94	JP94	2-pin	Enables ac coupling for IN6[1]	Open
JP95	JP95	2-pin	Enables ac coupling for IN7[1]	Open
JP96	JP96	2-pin	Enables ac coupling for IN8[1]	Open
J20	-	3-pin	IN8 SMA or host connector select[2,3]	IN8-SMA
J21	-	3-pin	IN8b SMA or host connector select[2,3]	IN8B-SMA

1. The onboard MCU sets this pin automatically according to the CBPro project file.
2. Install jumper shunts on positions 1-2 for SMA. Install on positions 2-3 for host connector.
3. Jumper pitch is 50 mil.

The jumper settings for the output clocks are in Table 2. The ac-coupling capacitor bypass jumpers need to be installed/removed based on the required frequency plan. For further details and header pin locations on the board, see "8.5. Flexible Clock Outputs [BGA: OUT0-5,12-13; QFN: OUT0-2,7-8]" on page 29 and "8.7. Clock Outputs from Host Connector [BGA: OUT12-13, QFN: OUT7-8]" on page 30.

Table 2. Clock Output Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP20	JP20	2-pin	OUT0 ac-coupling capacitor bypass[1]	Open
JP21	JP21	2-pin	OUT0b ac-coupling capacitor bypass[1]	Open
JP22	JP22	2-pin	OUT1 ac-coupling capacitor bypass[1]	Open
JP23	JP23	2-pin	OUT1b ac-coupling capacitor bypass[1]	Open
JP24	JP24	2-pin	OUT2 ac-coupling capacitor bypass[1]	Open
JP25	JP25	2-pin	OUT2b ac-coupling capacitor bypass[1]	Open
JP26	-	2-pin	OUT3 ac-coupling capacitor bypass[1]	Open
JP27	-	2-pin	OUT3b ac-coupling capacitor bypass[1]	Open
JP28	-	2-pin	OUT4 ac-coupling capacitor bypass[1]	Open
JP29	-	2-pin	OUT4b ac-coupling capacitor bypass[1]	Open
JP30	-	2-pin	OUT5 ac-coupling capacitor bypass[1]	Open
JP31	-	2-pin	OUT5b ac-coupling capacitor bypass[1]	Open
JP32	-	2-pin	OUT12 ac-coupling capacitor bypass[1]	Open
JP33	-	2-pin	OUT12b ac-coupling capacitor bypass[1]	Open
JP34	-	2-pin	OUT13 ac-coupling capacitor bypass[1]	Open
JP35	-	2-pin	OUT13b ac-coupling capacitor bypass[1]	Open
J46	-	3-pin	OUT12 SMA or host connector select[2,3]	2-3
J47	-	3-pin	OUT12b SMA or host connector select[2,3]	2-3
J48	-	3-pin	OUT13 SMA or host connector select[2,3]	2-3
J49	-	3-pin	OUT13b SMA or host connector select[2,3]	2-3
-	JP32	2-pin	OUT7 ac-coupling capacitor bypass[2,3]	Open
-	JP33	2-pin	OUT7b ac-coupling capacitor bypass[2,3]	Open
-	JP34	2-pin	OUT8 ac-coupling capacitor bypass[2,3]	Open
-	JP35	2-pin	OUT8b ac-coupling capacitor bypass[2,3]	Open
-	J46	3-pin	OUT7 SMA or host connector select[2]	2-3
-	J47	3-pin	OUT7b SMA or host connector select[2]	2-3
-	J48	3-pin	OUT8 SMA or host connector select[2]	2-3
-	J49	3-pin	OUT8b SMA or host connector select[2]	2-3

1. Install jumper shunt for dc-coupling. Remove shunt for ac-coupling.
2. Install jumper shunt on position 2-3 for SMA. Install shunt on position 1-2 for host connector.
3. Jumper pitch is 50 mil.

The jumper settings related to the oscillators are Table 3. OCXO is selected by default, which works for most default cases but may to be changed in order to test different oscillators. See "7. Reference Clock Source Configuration" on page 23 for further details and to see header pin locations.

Table 3. Oscillator Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP37	JP37	2-pin	OCXO (U2) power[1]	Installed
JP38	JP38	2-pin	TCXO/OCXO (X2, X3, X4, X5) power[1]	Open
J58	J58	3-pin	Reference select[2]	OCXO

1. Installing the jumper shunt powers on the oscillator. Removing the jumper shunt powers down the oscillator.
2. Install a shunt on 1-3 to select U2 OCXO. Install a shunt on 5-3 to select X2, X3, X4, X5 oscillator. Install a shunt on 4-3 to select the SubMiniature version A (SMA) connector.

The jumper settings related to the GPIO are described in Table 4. See "10.1. Reset Pin" on page 34 and "10.2. GPIO" on page 34 for further details and to see header pin locations.

Table 4. GPIO Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal[1]	Default Jumper Settings
JP39	JP39	2-pin	GPI0[1]	Open
JP41	JP41	2-pin	GPI1[1]	Open
JP43	JP43	2-pin	GPI21[1]	Open
JP42	JP42	2-pin	GPI6[1]	Open
JP45	JP45	2-pin	GPI3[1]	Open
JP47	JP47	2-pin	GPI4[1]	Open
JP40	-	2-pin	GPI5[1]	Open
JP44	-	2-pin	GPI7[1]	Open
JP46	-	2-pin	GPI8[1]	Open
JP48	-	2-pin	GPI9[1]	Open
JP49	JP49	2-pin	RSTb[1]	Open

1. Install the jumper shunt to assert GPIO. Remove the jumper shunt to deassert GPIO.

The jumper settings related to serial communications are described in Table 5. For further information, and to see header pin locations, refer to "9. Serial Communication and Bus Switch" on page 31.

Table 5. Serial Communications Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP50	JP50	2-pin	Host control select[1]	Open
JP51	JP51	2-pin	I2C_SEL[2]	Open
JP52	JP52	2-pin	Bus switch disable[3]	Open
J61	J61	4x3	I²C or SPI select[4]	(x4) jumpers on "SPI" side

1. Install shunt for DUT to be controlled by host connector. Remove shunt for DUT to be controlled by CBPro via a USB cable. See "7. Reference Clock Source Configuration" on page 23 for further details.
2. Install jumper to put DUT in I²C mode. Remove jumper for SPI mode.
3. Installing shunt cuts off DUT communication from both the host connector and CBPro (USB connector). Typically, this is not needed.
4. Connects DUT to an MCU SPI port or I²C port. See"7.1. Configuring OCXO/TCXO References" on page 23 for more details.

The jumper settings related to source selection for the 5 V, 3.3 V, and 1.8 V power planes are described in Table 6. For further information and to see header pin locations, see "6.1.1. Configuring the +5 V Supply Plane" on page 14 and "6.1.2. Configuring the +3.3 V and +1.8 V Supply Planes" on page 15.

Table 6. External Power Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP53	JP53	3-pin	5 V wall adapter or banana (lab) select[1]	5V_Wall
JP54	JP54	3-pin	3.3 V plane buck or banana (lab) select[2]	3V3_Buck
JP55	JP55	3-pin	1.8 V plane buck or banana (lab) select[2]	1V8_Buck

1. Install shunt on position 1-2 for wall adapter. Install on 2-3 for banana connector. See 6.1.1. "Configuring the +5 V Supply Plane," for further information.
2. Install shunt on 1-2 for buck converter. Install on 2-3 for banana connector. See 6.1.2. "Configuring the +3.3 V and +1.8 V Supply Planes," for further information.

The jumper settings related to the 3.3 V and 1.8 V buck converts are described in Table 7. For further information and to see header pin locations, see "6.1.2. Configuring the +3.3 V and +1.8 V Supply Planes" on page 15.

Table 7. Buck Converter Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP56	JP56	2-pin	3.3 V buck disable[1, 2]	Open
JP57	JP57	2-pin	1.8 V buck disable[1, 2]	Open
JP58	JP58	2-pin	3.3 V buck synchronized to external clock[2]	Open
JP59	JP59	2-pin	1.8 V buck synchronized to external clock[2]	Open

1. Install shunt to disable converter.
2. See 6.1.2. "Configuring the +3.3 V and +1.8 V Supply Planes," for further information.

The jumper settings related to the LDOs are described in the table below. For further information and to see header pin locations, see "6.1.3. Configuring Each 3.3/2.5/1.8 V VDD Pin" on page 17 and "6.1.4. Configuring Each 1.8 V-Only VDD Pin" on page 18.

Table 8. LDO Jumper Settings

Location (Neptune)	Location (Triton)	Type	Description or Signal	Default Jumper Settings
JP60	JP60	2-pin	LDO VDDO1 disable[1]	Open
J71	J71	T-shaped	VDDO1 voltage source select[2]	3-4
JP61	JP61	2-pin	LDO VDDO2 disable[1]	Open
J70	J70	T-shaped	VDDO2 voltage source select[2]	3-4
JP64	JP64	2-pin	LDO VDDO3 disable[1]	Open
J72	J72	T-shaped	VDDO3 voltage source select 2	3-4
JP65	-	2-pin	LDO VDDO4 disable[1]	Open
J73	-	T-shaped	VDDO4 voltage source select[2]	3-4
JP68	JP68	2-pin	LDO VDDIN1 disable[1]	Open
J74	J74	T-shaped	VDDIN1 voltage source select[2]	3-4
JP69	JP69	2-pin	LDO VDDIN2 disable[1]	Open
J75	J75	T-shaped	VDDIN2 voltage source select[2]	3-4
JP72	JP72	2-pin	LDO VDDIN3 disable[1]	Open
J76	J76	T-shaped	VDDIN3 voltage source select[2]	3-4
JP74	JP74	2-pin	LDO VDD18_DIG disable[1]	Open
JP77	JP77	3-pin	VDD18_DIG voltage source select[3]	2-3
JP78	JP78	2-pin	LDO VDD18A disable[1]	Open
JP79	JP79	3-pin	VDD18A voltage source select[3]	2-3
JP75	JP75	2-pin	LDO VDDHV disable[1]	Open
J77	J77	T-shaped	VDDHV voltage source select[2]	3-4
JP80	JP80	2-pin	LDO VDDIO_MCU disable[1]	Open
JP81	JP81	2-pin	LDO VDDIO_DUT disable[1]	Open
J78	J78	T-shaped	VDDIO_DUT voltage source select[2]	3-4
JP85	JP85	2-pin	LDO VDD_OCXO disable[1]	Open
J80	J80	T-shaped	VDD_OCXO voltage source select[2]	3-4
JP84	JP84	2-pin	LDO VDDREF disable[1]	Open
J79	J79	T-shaped	VDDREF voltage source select[2]	3-4

1. Install jumper shunt to disable LDO.
2. Install shunt on position 3-4 to select LDO. Install shunt on position 3-5 to select 3.3 V plane. Install shunt on position 1-3 to select 1.8 V plane.
3. Install shunt on position 2-3 to select LDO. Install shunt on position 1-2 to select 1.8 V plane.

6. Flexible Power Supply Topology

The EVB power supply tree, which powers the DUT as well as the on-board oscillators and MCU, is shown in Figure 8. The flexible design allows the user to evaluate an all-LDO configuration (the default configuration) to an all-switching configuration, or an external power supply. Multiplexing is done on a per-VDD pin basis using jumper shunts, allowing for further flexibility.

Although the EVB can accept up to four external input supplies, only a single +5 V supply is required to power the board, and selection of 5 V, 3.3 V, and 1.8 V sources is performed using jumper shunts. A +5 V wall adapter is included in the kit. A US-style plug adapter may be required.

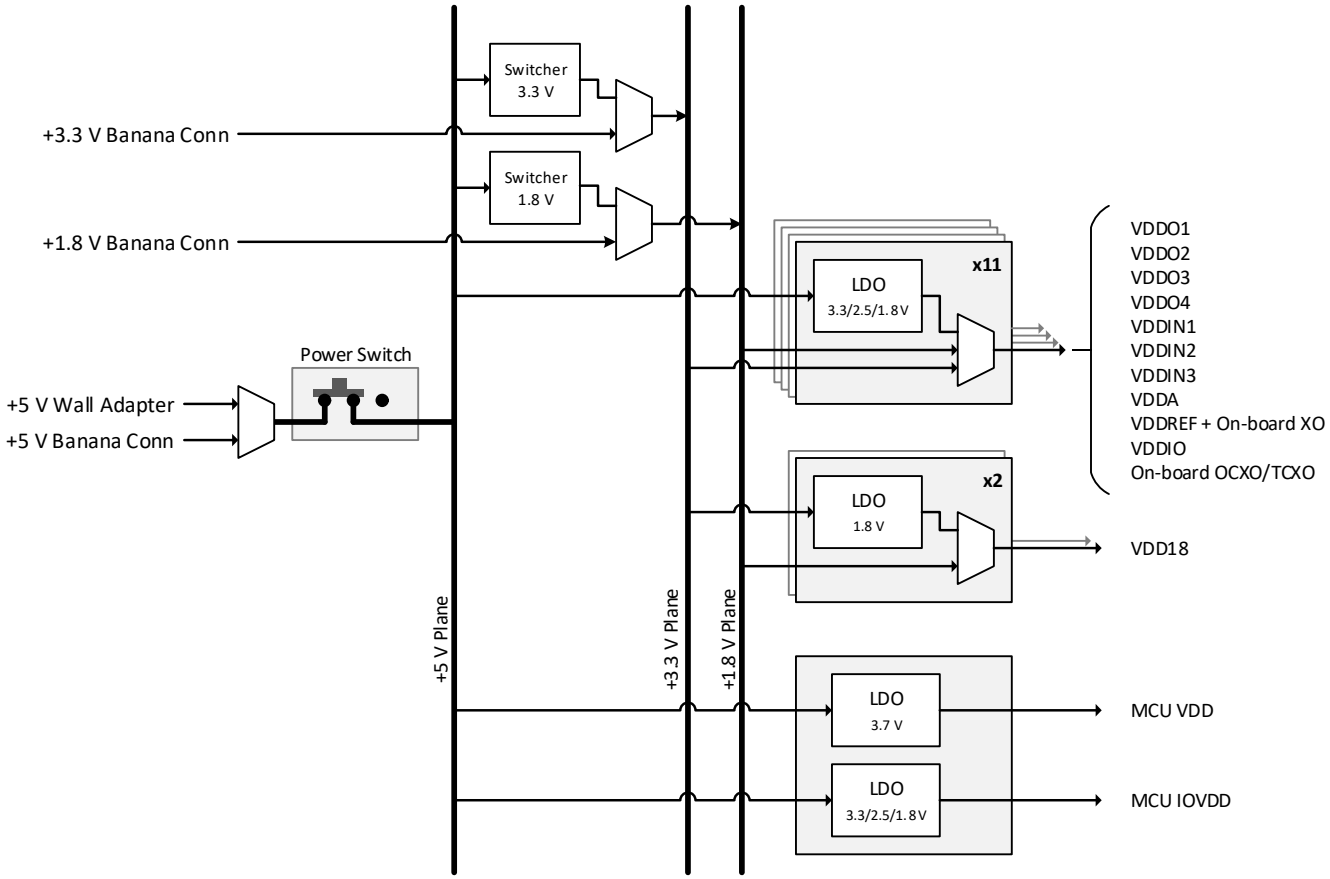

Figure 8. Power Supply Tree

"6.1. Power Supply Jumper Settings" on page 14 discusses the jumper settings related to the power supplies, and "6.2. Power Supply Use Cases" on page 18 covers the potential use cases for these features. It should be emphasized that no modifications to the default jumper settings are needed in order to start using and testing the evaluation board.

The jumper settings may only need to be changed when evaluating different power supply topologies, which comes later in the design process. See "6.2.1. Use Case #1: LDO-Only Configuration (Default Configuration)" on page 19 for the default LDO-only configuration.

6.1. Power Supply Jumper Settings

The jumper settings related to configuring the power supply are described in the following sections. There are four main parts of the power supply tree which can be configured using jumpers:

1. 5 V plane: Jumpers are used to determine whether 5 V comes from the wall adapter or banana connector.
2. 3.3/1.8 V planes: Jumpers are used to determine whether the on-board switching converters are used or an external supply is connected.
3. 3.3/2.5/1.8 V VDD pins: jumpers are used to determine whether the VDD pin is supplied by 3.3/2.5/1.8 V programmable LDO, 3.3 V plane, or 1.8 V plane.
4. 1.8 V only VDD pins: Jumpers are used to determine whether the VDD pin is supplied by 1.8 V LDO or 1.8 V plane.

6.1.1. Configuring the +5 V Supply Plane

A +5 V supply is required for the board to operate. The options and features regarding the +5 V supply are as follows:

1. J65 connector (silkscreen label “5V 3A +TIP”) wall adapter, included in the kit. This is the default method of powering the board.
2. J63/J64 standard size banana connectors for optional +5 V supply. By default, these connectors are not used, but they can be used as a substitute for J65.
3. JP53 selects which +5 V source is used.
   - Installing a jumper shunt on JP53[5V_WALL:5V] selects the wall adapter (default)
   - Installing a jumper shunt on JP53[5V:5V_LAB] selects the banana connectors
4. SW1 power switch turns the +5 V supply ON/OFF.
5. D17 LED indicates if the +5 V plane is powered.

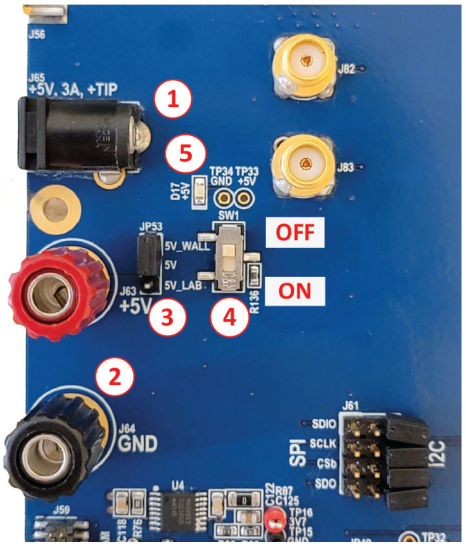

Figure 9. +5 V Supply Features

6.1.2. Configuring the +3.3 V and +1.8 V Supply Planes

The board includes onboard 3.3 V and 1.8 V switching regulators. Therefore, no external power to the +3.3 V and +1.8 V connectors are required for board use.

The options and features of the +3.3 V supply are as follows:

1. J66/J67 standard size banana connector for +3.3 V supply. By default, these connectors are not used because a 3.3 V buck converter is on the board.
2. JP54 selects whether to use the buck converter or external supply J66/J67.
   - Installing jumper shunt on JP54[3V3:3V3_BUCK] selects the switching converter (default)
   - Installing jumper shunt on JP54[3V3_LAB:3V3] selects external supply
3. JP56 enables/disables the 3.3 V buck converter. Note that CBPro (MCU) can also enable/disable the buck converter.
4. D20 LED indicates if the 3.3 V plane is powered.
5. JP58 allows the 3.3 V buck converter to be synchronized to an external clock, but doing so is not required.
   - Pin 1: ground, pin 2: clock
   - Logic low threshold: 0.8 V, logic high threshold: 2 V
   - If no clock is provided, the 3.3 V and 1.8 V converters switch at a nominal frequency of 700 kHz and 850 kHz, respectively.

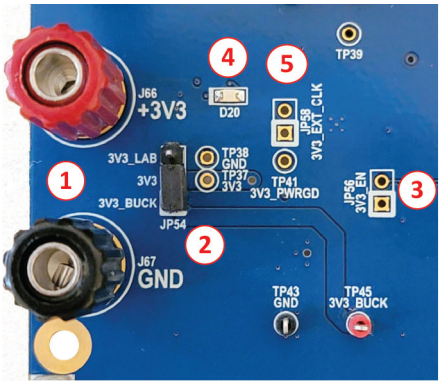

Figure 10. +3.3 V Supply Features

The +1.8 V supply is identical in design to the +3.3 V supply, and the options and features are repeated here:

1. J68/J69 standard size banana connector for +1.8 V supply. By default, these connectors are not used because a 1.8 V buck converter is on the board.
2. JP55 selects whether to use the buck converter or external supply J68/J69.
   • Installing the jumper shunt on JP55[1V8:1V8_BUCK] selects the switching converter (default)
   • Installing the jumper shunt on JP54[1V8_LAB:1V8] selects external supply
3. JP57 enables/disables the 1.8 V buck converter. Note that CBPro (MCU) can also enable/disable the buck converter.
4. D21 LED indicates if the 1.8 V plane is powered.
5. JP59 allows the 1.8 V buck converter to be synchronized to an external clock, but doing so is not required. The details of how to synchronize the converter are identical to that of the 3.3 V buck converter.

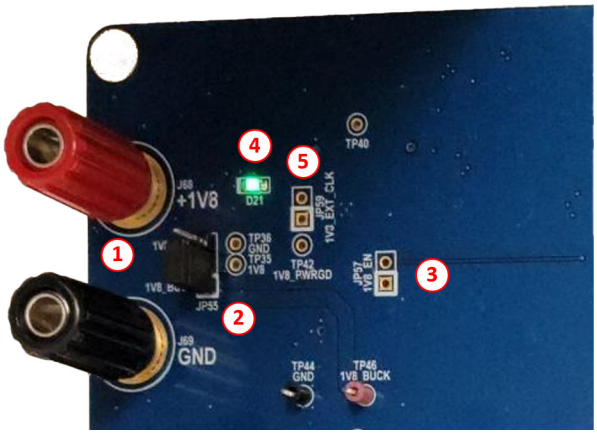

Figure 11. +1.8 V Supply Features

6.1.3. Configuring Each 3.3/2.5/1.8 V VDD Pin

The power supply pins of the DUT can be supplied by 3.3/2.5/1.8 V LDO, 3.3 V plane, or 1.8 V plane. The VDD pins for which this applies are VDDO[1:4], VDDIN[1:4], VDDA, VDDIO, VDDREF, and OCXO VDD. An example using the VDDO1 pin is provided below.

1. J71 T-header determines the source of the VDD pin.
   - Installing a jumper shunt on [VDDO1:TP51] selects the LDO
   - Installing a jumper shunt on [VDDO1:3V3] selects the 3.3 V plane
   - Installing a jumper shunt on [VDDO1:1V8] selects the 1.8 V plane
2. JP60 enables/disables the LDO. Note that CBPro (MCU) can also enable/disable the LDO.
3. TP1 is the test point for VDD pin voltage.

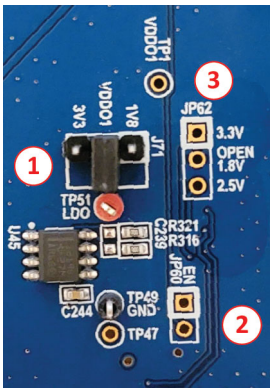

Figure 12. 3.3 V/2.5 V/1.8 V LDO Features

6.1.4. Configuring Each 1.8 V-Only VDD Pin

The VDD18 pins of the DUT require a 1.8 V supply voltage. They can be supplied either by a fixed 1.8 V LDO or the 1.8 V plane. An example using VDD18_DIG is provided below.

1. JP77 determines the source of the VDD pin.
   - Installing a jumper shunt on [VDD18_DIG_LDO:VDD18_DIG] selects the LDO
   - Installing a jumper shunt on [VDD18_DIG:1V8] selects the 1.8 V plane
2. JP74 enables/disables the LDO. Note that CBPro (MCU) can also enable/disable the LDO.
3. TP3 is the test point for VDD voltage.

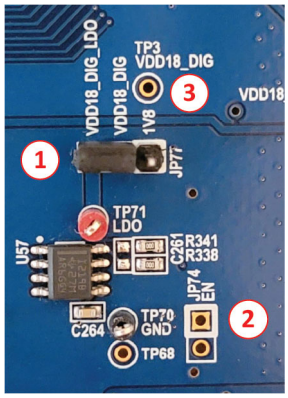

Figure 13. Fixed Voltage LDO Features

6.2. Power Supply Use Cases

The flexible power supply allows the user to evaluate various power supply topologies. Four typical use cases are presented below:

1. Use Case #1: LDO-Only Configuration (default configuration)
2. Use Case #2: Buck-Only Configuration
3. Use Case #3: Low-Power Mode
4. Use Case #4: Connecting External Power Supplies

Other use cases, such as a mix of LDOs and buck converters, can be supported with the flexible power tree.

6.2.1. Use Case #1: LDO-Only Configuration (Default Configuration)

LDOs provide lower noise than switching supplies and are the recommended method of powering NetSync and onboard oscillators. An example use case demonstrating an LDO-only configuration powered by the single +5 V wall adapter is shown in Figure 14. For the sake of simplicity, the supply for the MCU is not highlighted in the diagram.

This use case has the following features:

- A +5 V wall adapter powers the entire board
- The 3.3 V buck converter powers the 1.8 V LDOs
- All VDD pins are configured to be supplied by LDO
- The specific voltages of the programmable 3.3/2.5/1.8 V LDO may vary between frequency plans

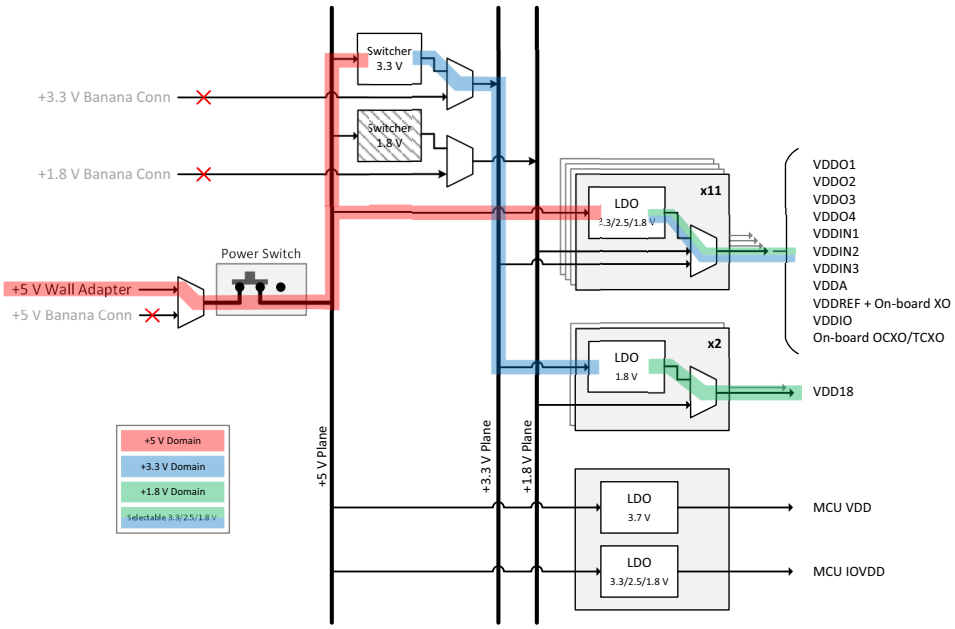

Figure 14. All-LDO Configuration Power Supply Tree

The default jumper settings described in Table 8 support this use case.

6.2.2. Use Case #2: Buck-Only Configuration

Switching supplies operate with higher efficiency than LDOs. The tradeoff is a higher noise supply in the form of voltage ripple. An example use case demonstrating an all-buck configuration powered by a single +5 V wall adapter is shown in Figure 15. For the sake of simplicity, the supply for the MCU is not highlighted in the diagram.

To configure the evaluation board for this use case for all the VDD pin supplies, configure the power supplies to select either the 3.3 V plane or 1.8 V plane according to the instructions in 6.1.3. "Configuring Each 3.3/2.5/1.8 V VDD Pin," item #1 and 6.1.4. "Configuring Each 1.8 V-Only VDD Pin," item #1.

This use case has the following features:

- +5 V wall adapter powers the entire board
- 3.3 V buck converter powers all 3.3 V VDD pins
- 1.8 V buck converter powers all 1.8 V VDD pins

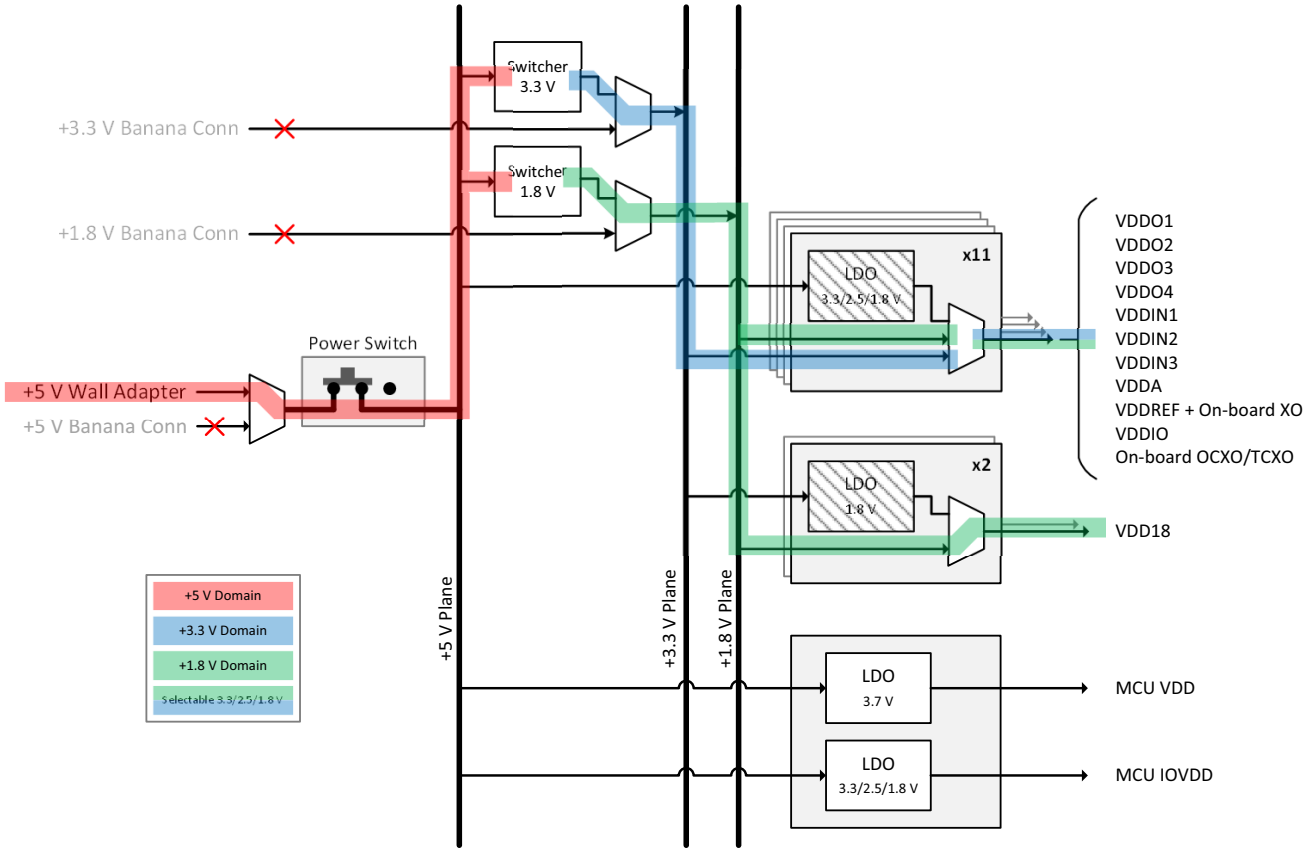

Figure 15. All-Switcher Configuration Power Supply Tree

6.2.3. Use Case #3: External Connectors

Any external lab supply can be connected to the +3.3 V or +1.8 V planes using the banana connectors. This may be useful when using an LDO/buck vendor evaluation board. An example using both +3.3 V and +1.8 V external connectors is shown in Figure 16. For the sake of simplicity, the supply for the MCU is not highlighted in the diagram.

To configure the evaluation board for this use case for all the VDD pin supplies, configure the power supplies to select either the 3.3 V plane or 1.8 V plane according to the instructions in 6.1.3. "Configuring Each 3.3/2.5/1.8 V VDD Pin," item #1 and 6.1.4. "Configuring Each 1.8 V-Only VDD Pin," item #1. Additionally, configure the 3.3 V and 1.8 V planes to select external supplies according to 6.1.2. "Configuring the +3.3 V and +1.8 V Supply Planes," item #2.

The use case has the following features:

- The +5 V wall adapter does not provide power to the DUT but is required to power the MCU and other peripheral components
- Any 3.3 V VDD pins are powered by the supply connected to the +3.3 V banana connector
- Any 1.8 V VDD pins are powered by the supply connected to the +1.8 V banana connector

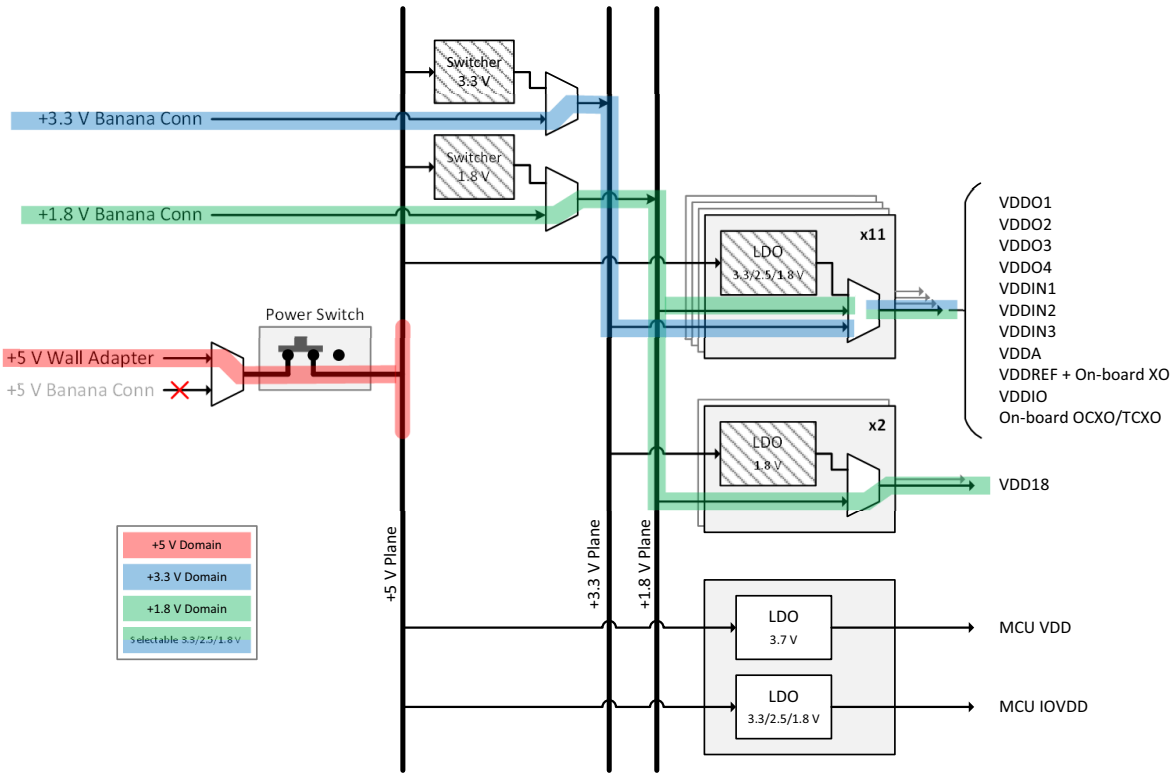

Figure 16. Power Supply Tree for External Supplies

Note that the voltages supplied to the banana connectors may be different from the nominal voltages, but should be evaluated on a case-by-case basis so that all the connected components operate properly and are not damaged. For example, a 2.5 V supply can be connected to the 3.3 V banana connectors if all VDD pins connected to that supply are 2.5 V-compatible.

6.2.4. Use Case #4: Low-Power Mode

Low-power mode refers to the use case where all supplies, with the notable exception of VDDREF, are operating at 1.8 V to minimize power consumed by the device. VDDREF must operate at either 2.5 V or 3.3 V. Typically, the LDO-only configuration can be used, with all the LDOs set to 1.8 V. However, low-power mode can also be implemented using the 1.8 V buck converter. With the default jumper settings, the supplies are controlled by CBPro and can be set to 1.8 V using the CBPro EVB GUI. No modified jumper settings are required to test low-power mode.

When all the supplies are operating at 1.8 V, any LVCMOS inputs must also be 1.8 V. This is important when using an XO/TCXO/OCXO input. The default populated oscillators on the board operate with a 3.3 V signaling level, so a resistive divider must be used to reduce the signal down to 1.8 V. R65 and C103 may form a resistive divider for U2, and R68 and C104 may form a resistive divider for X2, X3, X4, or X5.

7. Reference Clock Source Configuration

7.1. Configuring OCXO/TCXO References

Evaluating the NetSync in SyncE and IEEE 1588 PTP typically requires a stable OCXO/TCXO. Evaluating the NetSync in-line card or jitter attenuator applications typically does not require an OCXO/TCXO.

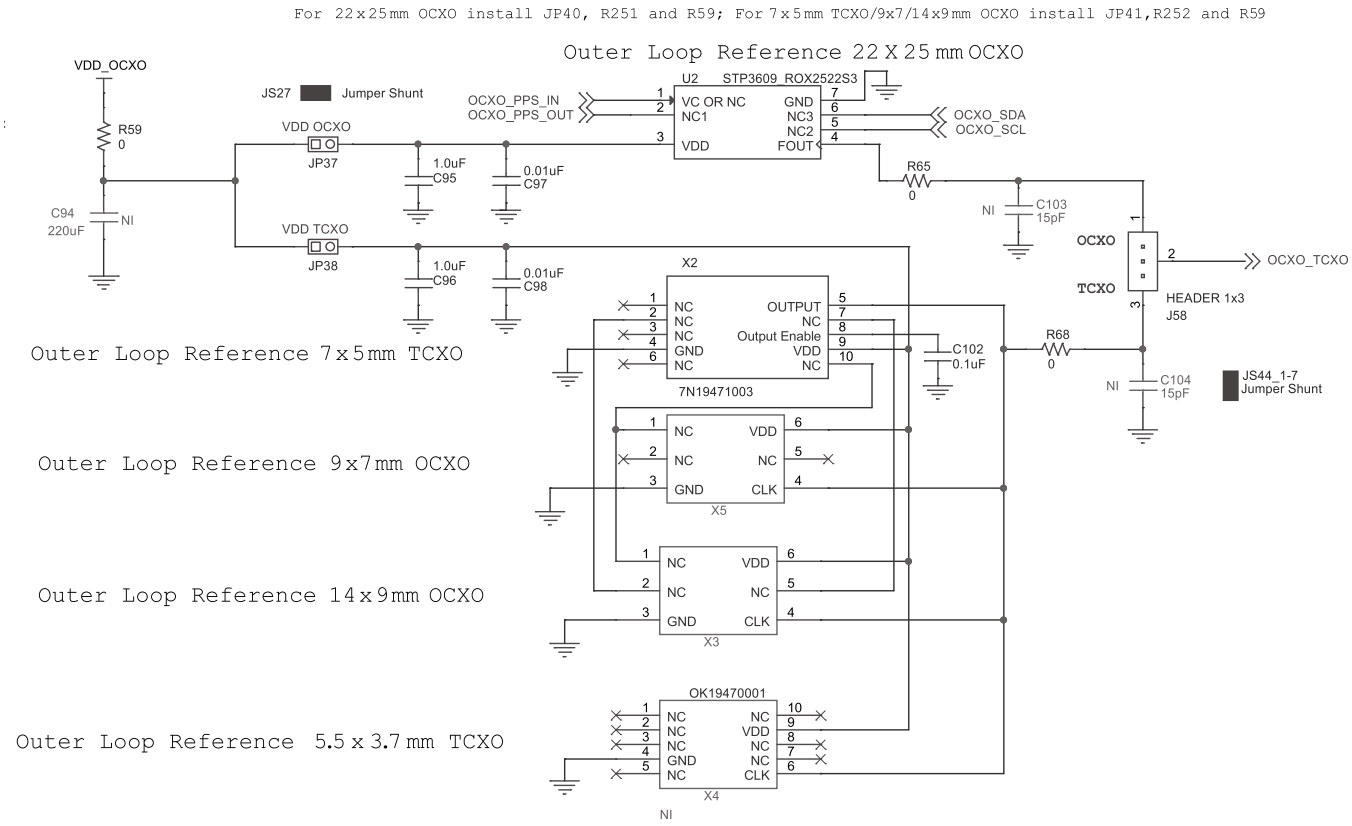

Figure 17. Schematic of OCXO/TCXO References on Neptune and Triton Evaluation Boards

The oscillator footprints supported on the Neptune and Triton evaluation board are:

- 22 x 25 mm (U2)
- 14 x 9 mm (X3)
- 9 x 7 mm (X5)
- 7 x 5 mm (X2)
- 5.5 x 3.7 mm (X4)

7.1.1. Using the 22 x 25 mm Oscillator

The Neptune and Triton boards are populated with a 22 x2 5 mm, 19.44 MHz OCXO by default. To use this oscillator:

- Install jumper on JP37
- Remove jumper from JP38
- Install jumper on JP58[OCXO:IN9]
- The default populated oscillator requires VDD_OCXO to be set to 3.3V, which is the default setting.

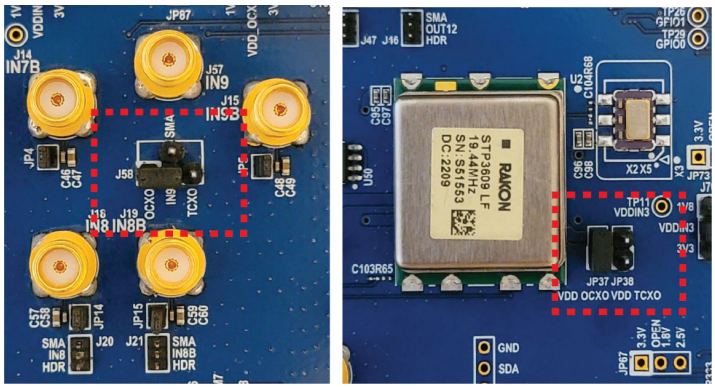

Figure 18. 22 x 25 mm Oscillator, Neptune Evaluation Board

7.1.2. Using the 14 x 9, 9 x 7, 7 x 5, and 5.5 x 3.7 mm Oscillators

The Neptune and Triton evaluation board are populated with a 19.44 MHz TCXO on X2 by default. A different oscillator can be populated on X2, X3, X4, and X5, but only one oscillator may be populated at a time. X4 is located on the back side of the board. To use this oscillator:

- Remove jumper from JP37
- Install jumper on JP38
- Install jumper on JP58[TCXO:IN9]
- The default populated oscillator on X2 requires VDD_OCXO to be set to 3.3 V, which is the default setting.

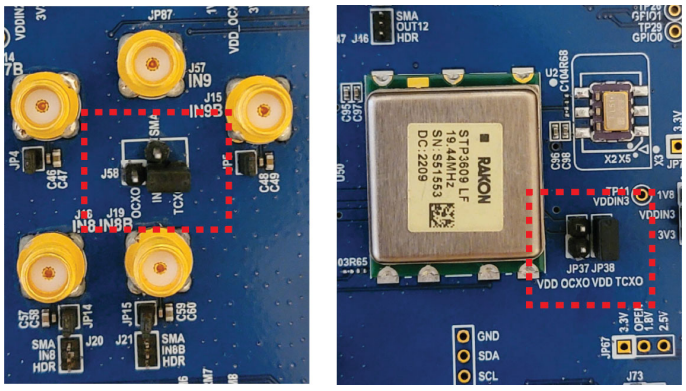

Figure 19. Small Oscillators, Neptune Evaluation Board

7.1.3. Connecting an OCXO/TCXO Using SMA

An external OCXO/TCXO may be connected to IN9 SMA (BGA) or IN8 SMA (QFN).

Neptune Evaluation Board:

- Remove R70
- Install a 0 Ω resistor on R69
- Power down the onboard OCXO/TCXO by removing JP37 and JP38

Triton Evaluation Board:

- Remove R70 and R433
- Install a 0 Ω resistor on R31
- Power down the onboard OCXO/TCXO by removing JP37 and JP38

8. Clock I/O

The EVB clock I/O is designed to support flexible functions while requiring minimal or no board rework.

8.1. Standard Clock Inputs [IN0-IN4]

By default, IN0-IN4 support ac-coupled differential clock inputs. They can be reworked to support dc-coupled LVCMOS inputs. However, doing so is typically not an efficient use of chip resources because IN5-IN9 allow both legs of the input to be utilized as independent LVCMOS clocks, whereas IN0-IN4 allows only the positive leg to be used as an independent LVCMOS clock. Typically, IN0-IN4 would be used for differential input clocks.

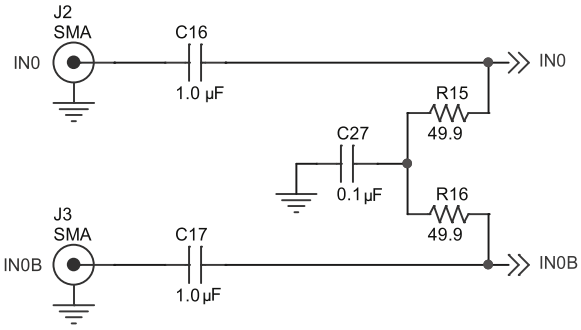

Figure 20. IN0/IN0b Schematic

Below are the instructions to reconfigure IN0 for dc-coupled LVCMOS. IN1-IN4 are configured similarly.

- Remove R15, C16, C15
- Install 0 Ω in C16.

8.2. Flexible Clock Inputs [IN5-IN8]

IN5-IN8 can support both ac-coupled differential and dc-coupled LVCMOS clocks. **CBPro automatically configures the flexible clock inputs based on the project file being written to the device and requires no manual control by the user.** Use U63/U64 to bypass the ac-coupling capacitor and enable toggling ac- versus dc-coupling (IN5/IN5b). Use U62 switching in the termination to enable toggling between terminated (differential) versus unterminated (LVCMOS). IN6-IN8 follow are configured similarly.

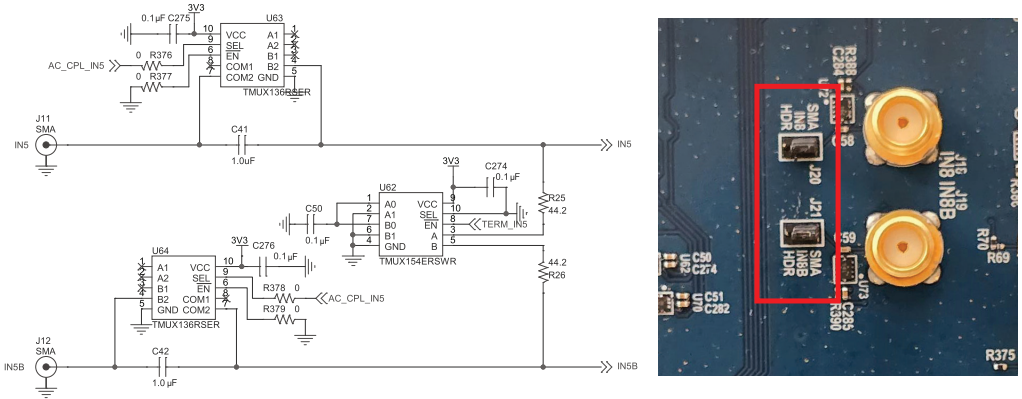

Figure 21. IN5/5b Schematic

When writing a project file to the evaluation board, CBPro automatically configures the flexible input clocks to match what was defined in the project file. However, in absence of CBPro automatic configuration, the flexible input clocks may be configured using the instructions below. IN5 is given as an example, and IN6-8 are configured similarly.

- For dc-coupling, remove jumper from JP93
- For ac-coupling, install jumper on JP93
- For Hi-Z termination, remove jumper from JP89
- For split termination, install jumper on JP89

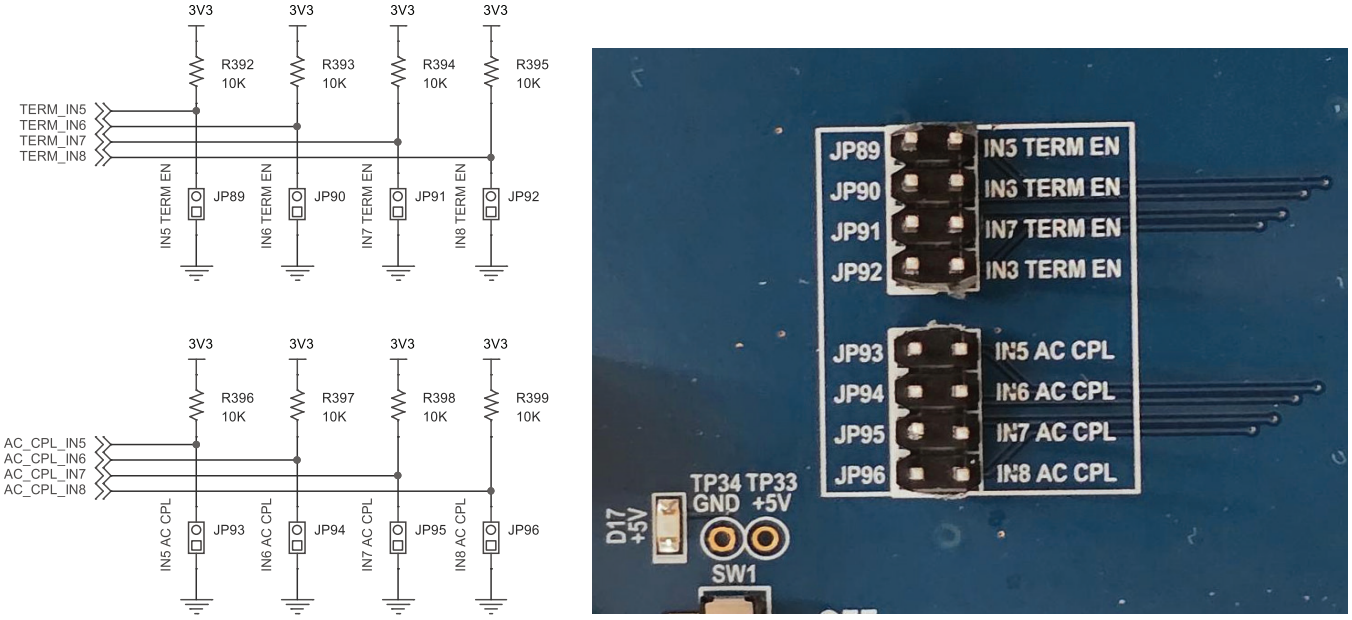

Figure 22. Jumpers for IN5-IN8

8.3. Clock Inputs from Host Connector [IN8/IN8b]

In addition to having flexible ac/dc coupling and flexible terminations, IN8/IN8B can be connected to either an SMA connector or host interface connector. The default mode of operation is to use the SMA connectors. The host interface connector may be used when evaluating the NetSync with a third party CPU EVB for AccuTime evaluation.

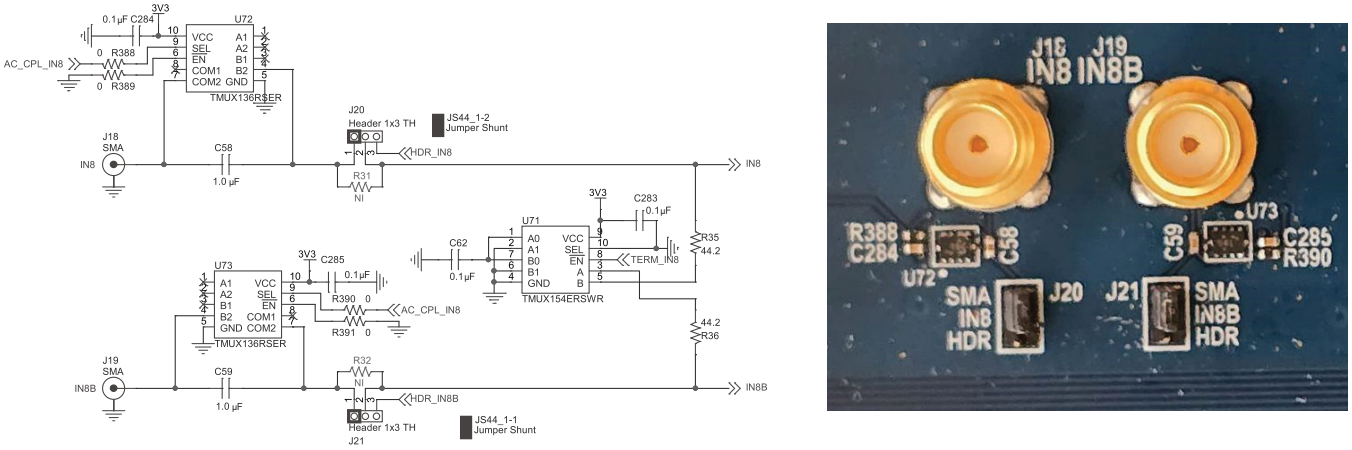

Figure 23. IN8/8b Schematic

To Configure IN8/IN8B:

- SMA connector: Install jumpers on J20[1:2] and J21[1:2]
- Host interface connector: Install jumpers on J20[2:3] and J21[2:3]

8.4. Clock Input from OCXO/TCXO

When evaluating the device, an OCXO/TCXO may be needed as described in “7.1. Configuring OCXO/TCXO References” on page 23. In the Neptune evaluation board, the onboard OCXO/TCXO may be routed to IN9. In the Triton evaluation board, it may be routed to IN8.

When evaluating jitter attenuators, these inputs may be used as a differential clock input or dual single-ended inputs since these products do not use an OCXO/TCXO. The external SMA connector may be used instead by populating R69 and removing R70.

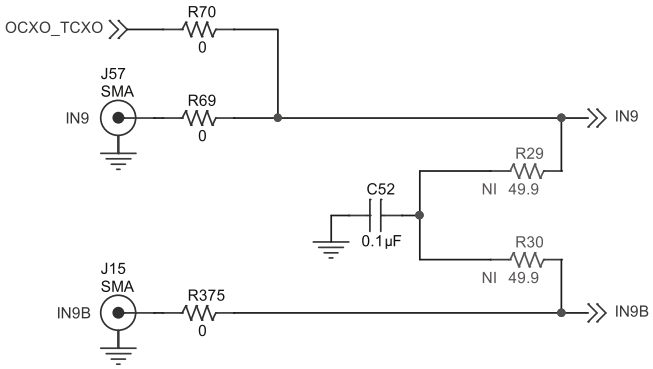

Figure 24. IN9/9b Example Schematic, Neptune Evaluation Platform

8.5. Flexible Clock Outputs [BGA: OUT0-5,12-13; QFN: OUT0-2,7-8]

OUT0-5, 12-13 for the BGA parts and OUT0-2, 7-8 for the QFN parts can support both ac-coupled and dc-coupled clock outputs.

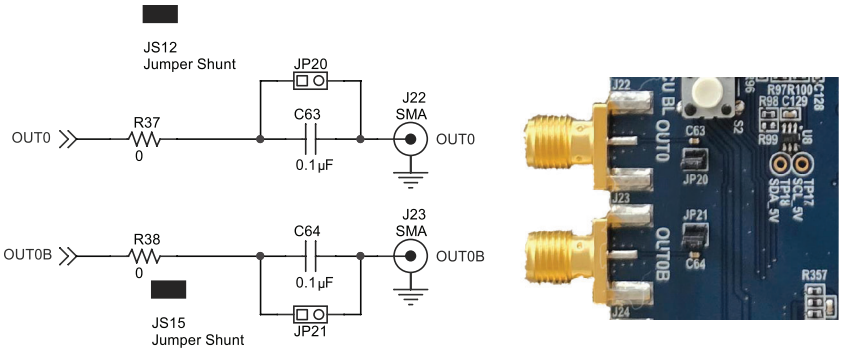

Figure 25. OUT0/0b Example Schematic, Neptune Evaluation Platform

OUT0 can be configured according to the instructions below. The remaining outputs are configured similarly.

- AC-coupled differential
  - Remove jumpers from JP20 and JP21
  - Ensure R37 and R38 are populated with 0 Ω
- DC-coupled differential
  - Install jumpers on JP20 and JP21
  - Ensure R37 and R38 are populated with 0 Ω
- DC-coupled LVCMOS
  - Install jumpers on JP20 and JP21
  - R37 and R38 may be populated with resistors according to the device reference manual for source termination. However, if signal overshoot is acceptable (e.g., during lab tests), then R37 and R38 may be left populated with 0 Ω.

8.6. Standard Clock Outputs [BGA:OUT6-11; QFN: OUT3-6]

OUT6-11 for the BGA parts and OUT3-6 for the QFN parts are configured as ac-coupled by default. In order to reconfigure for dc-coupled, the series capacitors can be replaced with 0 Ω resistors.

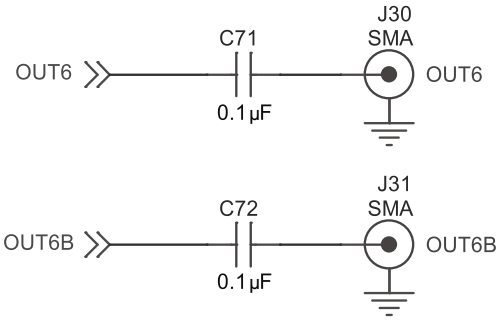

Figure 26. OUT6/6b Example Schematic, Neptune Evaluation Platform

8.7. Clock Outputs from Host Connector [BGA: OUT12-13, QFN: OUT7-8]

OUT12-13 in the BGA parts and OUT7-8 in the QFN parts can be connected to either the SMA connector or host interface connector. The default mode of operation is to use the SMA connectors. The host interface connector may be used when evaluating the NetSync with a third party CPU EVB for AccuTime evaluation.

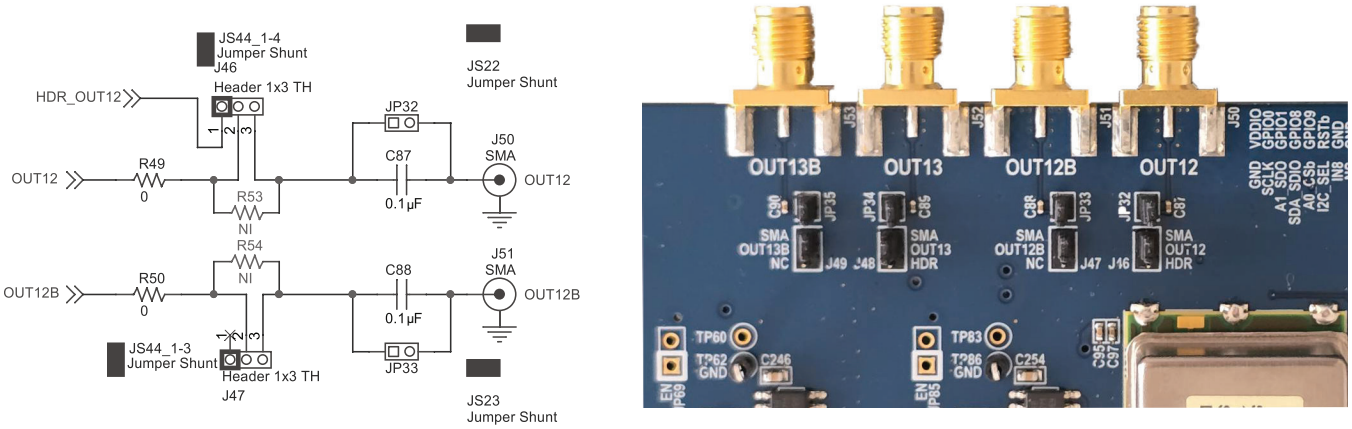

Figure 27. OUT12/12b Example Schematic, Neptune Evaluation Board

Example instructions to connect OUT12 on the BGA part to the host connector is shown below. The BGA OUT13, and QFN OUT7-8 are configured similarly.

- SMA connector: Install jumpers on J46[2:3] and J47[2:3].
- Host interface connector: Install jumper on J46[1:2]. J47 is a “don’t care.”

9. Serial Communication and Bus Switch

The EVB can be controlled by several sources:

- Default mode: Controlled by CBPro via the onboard MCU
- AccuTime mode: Controlled by the host interface connector
- Field programmer mode

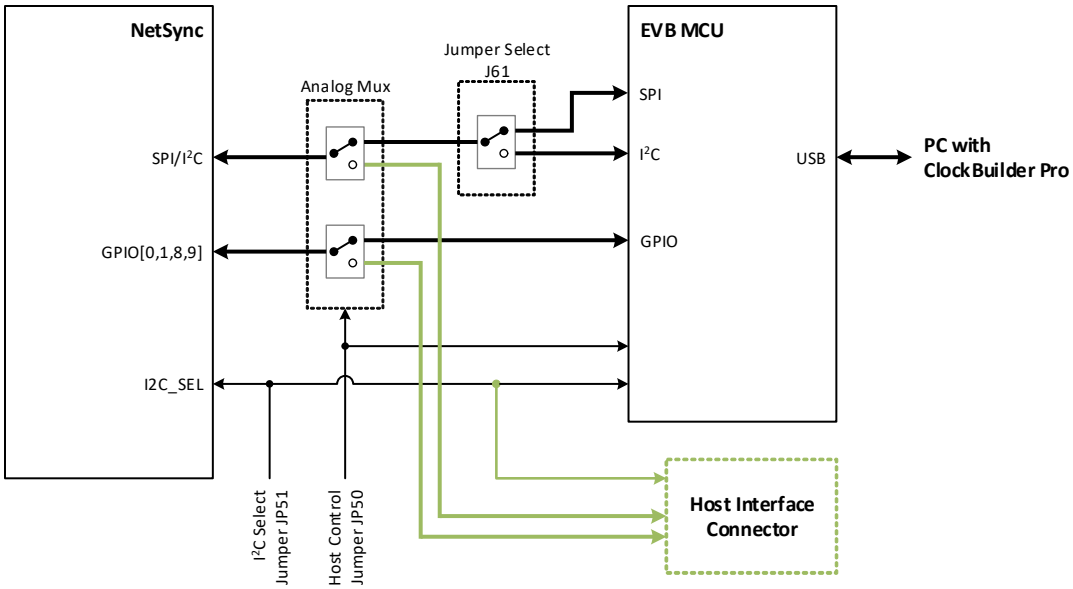

Figure 28. Serial Communication Block Diagram

9.1. Default Mode: Controlled by ClockBuilder® Pro via MCU

The default mode of operation is to have CBPro control the EVB using the onboard MCU and USB cable. Generally, this is the recommended mode because CBPro can control all components on the board such as the DUT, regulators, LEDs, and sensors. In this mode, the host interface connector is not used.

The MCU can communicate with the DUT either using SPI or I^2C. Generally, 4-wire SPI is used.

Configure the board as follows:

- SPI Mode:
  - Populate four jumpers on J61, towards the “SPI” side of the 3 x 4 header (see Figure 29).
  - Remove jumper JP51. This de-asserts the I2C_SEL pin on the DUT.
  - Remove jumper JP50. Confirm that LED D15 is off.
- I^2C Mode:
  - Populate four jumpers on J61 towards the “I^2C” side of the 3 x 4 header (see Figure 29).
  - Install jumper JP51. This de-asserts the I2C_SEL pin on the DUT.
  - Remove jumper JP50. Confirm that LED D15 is off.

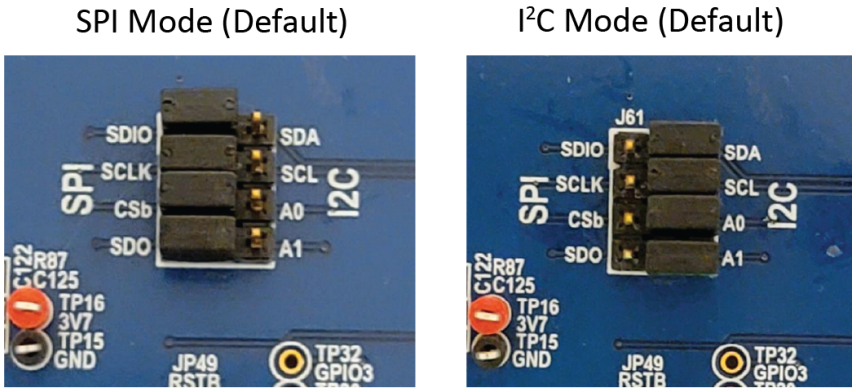

Figure 29. SPI/I²C Mode Header

9.2. AccuTime Mode: Controlled by Host Interface Connector

When evaluating the EVB in conjunction with AccuTime, a third party CPU evaluation board is required to run the AccuTime software and communicate with and program the NetSync.

Configure the evaluation board for AccuTime mode as follows:

- Install jumper JP50. Confirm that LED D15 is turned on.
- If DUT is operating in SPI mode, remove JP51. If DUT is operating in I²C mode, install JP51.

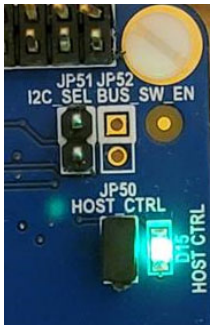

Figure 30. Host Interface Connector Selection

Note: *Although the host interface connector gives control of the DUT to a third-party CPU, the voltage regulators still need to be set to the desired levels. This is typically done by connecting the evaluation board to the CBPro EVB GUI via a USB cable and setting the voltage regulator levels in the GUI.*

9.3. Field Programmer Mode

The CBPro Field Programmer is typically used to debug devices that are already in the field. It is typically not useful when used with the Neptune or Triton evaluation boards since they contain an onboard MCU. However, connecting the field programmer to the evaluation can be useful when learning how to use the field programmer.

The field programmer can be connected to the device at multiple points. The easiest way is to remove the header pins from J61 and connecting to the middle 1 x 4 header row. However, it may be also connected to JP88 for even closer access, though it involves removing R342, R343, R344, R345, and R411 to prevent stubbing.

Note: *Although the field programmer takes control of the DUT, the voltage regulators still need to be set to the desired levels. This is typically done by connecting the evaluation board to the CBPro EVB GUI via a USB cable and manually setting the voltage regulator levels in the GUI.*

9.4. Setting VDDIO Voltage

In each of the three cases described, there must be agreement between the serial port master and DUT regarding the voltage level that is used to communicate. When using CBPro (default mode), the DUT VDDIO is always the same as the MCU I/O voltage. Therefore, no discrepancy occurs.

When using the host interface connector or field programmer, the DUT VDDIO voltage is set using the CBPro EVB GUI. However, the voltage on the master side must be set independently to match the DUT VDDIO.

10. Status LEDs and GPIO

10.1. Reset Pin

The device reset (RSTb) pin can be asserted by:

- Installing a jumper on JP49
- Using the CBPro EVB GUI
- Connecting an external CPU to the host interface connector

Asserting the pin holds the device in reset until the pin is de-asserted. This reset pin has no effect on other components on the board. When programming the device with CBPro, asserting RSTb with a jumper is typically not recommended because CBPro asserts the pin as needed.

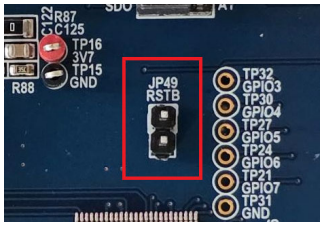

Figure 31. RSTb Header Pin

10.2. GPIO

The BGA devices have 10 GPIO status/control pins and the QFN devices have five GPIO status/control pins, each of which have programmable functions and programmable polarities. Common status functions include loss-of-lock (LOL) or interrupt (INTR). Common control functions include output enable (OE) or input select (IN_SEL).

For GPIO pins configured as status, the LED turns on when the status pin asserts. The corresponding control header has no effect. This process applies when the GPIO is configured as active-high or active-low.

For GPIO pins configured as control, installing a jumper on the header pin asserts the pin and the corresponding LED turns on. This process applies when the GPIO is configured as active-high or active-low.

Additionally, GPIO pins can be read and set from the CBPro EVB GUI software without utilizing the control header pins and status LEDs. The location of the LEDs and header pins are shown in Figure 32, and the reference designators are outlined in Table 9 and Table 10.

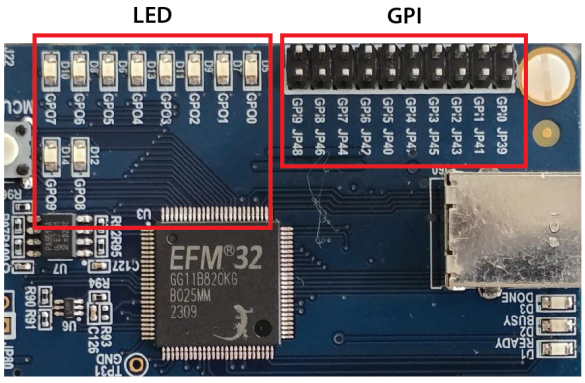

Figure 32. Neptune Evaluation Platform LED and GPI Headers

Table 9. GPI Header Pins

GPIO	Neptune Status LED (Silkscreen/Reference)	Neptune Control Header (Silkscreen/Reference)	Triton Status LED (Silkscreen/Reference)	Triton Control Header (Silkscreen/Reference)
GPIO0	GPO0/D5	GPI0/JP39	GPO0/D5	GPI0/JP39
GPIO1	GPO1/D7	GPI1/JP41	GPO1/D7	GPI1/JP41
GPIO2	GPO2/D9	GPI2/JP43	GPO2/D9	GPI2/JP43
GPIO3	GPO3/D11	GPI3/JP45	GPO3/D11	GPI3/JP45
GPIO4	GPO4/D13	GPI4/JP47	GPO4/D13	GPI4/JP47
GPIO5	GPO5/D6	GPI5/JP40	-	-
GPIO6	GPO6/D8	GPI6/JP42	-	-
GPIO7	GPO7/D10	GPI7/JP44	-	-
GPIO8	GPO8/D12	GPI8/JP46	-	-
GPIO9	GPO9/D14	GPI9/JP48	-	-

Table 10. GPO LEDs

LED	LED ON Indication	On During Normal Operation?
D17	Power applied to +5 V plane	Yes
D20	Power applied to +3.3 V plane	Yes
D21	Power applied to +1.8 V plane	Yes
D15	DUT controlled by host interface connector	No
D1	MCU ready	Yes
D2	MCU busy	Yes
D3	MCU done	Yes

11. Best Practices for Common Measurements

This section outlines several basic techniques that are useful when taking measurements on the EVB.

11.1. Phase Noise Measurements and Baluns

A balun is used when the NetSync clock output is a differential signal, but the phase noise analyzer input port is single-ended. A balun converts balanced signals to unbalanced signals and vice versa. A balun board is included in the evaluation kit. Connect differential clocks to the balanced end of the balun using phase-matched cables.

While it is possible to connect only one leg of a differential clock to the phase noise analyzer, it is generally not recommended because the measurement of interest is the clock differential phase noise, not the single-ended phase noise.

Single-ended LVCMOS clocks can be connected to the phase noise analyzer without a balun. Typically, ac-coupling is required, but this depends on the model of the phase noise analyzer being used.

11.2. Termination of Outputs

All used outputs must be terminated appropriately, even if they are not being analyzed. If differential outputs are not properly terminated, unwanted reflections occur between the load and source. This generally causes crosstalk to be more severe in phase noise measurements. For details on the recommended termination for a given output format, see the device reference manual.

For the most common differential output formats, which are LVDS and LVPECL, a 50 Ω SMA terminator should be placed on both legs of the output, with ac-coupling enabled. LVCMOS outputs should be left unterminated because they are intended to drive high impedance loads.

When taking measurements on one leg of a differential clock (e.g., oscilloscope measurements), it is important to terminate the other leg properly. Because both legs of the output driver operate as a differential pair, one unterminated leg may lead to distortion in both legs of the clock signal. For the most common differential output formats (LVDS and LVPECL), one leg can be ac-coupled to the instrument, and the other leg can be ac-coupled to a 50 Ω SMA terminator.

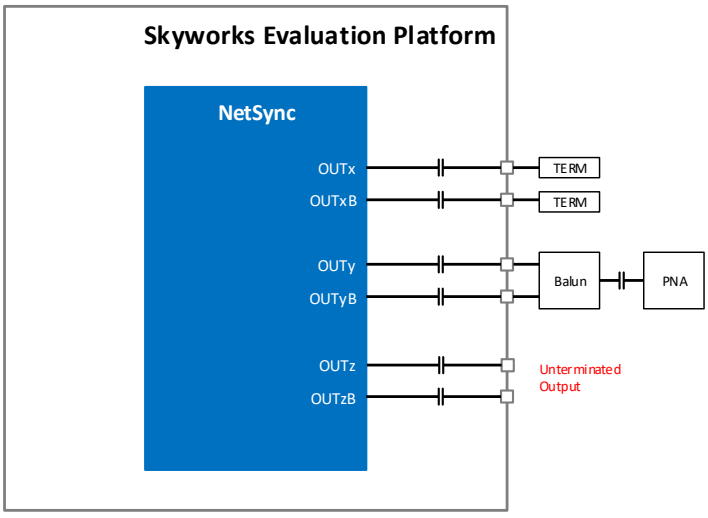

Figure 33. Output Termination Diagram

11.3. Zero Delay Mode (ZDM)

Zero Delay Mode (ZDM) externalizes the feedback path of the DSPLL® to bring the I/O delay of the DSPLL to nominally zero with a very tight tolerance. A typical application occurs when using the PPS PLL. Refer to the device reference manual for further information on ZDM.

Typically, the ZDM external feedback path is implemented using a very short trace from the chip output to chip input. However, this is not feasible using the evaluation board since the clock I/O are exposed through SMA connectors. To evaluate the ZDM performance of the NetSync, two pairs of phase-matched cables can be used (shown in green and orange in Figure 34).

If the cable pairs are perfectly matched and the channels of the lab clock generator and oscilloscope are perfectly in phase, then the clock skew displayed on the oscilloscope reflects the ZDM performance of the DUT.

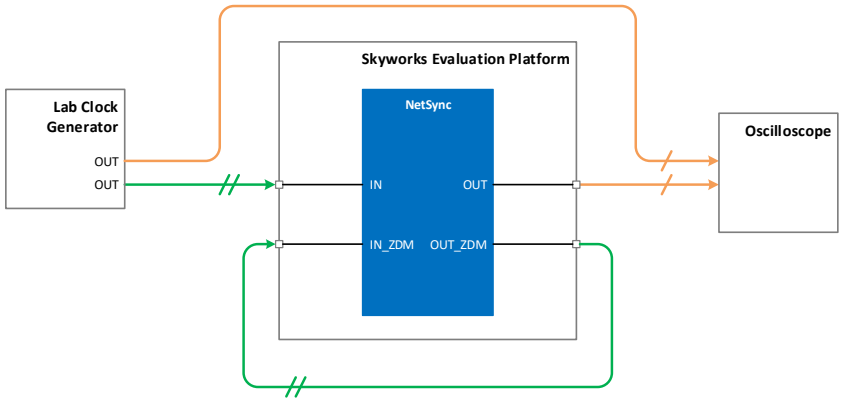

Figure 34. Zero Delay Mode Diagram

11.4. Measurement of Clock Waveform

When measuring the clock output waveform, it is important to use an oscilloscope with sufficient bandwidth to capture the clock rise and fall time. The data sheet specs describe the DUT in isolation and do not consider PCB effects. Therefore, the output clock rise and fall times may be slightly slower than what is specified in the data sheet due to the high-frequency losses in the evaluation board traces and SMA connectors. The device data sheet rise and fall times are defined using the 20 and 80 percent thresholds.

LVCMOS outputs require an external source resistance to match the total source resistance to the trace impedance. See the device reference manual for recommended resistor values. An 0402 source termination resistor can be placed on OUT0-5, 12-13 for the 144-pin BGA devices and on OUT0-2, 7-8 for the 64-pin QFN.

11.5. Measurement of Clock Skew

Measuring phase between clock outputs is important in some applications. Using an oscilloscope is often a good choice to capture the measurement. Alternatively, frequency counters may be used if they have the time interval measurement capability. However, an oscilloscope is preferred because the entire clock waveform can be observed.

In both cases, the zero-crossing voltage should be equal to the midpoint of the clock waveform. For ac-coupled clocks, this is at 0 V. Phase-matched cables should be used, and oscilloscope channel-to-channel skew should be calibrated out prior to taking the measurement in order to minimize errors due to instrumentation.

12. Ordering Information

Table 11. Ordering Options

Evaluation Platform	Part Number	Installed Clock Device	Clock Device Function	Holdover OCXO/TCXO Included?
Neptune	SKY69110BB-BGA-EVB	SKY69110	NetSync + ToD for timing card	Yes
	SKY69115BB-BGA-EVB	SKY69115	NetSync for pizza box	Yes
	SKY69120BB-BGA-EVB	SKY69120	Jitter attenuator + ToD for line card	No
Triton	SKY69112BB-QFN-EVB	SKY69112	NetSync + ToD for timing card	Yes
	SKY69116BB-QFN-EVB	SKY69116	NetSync for pizza box	Yes
	SKY69122BB-QFN-EVB	SKY69122	Jitter attenuator + ToD for line card	No

13. Revision History

Revision	Date	Description
B	July, 2026	Part numbers in Table 11 were corrected.
A	April, 2026	Initial release