Addressing Timing Challenges in 6G-SDI Applications

Introduction

Digital video transmission rates have steadily increased since the introduction of high-definition video. The latest trend in the industry for high-resolution video is the market adoption of 6G-SDI to support 4K digital cinema and ultra-high definition (UHD) television.

Digital video data delivery at higher speeds required by 6G-SDI poses new challenges in designing broadcast video production and transmission equipment. In particular, high frequency, low-jitter clocking solutions are a critical element to maintain proper signal integrity through the various components and interconnecting cables that constitute the high-definition video network. In addition, these timing solutions must be flexible enough to accommodate the multiple frequencies required by legacy video standards.

Higher Speed Video Standards on the Horizon

The Society of Motion Picture and Television Engineers (SMPTE) was founded in 1916 to standardize video content distribution. Video equipment manufacturers have since adhered to these standards. In 1997, the SMPTE established the SD-SDI 259M standard, which was the first ratified definition of a serial digital interface (SDI) to send and receive uncompressed digital video over 75-ohm coaxial cable within a studio environment. SDI supports transmission rates ranging from 270 Mbps to 360 Mbps.

Due to the fact that digitized video signals accumulate jitter across video components and interconnecting cables, SMPTE established limits on the allowable jitter content of SDI signals. As high-definition digital video advanced to 720p and 1080i, SMPTE defined the HD-SDI 292M standard to support higher bandwidth video transmission at 1.485 GB/s.

In 2005, the SMPTE introduced 3G-SDI to enable the transmission of 1080p video at 2.97 Gbps over existing 75-ohm coaxial cable. To support these higher video transmission speeds, the SMPTE has set increasingly stringent jitter requirements. Table 1 summarizes the timing requirements for the SMPTE-ratified SDI standards.

Table 1. SMPTE SDI Timing Requirements

	Example Video Format	SMPTE Standard	SDI Tx Data Rate	Sampling Clock (MHz)	Timing Jitter (pk-pk)		Alignment Jitter (pk-pk)	
SD-SDI	720x480i	259M-C	270 Mb/s	27	1 UI	3.70 ns	0.2 UI	740 ps
	960x480i	259M-D	360 Mb/s	36	1 UI	2.78 ns	0.2 UI	555 ps
NTSC/PAL	720x480p	344M	540 Mb/s	54	1 UI	1.85 ns	0.2 UI	370 ps
HD-SDI	1280x720p	292M	1.485 Gb/s	74.25, 74.25/1.001	1UI	673 ps	0.2 UI	134 ps
3G-SDI	1920x1080p	424M	2.97 Gb/s	148.5, 148.5/1.001	2 UI	673 ps	0.2 UI	67 ps

In recent years, continued technological innovation in digital video has pushed the boundaries of video resolution from 1080p (2K resolution) to 4K. Transmitting a larger number of pixels on the same infrastructure implies having to deliver the video payload at 5.97 GB/s. The goal of the standards published by the SMPTE has been to guide the increasing data transmission rates to ensure that existing video production facility infrastructure can support and broadcast higher resolution video. Although the SMPTE body has yet to ratify a standard for 6G-SDI, video equipment suppliers are already meeting the demand for 4K by introducing solutions to support the faster data rates.

Early 6G/12G-SDI Market Adoption

In response to surging interest and demand for 4K video components, broadcast video equipment suppliers are starting to release 6G-SDI compatible products such as 4K production switchers, video routers, encoders/decoders, video monitors, video servers and video converters. In addition to enabling transmission of UHD video over standard BNC cable, this equipment supports simplified switching between UHD, HD and SD formats. This enables broadcast video engineers to easily swap between different formats depending on their content production requirements. This flexibility eases the migration to UHD by enabling studios to leverage their existing investment in HD and SD equipment and continue to produce content in a variety of formats.

Semiconductor manufacturers have followed suit and have started to release ICs that are purpose-built for 6G-SDI. These devices include cable equalizers, cable drivers, reclockers and FPGAs with integrated SDI transceivers. One limitation with 6G-SDI is that 4K UHD can be transmitted at no more than 30 frames per second. Higher data rates are required to transmit video at higher frame rates.. Anticipating this demand, manufacturers are starting to release 12G-SDI components that support data rates of 11.8 GB/s.

Productization of these “proprietary” solutions increases the risk of future interoperability concerns. For this reason, the SMPTE has assembled a new Working Group to define UHD single-link, dual-link and quad-link electrical and optical SDI interfaces with nominal link rates of 6 Gb/s, 12 Gb/s and 24 Gb/s to support next-generation multi-media, high-frame-rate data transmission.

Timing Challenges for 6G-SDI

UHD video transmission creates many new hardware design challenges. There are three key timing-related design challenges affecting 6G-SDI applications.

Jitter

Excessive jitter increases the bit-error rate of the serial transmission link, degrading the quality of the video signal and potentially leading to corrupted, unrecoverable video data. Each component in the video signal chain, including cables, BNC connectors, printed circuit board traces, equalizers, reclockers, encoders/decoders, crosspoint switches and SDI transceivers, consumes a portion of the overall jitter budget.

Consider a signal chain that includes a coaxial cable, equalizer and reclocker. Typically, digital video is transmitted as an 800 mV binary digital signal on a coaxial cable. Signal losses increase with frequency on coaxial cables. To adjust for cable losses, equalizers are used to restore the original amplitude of the signal. Although equalizers are needed to maintain signal quality, they can also add jitter.

To mitigate the accumulation of jitter caused by the equalizer, reclockers are used to recover the clock from the digital video signal using a clock and data recovery circuit (CDR). A common implementation is to use a Voltage-Controlled Oscillator (VCXO) to synchronize to the recovered clock, filter unwanted jitter and re-time the output data signal. For 6G-SDI reclockers, it is critical to use low-jitter oscillators for reference timing. Starting with a low-noise reference clock enables more jitter budget to be allocated to the other components, potentially reducing their cost and complexity while simplifying PCB design.

Genclock (Timing Synchronization)

In a studio environment, all video sources are synchronized to a common reference signal from a master sync generator. This synchronization simplifies downstream video processing and switching while reducing the amount of buffering required. This process is known as "*Genlocking* the video equipment." Typically a clock generator with a low-bandwidth PLL (typically <10 Hz) is used to provide synchronous timing to the SDI serializer.

With SDI data rates increasing to 6G and beyond, it is critical that the Genlock timing generator provide a low-jitter reference clock. A rule of thumb is to select a Genlock clock that consumes no more than 20 percent of the overall timing alignment jitter budget.

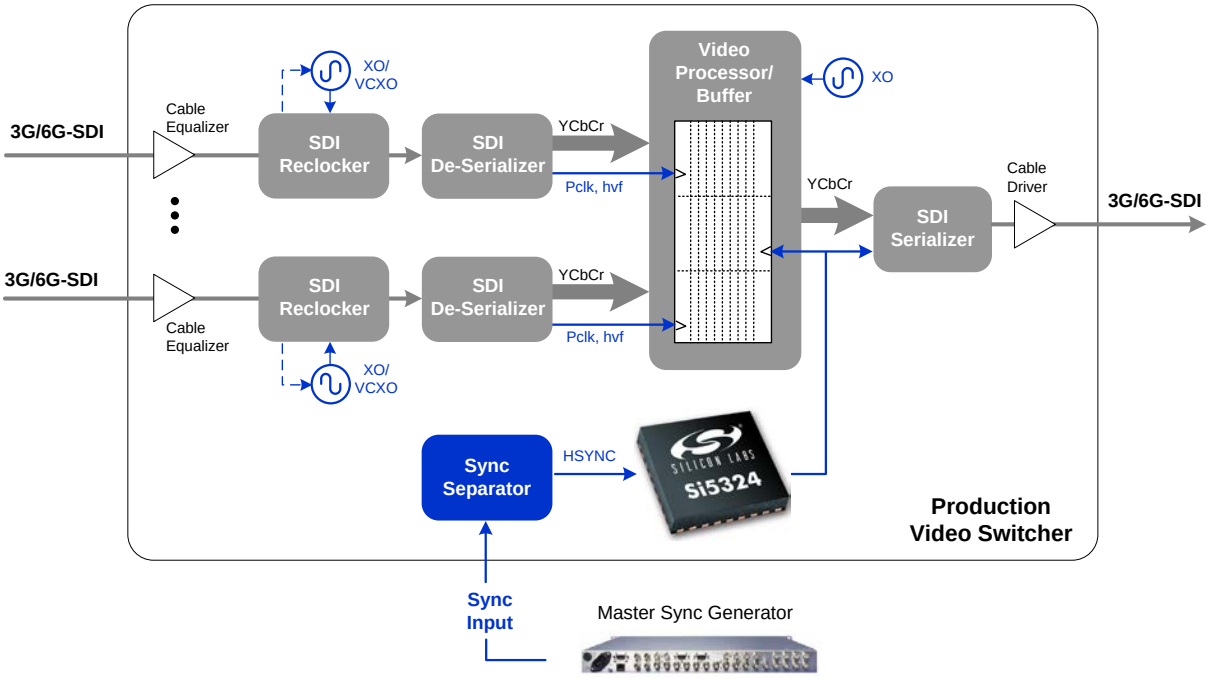

Figure 1. Example of SDI Application with Jitter-Attenuating High-Precision Clock

Frequency Flexibility

HD-SDI and 3G-SDI equipment require timing ICs to generate a combination of frequencies to support a myriad of different HDTV video formats and frame rates. Typical frequencies include 74.25 MHz, 74.25/1.001 MHz, 148.5 MHz and 148.5/1.001 MHz. This reference signal is internally multiplied within the SDI transmitter by a factor of 10 or 20 to generate the 1.485 GB/s or 2.97 GB/s signal.

Higher reference clock frequencies including 297 MHz and 297/1.001 MHz are used in proprietary 6G-SDI applications today. Using a higher frequency oscillator reference is superior to performing the additional clock multiplication within the SDI transmitter's clock multiplier unit (CMU) because discrete high performance timing devices have lower jitter than integrated PLLs used in SDI transmitters.

Low-Jitter, Frequency-Flexible Clocking Solutions for 6G-SDI/12G-SDI

The ideal clocking solutions for 6G-SDI and 12G-SDI digital video signal transmission are optimized for ultra-low jitter operation, Genlock video synchronization and frequency flexibility. In addition, the clocking solutions must be backward-compatible with 3G-SDI and other legacy video standards. The example below shows the Silicon Labs Si552 dual frequency VCXO being used as a frequency reference for a 6G-SDI

reclocker. Simple pin strapping is used to select between the 297 MHz and 297/1.001 MHz rates. Supporting jitter performance of 6.6 ps pk-pk, the Si552 VCXO maximizes jitter margin and minimizes risk in the design by shifting more jitter budget to the cable equalizer and cable driver.

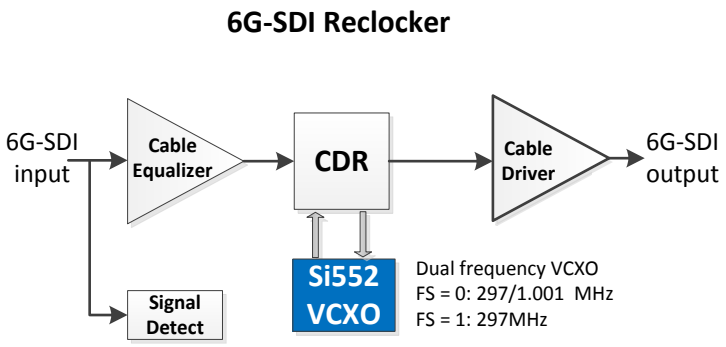

Figure 2. Low-Jitter VCXO Used in 6G-SDI Reclocker Application

An alternate solution to using a VCXO is to use a complete PLL solution. The Si5324 jitter-attenuating clock is an ideal solution for 6G-SDI Genlock clock generation. The Si5324 clock generates any output frequency from any input frequency without the need for discrete VCXOs. The frequency configuration of the device is fully programmable through I2C/SPI without the need for external BOM changes. The device has a fully integrated low-pass filter that attenuates >4 Hz timing and alignment jitter, enabling jitter filtering and timing synchronization. The Si5324 supports 5 ps pk-pk jitter performance, well below the requirements of 6G-SDI transmitters.

Summary

Continued innovation in 4K digital cinema and ultra-high definition (UHD) television increases the need for low-jitter, high-performance timing solutions. Frequency-flexible, low-jitter clocks and oscillators play a critical role in enabling the market transition to 6 Gb/s and faster data rates. Silicon Labs offers a comprehensive portfolio of frequency-flexible, low-jitter XO/VCXOs, CMEMS oscillators, clock generators, clock buffers and jitter-attenuating clocks.

Learn more about Silicon Labs' timing solutions at www.silabs.com/timing