How to Select the Right PLL-based Oscillator for Your Timing Application

Introduction

More than ten years ago, the frequency control industry introduced phase-locked loop (PLL)-based oscillators, an innovation that pioneered several features previously unavailable with traditional crystal oscillators (XOs). Leveraging internal clock synthesizer IC technology, PLL-based XOs can be programmed to support a wide range of frequencies. This breakthrough eliminated the material processing steps required to cut and machine quartz to make it resonate at a particular frequency. This innovation also made it possible for PLL-based XOs to be frequency-programmed and shipped to customers with very short lead times.

Given that traditional oscillator lead times can approach 14 weeks or longer, many hardware designers rushed to take advantage of programmable oscillators due to their significant lead-time benefit. Unfortunately, significant issues arose. Some designs that had migrated from using traditional XOs to using PLL-based XOs ran into jitter-related issues that caused application-related failures ranging from excessive bit-error rates in communication links to inoperable SoCs and processors. These issues forced many IC suppliers to specify that PLL-based oscillators could not be used in conjunction with their devices. This turn of events made it challenging for hardware designers to take advantage of the frequency flexibility and short lead benefits offered by PLL-based oscillators.

Why did this happen? It turns out that PLL technology varies widely from supplier to supplier. A sub-optimal PLL design leads to excessive oscillator phase noise and jitter peaking as shown in the left-hand diagram of Figure 1. The phase jitter of this particular PLL-based XO was measured as being 150 ps RMS integrated over the 12 kHz to 20 MHz band. This level of performance makes it unsuitable for clocking high-speed PHYs, which typically require <1 ps RMS jitter references. The period jitter of the XO is shown in the right-hand diagram of Figure 1. This bimodal period jitter may be a sign of a PLL stability issue that could have a detrimental performance impact on the SoC using this XO. A second area of concern with programmable oscillators that exhibit jitter peaking is cascaded PLLs. When such a PLL-based oscillator is connected to an IC with a PLL in a subsequent circuit, jitter may increase.

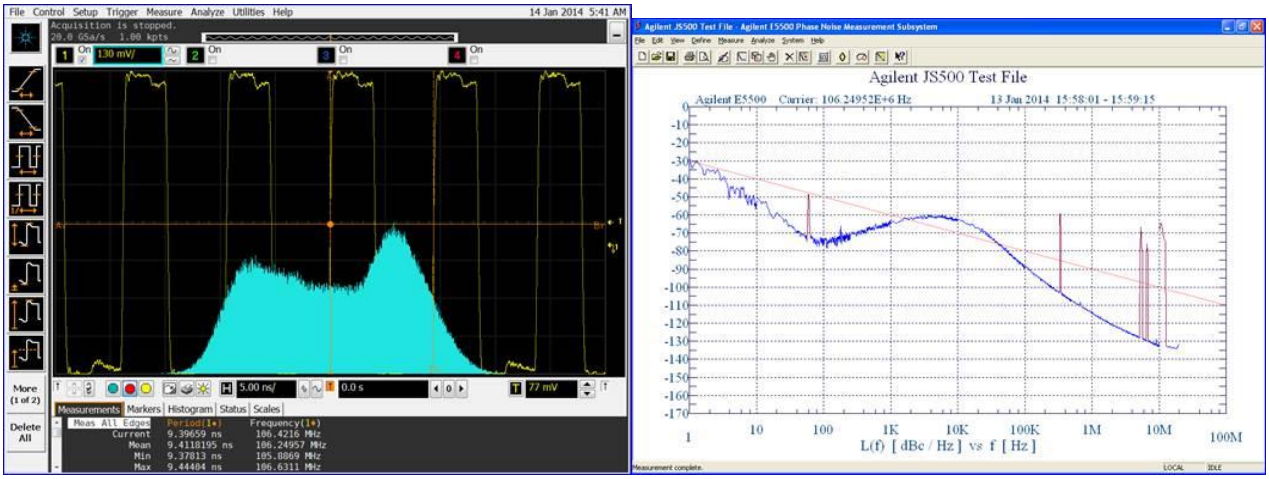

Figure 1. Example Sub-optimal PLL-based XO Phase Noise and Period Jitter

The good news is that not all PLLs, and certainly not all PLL-based oscillators, are created equal. With proper PLL design techniques, programmable oscillators can deliver jitter performance rivaling best-in-class quartz oscillators while addressing the issue of cascaded PLLs. These high-performance PLL-based oscillators can be used for processor/SoC clocking as well as clocking high-speed serializers, PHYs and FPGAs.

Developers can use three simple criteria to evaluate if a PLL-based XO can be used in a given application.

Jitter Generation

In cascaded PLL applications such as FPGA and PHY clocking, the XO reference clock jitter is compounded with the FPGA/PHY's internal PLL jitter. Starting with a low-jitter XO reference (e.g. <<1 ps RMS phase jitter) maximizes the amount of tolerable jitter than can be generated by the FPGA/PHY's internal PLL, maximizing margin in the overall design.

Jitter Peaking

Cascading PLLs run the risk of excessive jitter due to jitter peaking when the loop bandwidth of the first-stage and second-stage PLLs are the same. This risk is easily mitigated by using a PLL-based oscillator with a relatively low internal PLL bandwidth. The PLL should be well damped to ensure less than 1% peaking (<0.1dB). The bandwidth of second-stage PLLs in common SoC/FPGAs is typically >1 MHz. Using a PLL-based oscillator with low jitter peaking and a much lower internal bandwidth ensures that its peaking won't overlap with the downstream PLL's bandwidth. This architecture enables the second-stage PLL to easily track changes in the first-stage PLL while maintaining acceptable loop stability and phase margin.

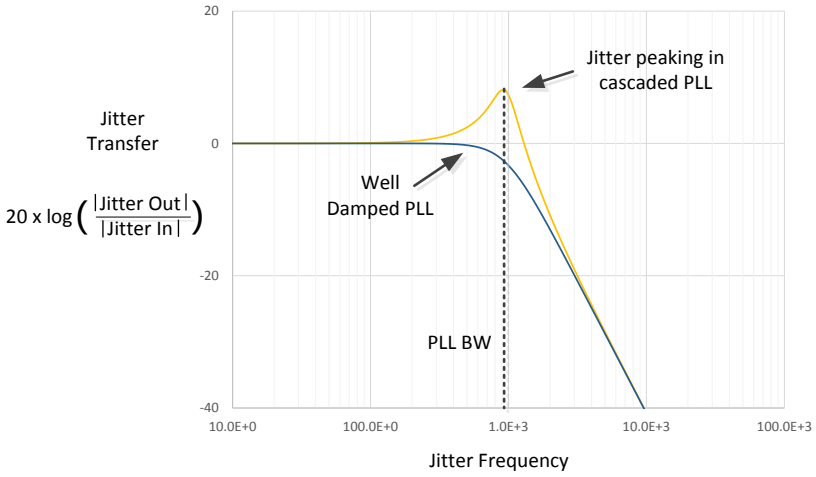

Figure 2. PLL-Based Jitter Tracking and Filtering

Phase Noise

How do you know if a PLL-based oscillator will work in your application? The oscillator period jitter can be easily observed using an oscilloscope. Oscillator phase noise can be measured using a spectrum analyzer. If you do not have access to a spectrum analyzer, contact your frequency control supplier for phase noise measurements. Phase jitter can be calculated directly from the phase noise plot by using the relevant jitter integration bandwidth required by the application. Phase noise plots also show the spurious performance of the reference clock. The spurious contribution to phase jitter can be easily measured to ensure the application's requirements are met. The phase noise plot will also show any peaking effects of the internal PLL. Overdamped PLLs will exhibit low peaking.

When selecting an oscillator, an important consideration is power supply noise filtering. Oscillators with internal power supply voltage regulation provide noise rejection, enabling more resilient operation by ensuring the device does not violate its stated jitter specifications when subjected to system-level noise.

Silicon Labs Si5xx Crystal Oscillators

Silicon Labs' Si5xx crystal oscillators leverage proprietary DSPLL technology to generate any frequency from 100 kHz to 1.4 GHz. DSPLL-based oscillators are designed to be overdamped with low jitter peaking (<0.1 dB). The internal PLL bandwidth of DSPLL-based oscillators is ~300 kHz, enabling usage in PLL-based high-speed serializer applications such as OTN, DWDM, 10GbE/40GbE/100GbE, SONET/SDH, 3G SDI and 6G SDI applications. Figure 3 shows the typical phase noise performance of Silicon Labs' XOs.

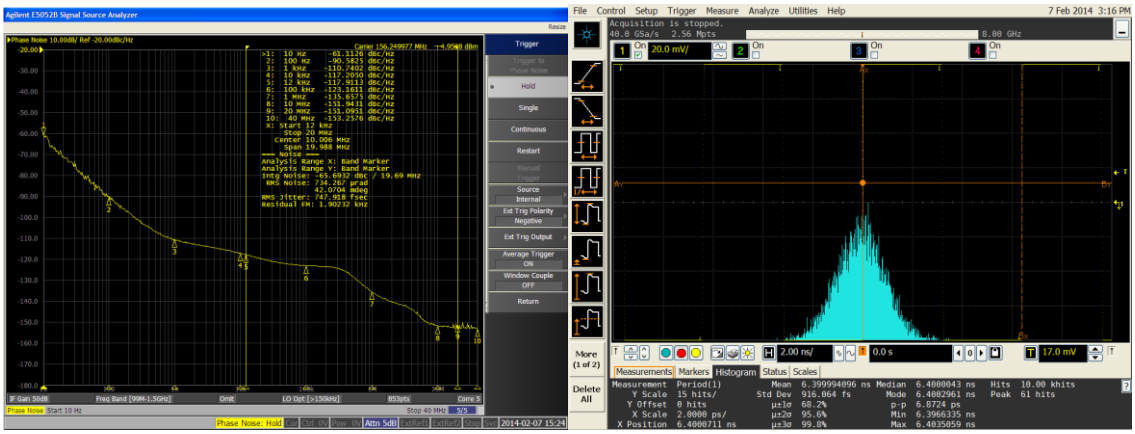

Figure 3. Silicon Labs Si510 Phase Noise and Period Jitter ($f_{CARRIER}$ = 156.25 MHz)

Multiple XO product families are available from Silicon Labs ranging in phase jitter performance from 0.2 ps RMS to 0.8 ps RMS. Contact Silicon Labs to request phase noise or period jitter measurements for any frequency and any device. Si5xx samples are available with 2-week lead times and can be requested at the following link: http://www.silabs.com/products/clocksoscillators/Pages/utilityintro.aspx

XO Product Family	Frequency Range	RMS Phase Jitter (12 kHz to 20 MHz)	Internal PLL Bandwidth
Si51x	0.1 to 250 MHz	0.8 ps	300 kHz
Si53x	10 to 1400 MHz	0.2~0.3 ps	300 kHz
Si57x (I2C prog.)	10 to 1400 MHz	0.3 ps	300 kHz
Si59x	10 to 800 MHz	0.5 ps	300 kHz

Table 1. Silicon Labs Crystal Oscillators

Learn more about Silicon Labs' timing solutions at www.silabs.com/timing

Silicon Labs invests in research and development to help our customers differentiate in the Internet of Things, Internet Infrastructure, industrial and broadcast markets with innovative low-power, small size, analog intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.