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# Simplify Timing Architectures with Flexible Clocks

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## Introduction

Due to the wide diversity of frequency and jitter requirements of the reference clocks required in modern electronic systems, an assortment of standalone crystal oscillators and fixed-frequency clock multiplier ICs are typically required to provide a complete timing architecture for both the data path and control plane. The Si5338 is the industry's first clock generator capable of supporting any-rate frequency synthesis on four independent output clocks. By providing this level of frequency flexibility, the Si5338 eliminates the need for fixed-frequency clock generators and discrete crystal oscillators.

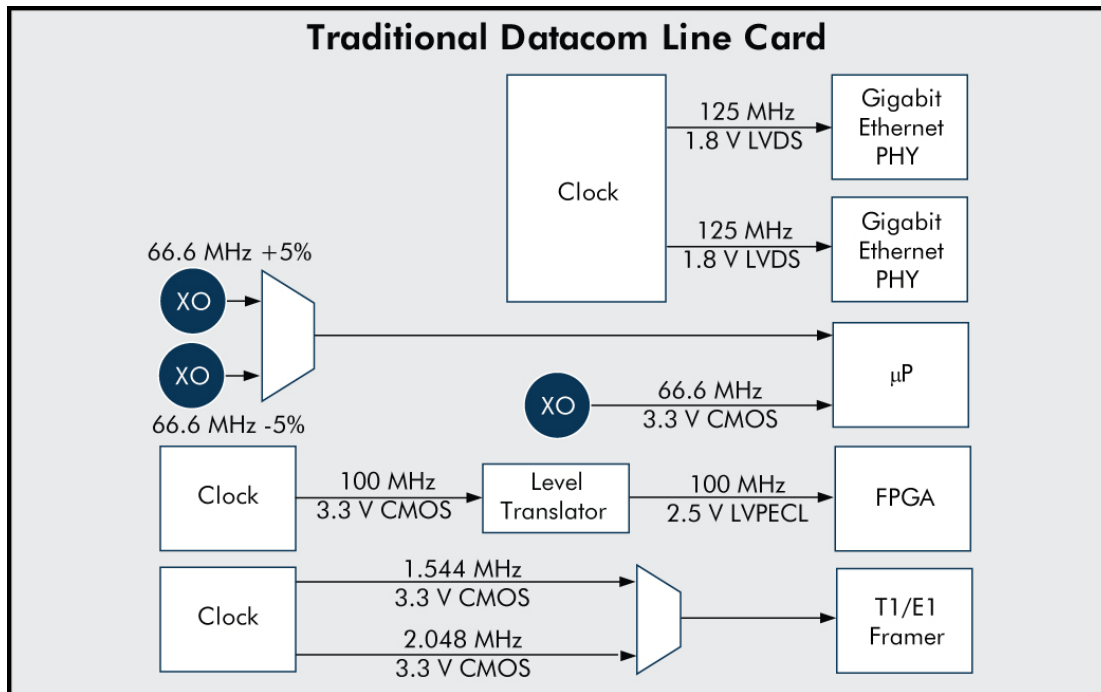
Modern communication, networking, and broadcast video hardware designs use a wide variety of processors, FPGAs, memory, and physical layer transceivers to perform all of the tasks and processes required by end applications. The timing architecture in these applications is becoming increasingly complex due to the growing level of integration required in new designs. Each IC has its own unique reference clock requirements and multiple clock domains must be carefully managed in a single design. Further complicating hardware design, high-speed physical layer transceivers and FPGAs with embedded serializer/deserializers (SERDES) have stringent jitter requirements to ensure compliance with the end applications' bit-error rate (BER) specifications.

Table 1 shows the broad range of typical clock frequencies required by processors, memory, and physical layer transceivers in popular communication, networking, and broadcast video applications.

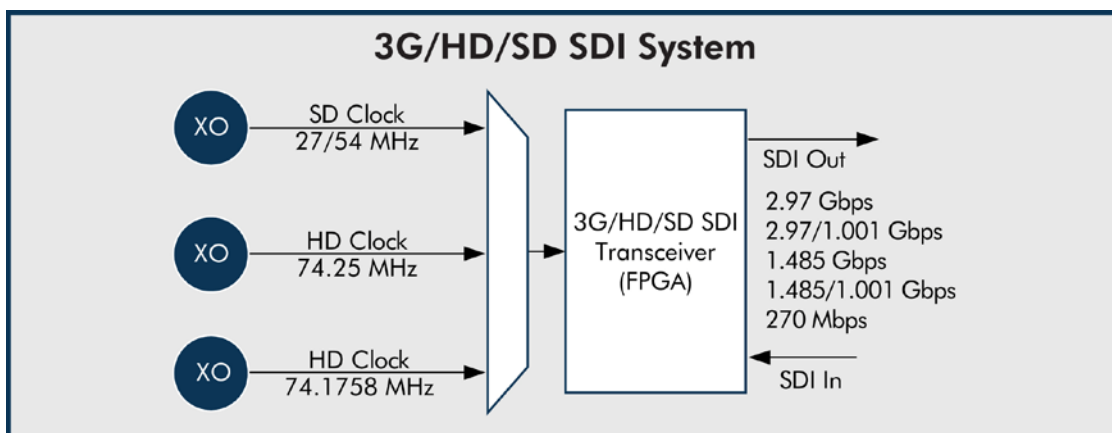
| Component                     | Typical Reference Clock (MHz)  |
|-------------------------------|--------------------------------|
| Processors/Network Processors | 33.33, 66.66, 100, 125, 133.33 |
| Memory                        | 100, 133, 166, 200, 266        |
| Fast Ethernet                 | 25                             |
| Gigabit Ethernet              | 125                            |
| Fibre Channel                 | 106.25                         |
| PCI Express 2.0               | 100                            |
| xDSL                          | 35.328, 70.656                 |
| SONET/SDH OC-3/STM-1          | 77.76                          |
| SONET/SDH OC-12/STM-4         | 155.52                         |
| HD-SDI                        | 74.1758, 74.25                 |
| 3G-SDI                        | 148.3517, 148.5                |
| T1                            | 1.544                          |
| E1                            | 2.048                          |

**Table 1.** Typical Clock Frequencies by Application

Examples of traditional timing architectures providing clock generation and clock distribution in the end application as shown in Figures 1 and 2.



**Figure 1.** Traditional Timing Architecture in Communication and Networking Applications



**Figure 2.** Traditional Timing Architecture in Broadcast Video Applications

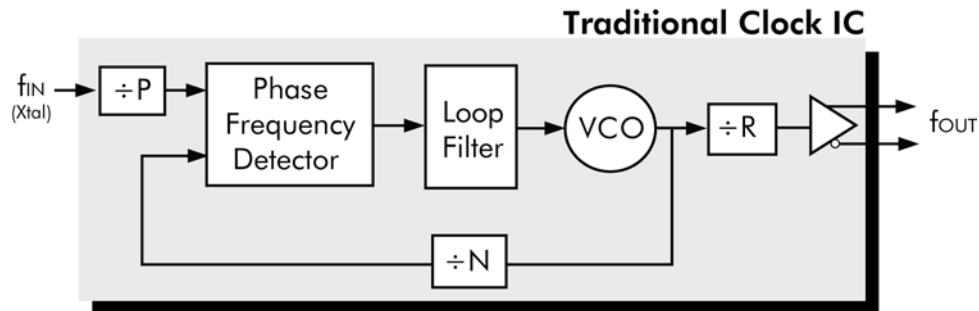
Given the unique requirements of each hardware design, the timing architecture is typically customized for each application using a combination of fixed-frequency clock generators/multipliers, discrete crystal oscillators, and muxes. Additional level translator ICs are necessary when clock format translation is required between the clock generator and the IC. Some applications require multi-protocol high-speed serial data transmission, as shown by the HDTV broadcast video example in Figure 2 above. These applications require multiple oscillators and supporting mux circuitry to support the application's multi-protocol requirements.

In addition to generating nominal clock frequencies, some applications require frequency-margined clocks that produce references that are at a slight positive or negative offset to the nominal frequency (e.g., 66.6 MHz  $\pm$ 5%). These frequency-margined clocks are used during product validation and/or manufacturing test to test the robustness of the design over voltage and temperature and ensure sufficient setup and hold margin for the critical components in the system. Traditionally, frequency margining has been implemented using discrete custom frequency oscillators. Since these additional components are exclusively used during product validation and/or manufacturing test and not during normal operation, BOM cost and complexity are increased to support this requirement.

### Traditional Clock Multiplier Architecture

Traditional clock generators use a simple integer-N phased-locked loop (PLL)-based architecture. The output clock frequency is a function of the input clock frequency and the PLL divider values as shown in the equation and Figure 3:

$$f_{OUT} = \frac{f_{IN} \cdot N}{P \cdot R}$$

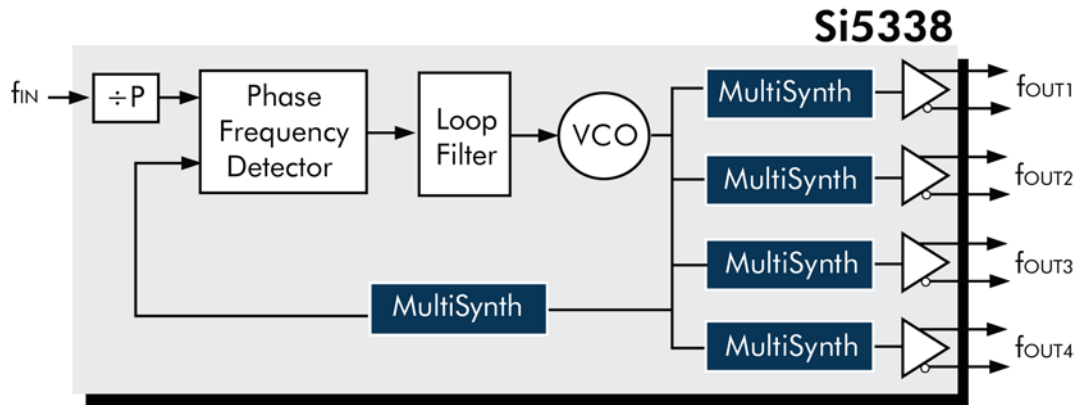


**Figure 3.** Traditional Integer-N PLL Clock Architecture

Traditional single PLL-based IC solutions are suitable for simple integer clock multiplication of reference inputs or clock generation from crystal inputs. However, many applications require clock generation of multiple non-integer-related frequencies (e.g., 125 MHz Ethernet and 106.25 MHz Fibre Channel). Traditional solutions require that the crystal frequency be changed to support each unique frequency plan. This forces the designer to use one or more custom crystals and multiple clock generator ICs to generate the required set of frequencies, increasing the cost, complexity and power consumption of the overall solution.

### New Any-Rate Clock Multiplier Architecture Simplifies Design

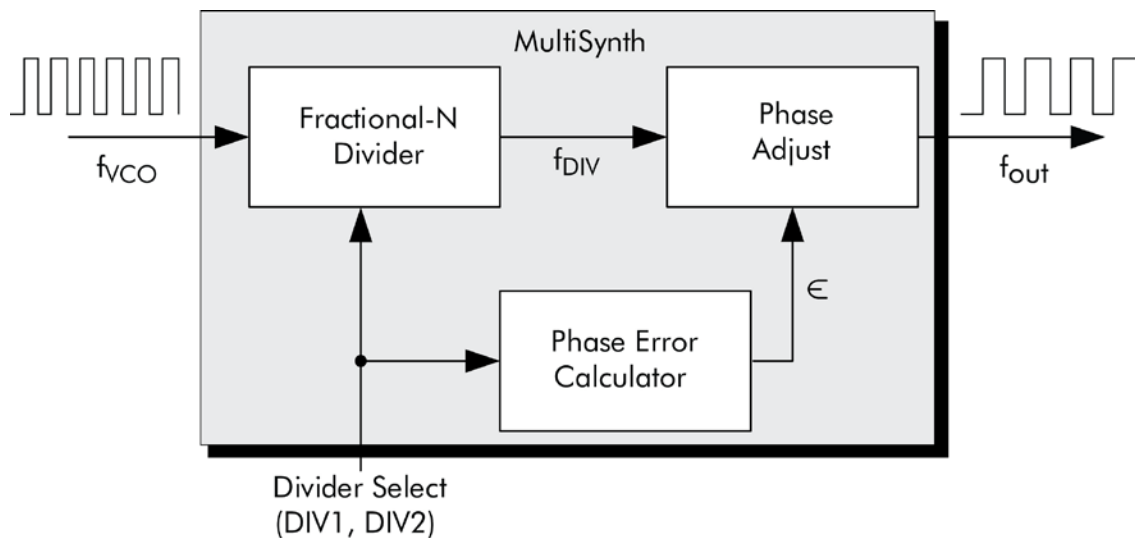
Recent advances in mixed-signal analog design have made it possible to provide any-rate frequency synthesis from a single device. As shown in Figure 4, Silicon Labs' newest clock architecture leverages a fractional-N PLL used in concert with a low-jitter fractional divider termed MultiSynth to produce any-rate frequency synthesis on multiple output clocks. The flagship of this new product family is the Si5338 Any-Rate, Any-Output Quad Clock Generator. This technology dramatically simplifies timing architectures by integrating the frequency synthesis capability of four PLLs in a single device, greatly reducing size and power requirements compared to traditional solutions.



**Figure 4.** Si5338 Any-Rate, Any-Output Clock Generator Architecture

### MultiSynth Technology

Figure 5 shows a detailed block diagram of the MultiSynth fractional divider. The Si5338's low phase noise, high-frequency VCO supplies a high-frequency output clock to the MultiSynth block on each of the four independent output paths. The first stage of the MultiSynth architecture is a fractional-N divider, which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, the MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance. Based on this architecture, each output clock can be individually programmed to generate any frequency from 0.16 to 350 MHz, and select frequencies to 700 MHz. Typical jitter performance enabled by this MultiSynth-based architecture is 1 ps RMS.



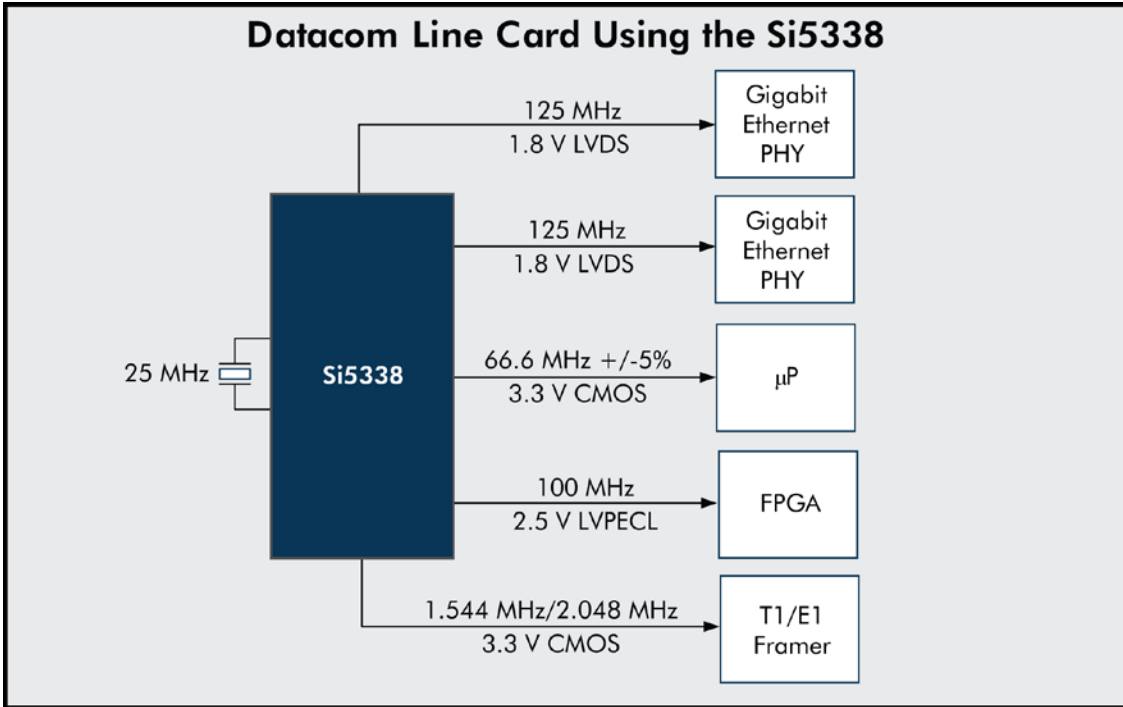
**Figure 5.** MultiSynth Architectural Overview

This MultiSynth-based architecture provides excellent jitter performance as summarized in Table 2.

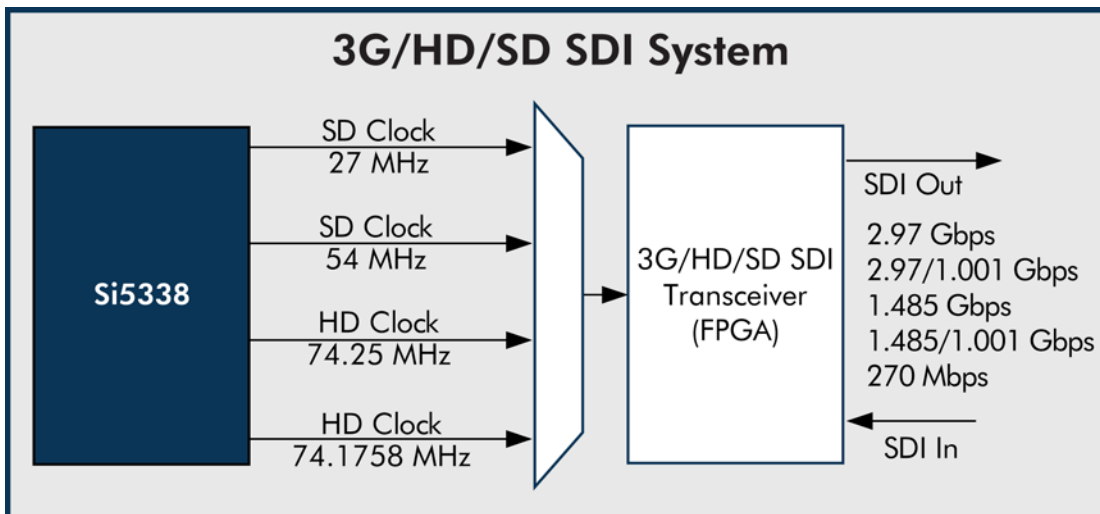
| Parameter                              | Test Condition                          | Max Jitter  |
|--|---|-------------|
| Random Phase Jitter (12 kHz to 20 MHz) |   | 1.5 ps RMS  |
| Deterministic Phase Jitter             | MultiSynth producing fractional divisor | 15 ps pk-pk |
|  | MultiSynth producing integer divisor    | 10 ps pk-pk |
| Total Jitter (12 kHz to 20 MHz)        | MultiSynth producing fractional divisor | 36 ps pk-pk |
|  | MultiSynth producing integer divisor    | 20 ps pk-pk |
| Cycle-Cycle Jitter                     | N = 10,000 cycles                       | 50 ps pk-pk |
| Period Jitter                          | CLKIN = 25 MHz<br>All CLKns at 100 MHz  | 30 ps pk-pk |

**Table 2.** Si5338 Any-Rate, Any-Output Clock Generator Jitter Performance

This level of jitter performance makes it possible to consolidate data path and control plane clocking into a single device as shown in Figures 6 and 7. In addition to dramatically simplifying BOM cost and complexity, power savings of 50% or more can be realized by migrating to this new solution. Board space is also minimized since multiple components are replaced with a single IC packaged in a small 4x4 mm 24-QFN package.



**Figure 6.** Si5338 Simplifies Communication and Networking Timing Architecture



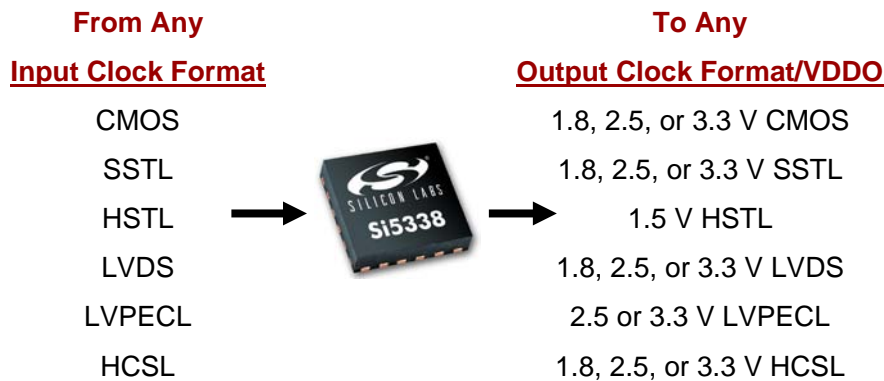
**Figure 7.** Si5338 Simplifies Broadcast Video Timing Architecture

### Frequency Margining for Board-Level Test

Frequency margining is greatly simplified using this approach because the MultiSynth's fractional divider value can be changed dynamically such that the clock output produces a variable clock source. All frequency transitions are continuous and glitchless. Frequency transitions as small as 1 kHz and as large as 10 MHz are possible using this architecture. The frequency of each output clock can be changed dynamically for any frequency up to 350 MHz. As a result, standalone crystal oscillators traditionally used for board-level test can be eliminated.

### Integrated Level Translation

The signal format of each Si5338 output clock is user-programmable to any of the options listed in Figure 8. This functionality eliminates the need to use external level translators in most designs. Further, use in mixed-supply applications is simplified since every Si5338 output clock has an independent supply voltage. Each of the device outputs can be programmed to support any output clock/VDD combination listed below. For example, 1.8 V LVDS, 3.3 V CMOS, and 2.5 V LVPECL can be supported simultaneously. The device core operates from a separate supply voltage operating at 1.8, 2.5 and 3.3 V and is independent of the output clock supply voltage (VDDO0 to VDDO3).



**Figure 8.** Si5338 Provides User-Programmable Output Clock Formats

### Summary

The Si5338 is the industry's first clock generator capable of supporting any-rate frequency synthesis on four independent output clocks. By providing this level of frequency flexibility, the Si5338 eliminates the need for fixed-frequency clock generators and discrete crystal oscillators. The device provides outstanding jitter performance of 1 ps RMS, enabling a single device to provide reference timing for physical layer transceivers as well as processors, network processors, FPGAs and memory. Frequency margining is greatly simplified because crystal oscillators at margined frequencies are no longer required. To further reduce BOM cost and complexity, the device supports user-programmable output clock formats, eliminating the need for discrete level translators. The best-in-class performance and integration provided by the Si5338 greatly simplify timing architectures in communication and broadcast video applications.