Programmable Crystal Oscillators with Sub-ps Jitter and Multiple Frequency Capability

Oscillator packages today are smaller; stabilities are tighter, and frequencies are higher. Yet, quartz crystals are still fabricated in much the same way that they were in 1943. Each new frequency requires a new crystal to be cut, x-rayed, lapped, mounted and sealed into the final package. Additionally, the aging and reliability problems experienced by the 8th Air Force in 1943 have been exacerbated by new techniques to achieve higher frequencies by chemically thinning the quartz into inverted mesa shapes.

While programmable oscillators introduced in the 90s offered the promise of reinvigorating the manufacturing process, the phase-locked loop (PLL) synthesis techniques employed generated so much jitter that they were only useful in low-performance applications.

And so, the quartz industry has remained largely strapped to the same manufacturing methods of the 1940s for producing quartz crystal oscillators. Each new frequency requires a new "rock."

Implication of Circuit Architecture on Hybrid Crystal Oscillator Manufacturing

As shown in Figure 1, the basic architecture of a crystal oscillator is quite simple. Gain block A represents the oscillator sustaining-amplifier, and block B is the feedback network containing the crystal resonator.

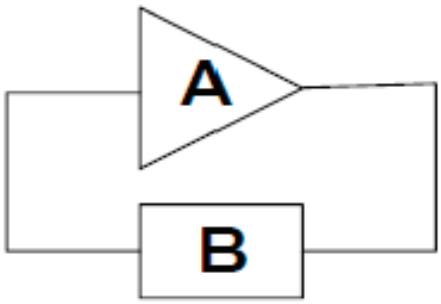

Figure 1. Basic Feedback Oscillator

Barkhausen's well-known criteria for oscillation states that if a frequency exists where the phase around the loop is zero, and the gain of A exceeds the loss of B, then the circuit will oscillate at that frequency. The obvious implication with a narrowband resonator, such as a quartz crystal, is that each new frequency requires a new crystal with the manufacturing consequences being quite profound.

Thousands of distinct crystal frequencies are required to support the wide variety of electronic systems in production today. The required temperature ranges and frequency stabilities are also variable; so, the quartz bar cutting angles must also vary. Not only must the quartz crystal thickness be unique for each different frequency, but the angle of cut from the quartz bar is also varied for different orders. Figure 2 illustrates the typical sequence of processes utilized in manufacturing a hybrid crystal oscillator. Because of the simple feedback oscillator topology, each new oscillator design must begin with quartz blank fabrication. If blank design changes are required due to difficulties encountered in the testing phase, the process must restart at cutting.

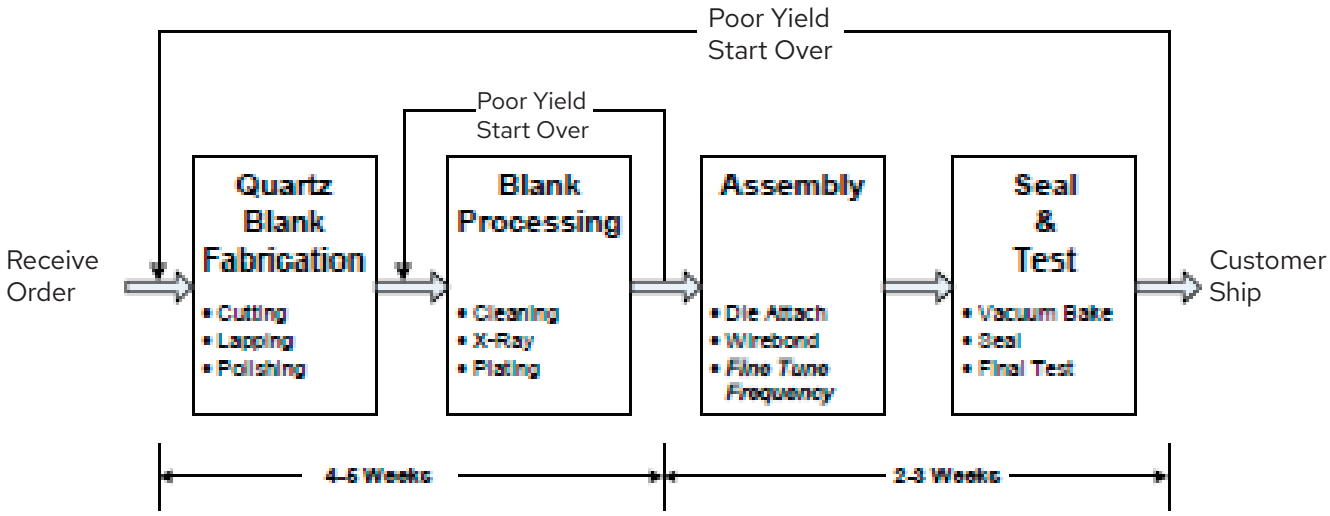

Figure 2. Hybrid Quartz Crystal Oscillator Production Steps

One only needs to tour a typical crystal oscillator factory to see the staggering array of crystals in production at any given point in time. In addition to requiring long and often unpredictable lead times, this build-to-order process complicates implementation of modern manufacturing systems such as statistical quality control or continuous improvement. High-frequency fundamental (HFF) crystals required for low-jitter clocks undergo additional chemical milling of the blank to achieve quartz thicknesses of tens of microns, further exacerbating processing issues.

The situation is no less complicated for SAW-based oscillators where each new frequency requires a new wafer mask to be developed. This requires CAD layout, mask fabrication and wafer processing to be performed for each frequency.

It is quite an achievement that the quartz industry has been able to develop production methods compatible with this tremendous product mix and associated complex quartz processing.

A Frequency-Programmable Architecture For Low Jitter Clock Generation

Over the past few years, advances in fine line CMOS process technology have enabled IC designers to develop high-frequency PLL technology for use as frequency agile clock multipliers and jitter attenuators in multi-gigabit per second optical networking applications. By using this technology to create a new class of hybrid oscillator, many of the manufacturing complexities and performance issues traditionally associated with high-frequency resonators can be eliminated.

This new class of oscillator combines a fixed low-frequency crystal resonator with a new DSP-based PLL architecture known as DSPLL® as shown in Figure 3. The DSPLL is programmed with a multiplication value to translate the fixed low-frequency crystal frequency to the desired output frequency. Using this architecture, high-frequency clocks operating at over 1 GHz are possible with jitter performance that is comparable to traditional high-performance voltage-controlled crystal oscillators (VCXOs) and voltage-controlled SAW oscillators (VCSOs)[4]. The DSPLL engine was designed with 1 ppb resolution over a tuning range that spans 10 to 945 MHz. Above 945 MHz, oscillator operation is limited to select bands to 1.4 GHz. All frequencies are synthesized from a fixed external crystal using a basic feedback oscillator topology. The crystal resonator need not be of high accuracy and does not need to be pullable as all fine frequency tuning is performed digitally via the DSPLL clock synthesis IC. Non-volatile memory (NVM) is provided on-chip to maintain frequency synthesis settings when supply voltage is cycled.

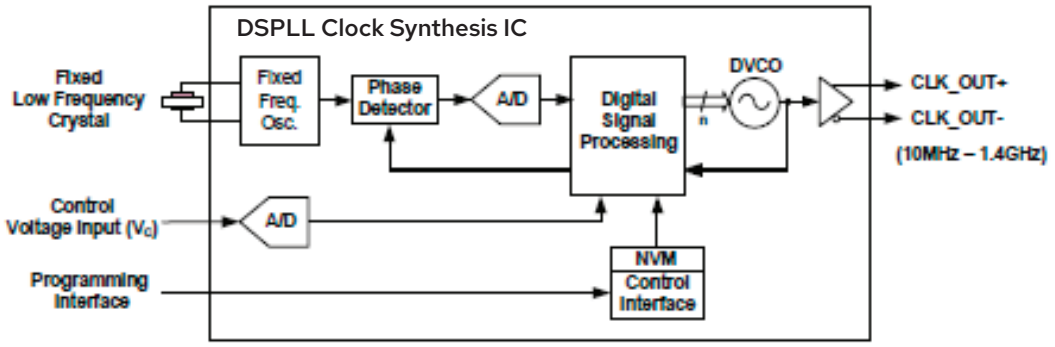

Figure 3. DSPLL-Based Oscillator

A key advantage of this architecture is that a wide range of low-jitter, high-frequency clock signals can be generated from a conventional fixed frequency overtone quartz crystal. This eliminates the need to fabricate unique HFF crystals or SAW resonators for each frequency. Besides the obvious manufacturing issues associated with maintaining a wide range of different resonator frequencies to support a diverse set of customer requirements, HFF crystals and SAW resonators both have reliability and performance issues that can be significantly improved upon through the new oscillator architecture shown in Figure 3.

Hybrid Clock Module With Fixed Frequency Crystal

The DSPLL clock synthesis IC was designed to be packaged together with a quartz crystal into a hermetic ceramic package to support both crystal oscillator (Si530 XO) and voltage-controlled crystal oscillator (Si550 VCXO) applications. Figure 4 shows a functional block diagram of the Si550 hybrid VCXO incorporating the DSPLL technology. A provision to enable or disable the output signal is available through the OE pad. A fixed frequency crystal, such as 120 MHz third overtone, is used inside of the ceramic, hermetically-sealed, hybrid module.

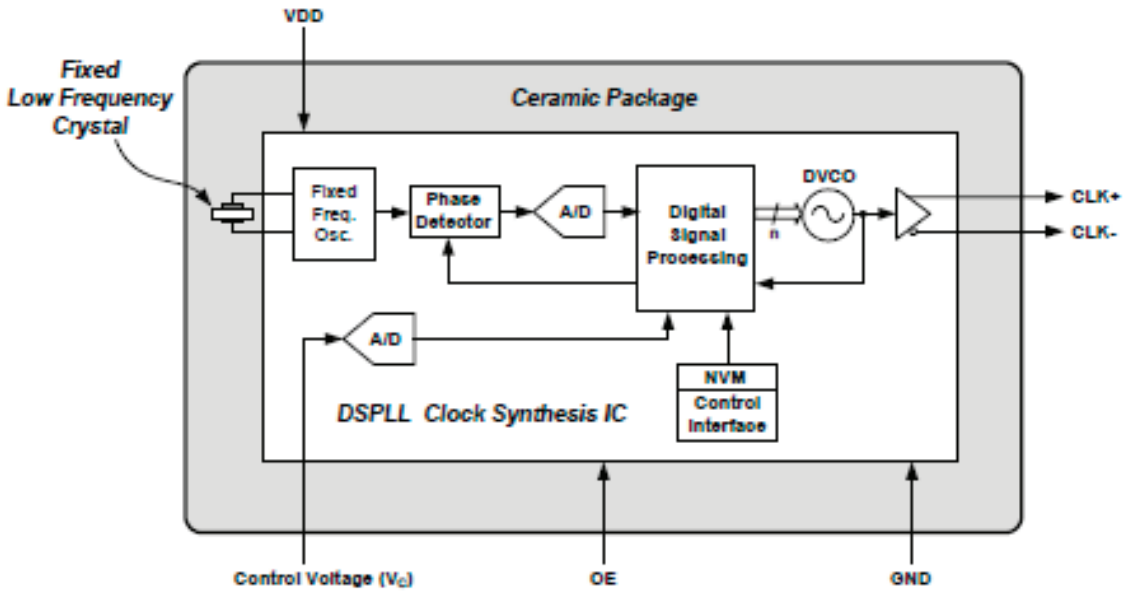

Figure 4. Si550 VCXO Module Incorporating DSPLL

As in conventional hybrid XOs and VCXOs, high-temperature, co-fired ceramic (HTCC) is used for the package, and the lid is welded using seam-sealing techniques. Package hermeticity is better than 5x10-8 ATM-cc/sec, as verified by helium fine leak testing. Industry-standard 7 x 5 mm package dimensions and pad layouts are used for backward compatibility with existing oscillator products.

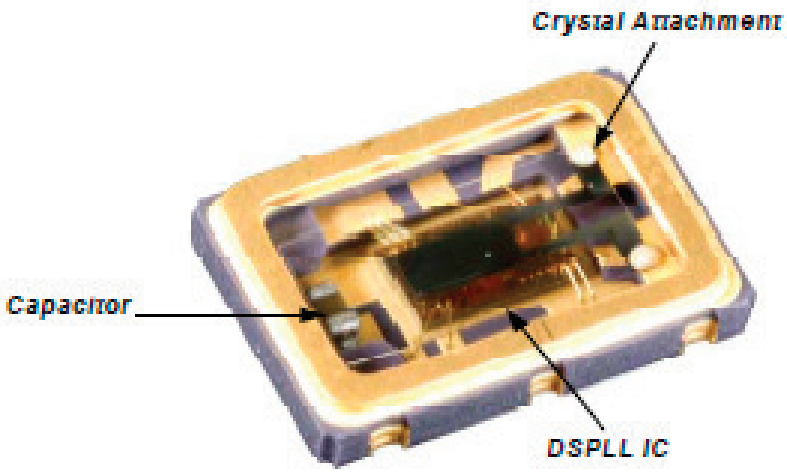

Figure 5. Si550 VCXO Oscillator Module with Lid Removed

Revolutionized Manufacturing Flow

A manufacturing flow that is tailored for short lead times and process optimization as shown in Figure 6 is made possible by hybrid oscillators incorporating the DSPLL clock synthesis IC. In this flow, an inventory of "raw" un-programmed oscillators is produced by hermetically sealing the DSPLL IC together with the low-frequency crystal blank. While the hybrid assembly of the crystal blank and IC share some similarities to the flow shown in Figure 2, there are two major simplifications. First, only one frequency of crystal blank is required; and second, the fine frequency-tuning step is eliminated. This allows for continuous improvement of the blank and hybrid assembly process while eliminating an entire processing step.

In response to customer orders, "raw" devices are pulled from inventory, programmed to satisfy customer frequency specifications and shipped. Thus, the order fulfillment flow changes from a complex build-to-order process with eight-week lead times to a simple program-to-order process with one-week lead times. In addition to offering much shorter lead times, this method also facilitates modern techniques, such as lean manufacturing and continuous improvement.

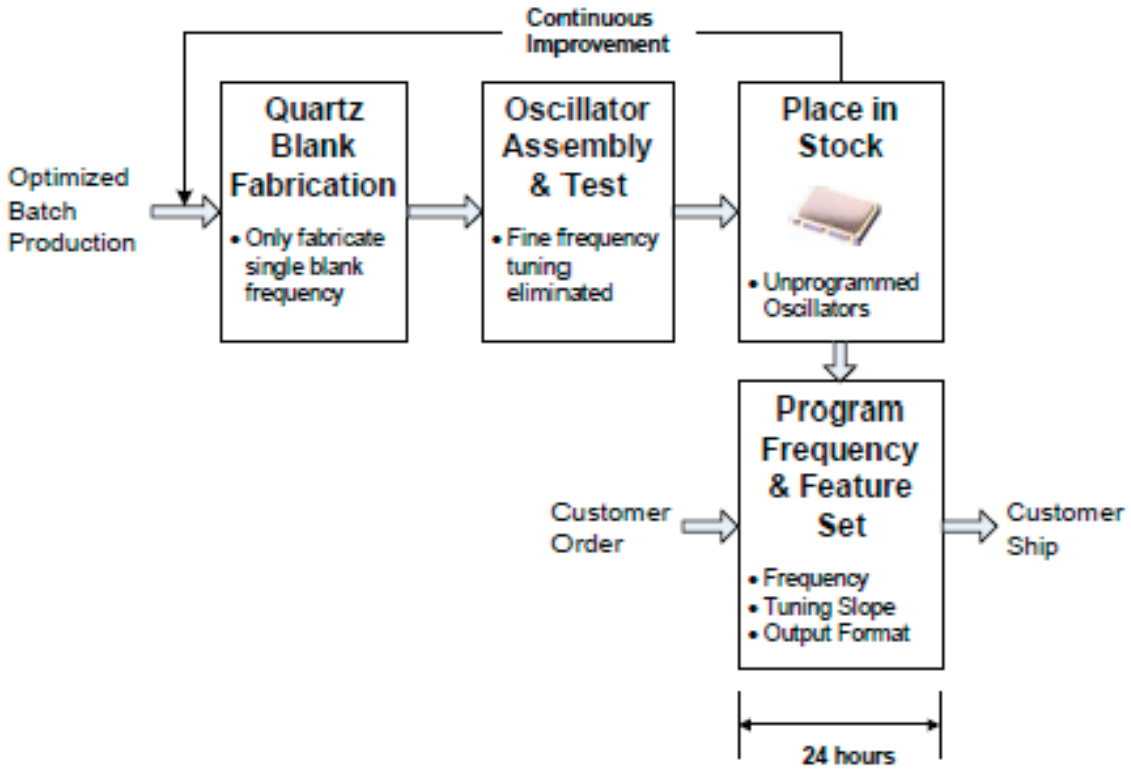

Figure 6. Program-To-Order Flow of Programmable Crystal Oscillator

Improved Initial Frequency Accuracy

Oscillator designs using the DSPLL clock IC for high-resolution frequency synthesis eliminate one of the largest variables that determines the initial accuracy of XOs. Both traditional crystals and hybrid XOs experience a two-step frequency adjustment process. The first step, termed base plating, is performed in a batch mode using thin-film deposition techniques, such as sputtering. A monitor crystal is co-located with devices to be plated, and the frequency is monitored as a measure of film thickness. Since varying the film thickness slightly alters the vibrating mass, the frequency can be slightly adjusted by trimming the film thickness. This technique is limited to an accuracy of a few hundred ppm; so, a second fine-tuning process is required. Fine-tuning involves selectively adding or removing metal from the surface of the quartz and again modifying the vibrating mass. Frequency is continuously monitored, and the process is stopped when the target frequency is achieved. The process sensitivity is quite severe for HFF crystal oscillators. Since a single atomic layer of metal may cause the frequency to change by many tens of ppm[5], achieving an initial tolerance of 10 ppm requires depositing less than one atomic monolayer. Unfortunately, the oscillator must then be sealed, and the resulting change in parasitic capacitance causes additional changes in frequency. Residual mechanical stresses in the package also cause frequency shifts. For HFF VCXOs, initial accuracy may be in the several tens of ppm. SAW oscillators are similarly affected by the ability to control ultra-thin film deposition and residual package stresses.

By incorporating high-resolution frequency synthesis into the DSPLL clock IC, the oscillator frequency is set through a simple programming step rather than the traditional two-step tuning process. In contrast, the specifications for the crystal resonator in DSPLL-based hybrid oscillators can be relaxed to an initial accuracy of ±10,000. As a result, only the initial baseplating of the crystal is necessary, and the fine-tuning step can be eliminated. Additionally, the frequency shifts due to both parasitic capacitance change and residual package stress can be compensated for since the oscillator is programmed to the final frequency after sealing. Finally, because the DSPLL clock IC offers programming resolution of less than one ppb, it would be expected that initial frequency accuracies of one ppm are possible for high frequency XO and VCXO devices. This is roughly an order of magnitude better than traditional high frequency oscillators

Improved Aging Performance

Operation on an overtone reduces the resonator C1 by the reciprocal of the overtone, squared. This means that a third overtone crystal will have approximately one-ninth the pull range of a fundamental, and a fifth overtone will have only one-twenty-fifth the pull range. While this is beneficial for high-stability OCXOs, this is undesirable for wide-pull VCXO operation and essentially mandates the use of fundamental mode crystals. Achieving adequate pull range is the underlying reason behind the use of HFF crystals for VHF-band VCXOs, such as 155 MHz. It is well known that aging performance is related to the inverse of quartz blank thickness (i.e. a thick quartz blank can have superior aging). For example, a 38.8 MHz fundamental-mode resonator will have aging stability superior to that of a 155 MHz resonator. The 38.8 MHz fundamental will also have a third overtone resonance at 116.4 MHz. Since the oscillator is not directly pulled with the DSPLL architecture, this

resonator can readily be used in a VCXO using the Si5301 IC. Since the resonator thickness of a 116.4 MHz third overtone will be four times the thickness of a 155 MHz fundamental, aging performance will be similarly improved. Aging for the module is specified at ± 10 ppm over a typical 15-year life. This contrasts with typical SAW or HFF aging of several ppm/year.

Low Jitter Clock Signals

Jitter is a critical clock signal parameter for many applications and is a major factor in determining key system attributes, such as bit-error-rate (BER). Jitter is derived from an integration of phase noise over a specified bandwidth. For example, OC-192 systems specify a jitter integration bandwidth of 12 kHz to 20 MHz. Phase noise for a 1.24 GHz clock signal is shown in Figure 7.

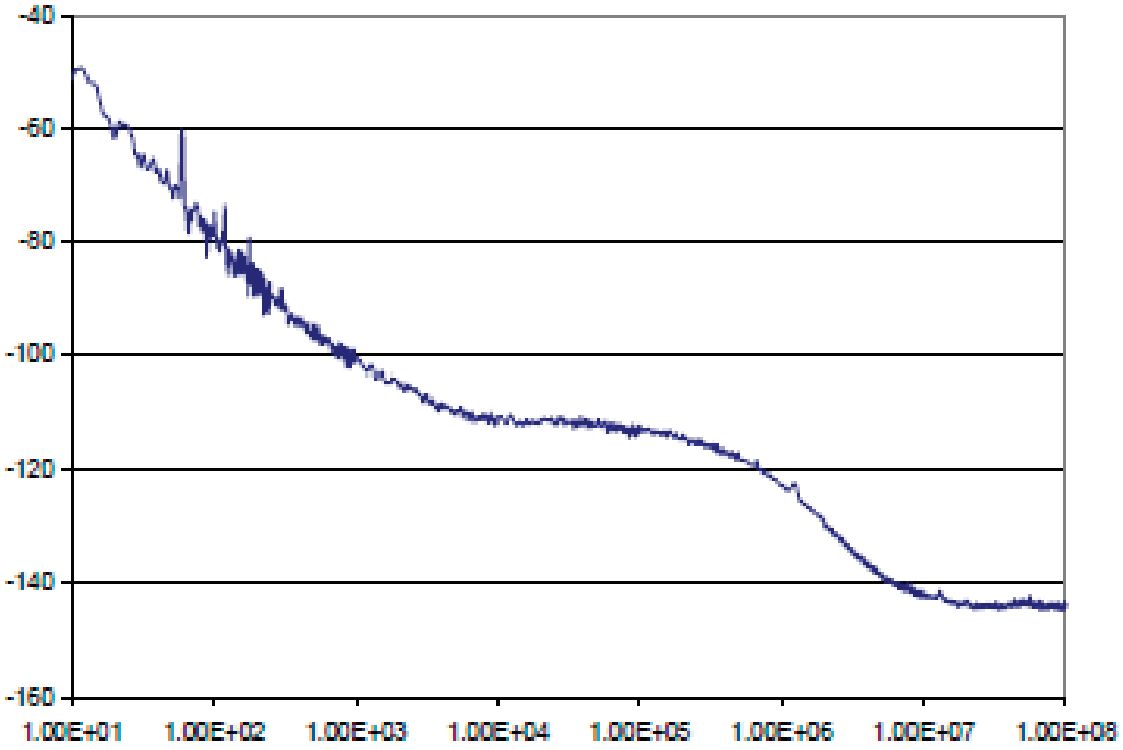

Figure 7. Phase Noise of Si550 VCXO at 1.24 GHz

Phase noise performance at offsets lower than 10 kHz is determined primarily by the on-chip crystal oscillator, while the output LVPECL signal levels largely set the noise floor for offset frequencies greater than 10 MHz. Intermediate frequency phase noise performance is determined by the on-chip VCO and associated PLL components. Jitter derived from integration of phase noise is 0.332 ps over the bandwidth of 12 kHz to 20 MHz and 0.319 ps over the bandwidth of 50 kHz to 80 MHz. This performance essentially matches performance results typically obtained when using high-performance SAW or HFF resonators in the conventional feedback oscillator topology of Figure 1. Depending on the ratio of output frequencies to crystal resonator frequency, some spurious signal content may be generated. At a specified value of -80 dBc, spurious content is substantially lower than previously available in programmable clocks.

Programmable Tuning Slope

Traditional VCXOs utilize a varactor diode to modify the resonant frequency of the oscillation loop. Since the loop-resonant frequency is modified by the well-known C1/2(C0+CL), where C1 and C0 are crystal equivalent circuit values and CL is the load capacitance, changes to CL affect the output frequency. Non-linear behavior in the oscillation loop determines the overall tuning slope linearity. The tuning slope, Kv, is measured in ppm/V and is directly proportional to the crystal motional capacitance C1.

In contrast, the tuning voltage, Vc, is digitized on the DSPLL IC through a high-resolution ADC. The resulting digital number is used to slightly modify the frequency synthesis engine and hence the output frequency. Since Kv is simply a numerical multiplication factor, differing values of Vc can be programmed after the oscillator is assembled. A family of tuning slopes for a 622.08 MHz VCXO is shown in Figure 8.

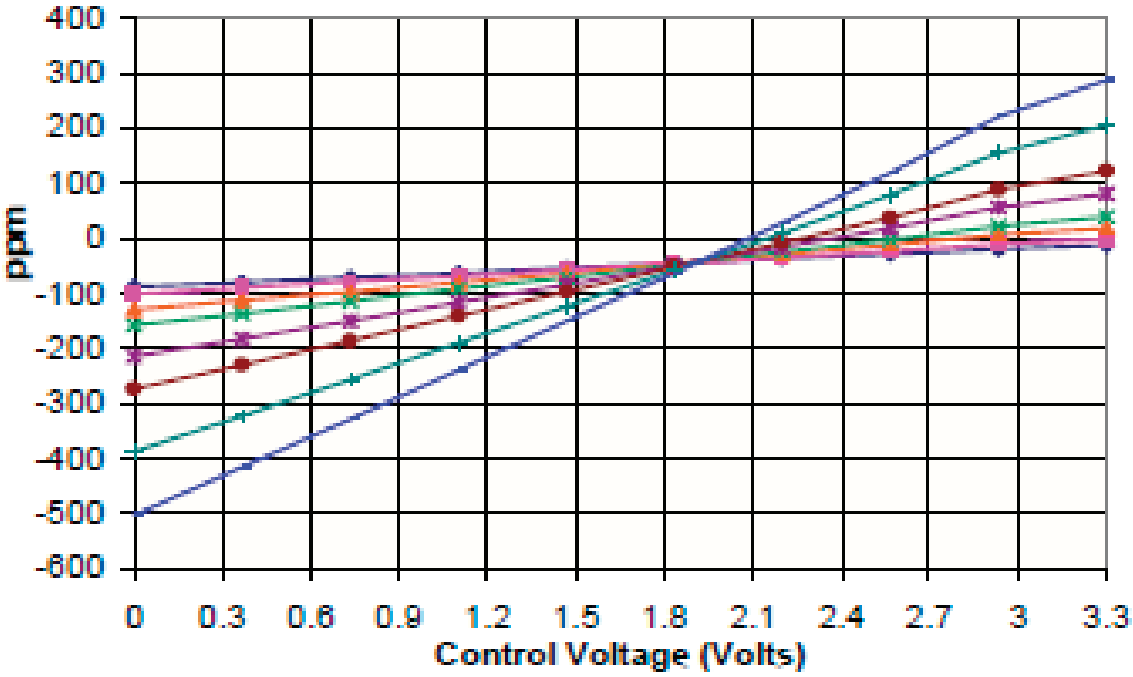

Figure 8. Programmed Tuning Slopes of DSPLL Based VCXO

These results were obtained from a single hybrid oscillator by simply reprogramming the value of Kv. With a programmable gain ranging from 15 to 270 ppm/V, Kv effectively emulates typical characteristics of most SAW and crystal VCXOs. The small roll-off at voltages above 3 V is due to slight drooping of the reference voltage for the ADC converter as Vc approaches VDD. Linearity, particularly for the most useful range below 3V, is dramatically improved compared to conventional varactor-based VCXOs.

Multiple Frequency Operation From One Crystal Resonator

Applications are emerging that require multiple clock frequencies slightly offset from each other. For example, 622.08 MHz is a widely-used SONET transport frequency. Forward error correction (FEC) is used to improve bit error rate performance; so, additional bits must be interleaved within the SONET payload. This increases the clock frequency to a slightly higher frequency, such as 666.5143 MHz. Conventional technology VCXOs must use distinct crystals or SAW resonators for each unique frequency. This approach becomes increasingly untenable as the number of required frequencies increases beyond two. Using DSPLL clock synthesis, multiple output frequencies can readily be generated from a single resonator. Using packaging similar to Figure 5, dual frequency XO (Si532) and VCXO (Si552) oscillator modules have been developed that provide two selectable output frequencies from a single quartz crystal. In the quad XO (Si534) and VCXO (Si554) series, additional pads are provided on the ceramic package for binary selection of four individual output frequencies. Similar to the dual frequency parts, only one quartz crystal is required, and the choice of output frequencies is arbitrary within the operating bandwidth of the DSPLL IC.

Summary

A new class of crystal oscillators has been developed which offers high-resolution, programmable frequency and high performance. These oscillators dramatically simplify the manufacturing process and thereby shorten product lead times. Additional performance advantages include better initial frequency accuracy, long-term aging and voltage control linearity.

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