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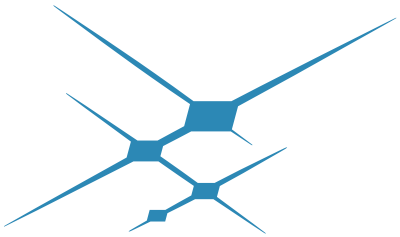

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Guide to Using Jitter Attenuator Status Indicators White Paper

This white paper is intended to help users understand how the Si539x status indicators and alarms operate and how to make the best use of them. It provides useful suggestions and recommendations for ClockBuilder® Pro (CBPro) settings.

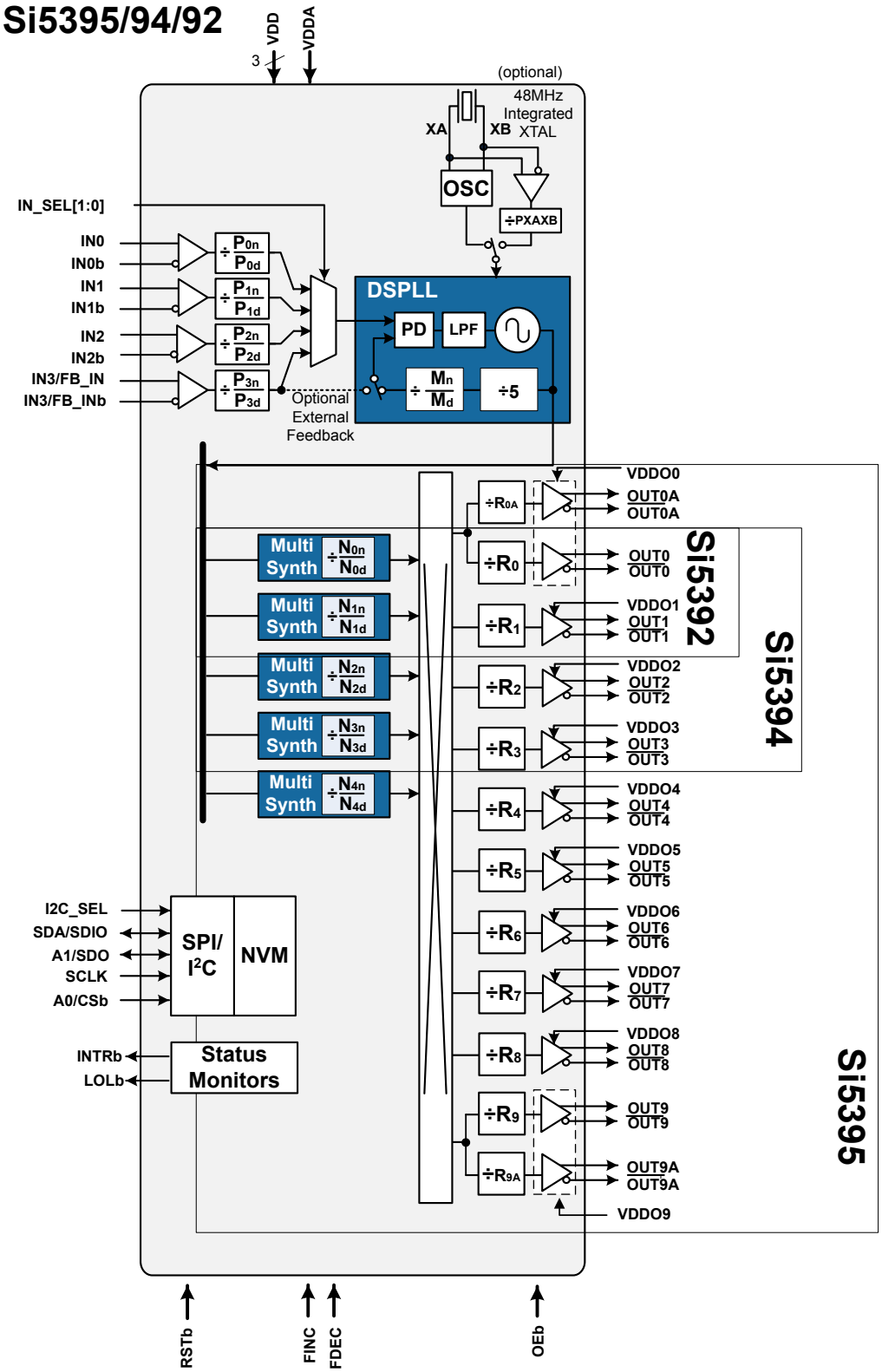
The Si539x alarms and status flags are used to control and monitor the behavior and status of Si539x devices. The alarms described in this white paper cover the input monitoring circuitry (loss of signal (LOS), out of frequency (OOF)) and PLL lock status (loss of lock (LOL)). This document is directed towards the Si5392, Si5394, Si5395, Si5396, Si5397 and Si5348 Rev E devices. Although some of the examples use the Si5395, the principles described apply equally well to the other devices listed.

All of the alarms listed above entail tradeoffs between speed and accuracy, and their programmability is an effort to mitigate this problem. In frequency measurement, the longer the measurement, the more accurate the reading. Mathematically, a quick measurement places limitations on the resulting resolution. For example, to measure the frequency of a 1 MHz signal to within 1 ppm, the measurement must take place for at least one second.

ClockBuilder Pro (CBPro) provides a “set for me” option and a default setting for alarm/status configuration registers. In almost all circumstances, these values provide the best solutions and performance. However, for rare exceptions, the information presented here will be useful in understanding the alarms and deciding the likely results of changing parameters.

Referring to the Si5395 block diagram, the alarms control the upper, blue, DSPLL section and the input mux. The output of the DSPLL is the VCO divided down by various values to produce different output frequencies. The input P dividers in the Si5395 block diagram drive the mux, which is also an HSW (hitless switching) engine. Clock selection can be register-based manual, pin-based manual, or automatically switched using the LOS and OOF alarms.

Both CBPro and the reference manuals for individual devices are companion resources that should be used for more details and background information.



Si5395 Block Diagram

1. Introduction

The loss of signal (LOS), out of frequency (OOF), and loss of lock (LOL) alarms are shown in the figure below. The following sections describe how they work. The figure shows the logical flow of the LOS/OOF status bits from the input clocks to the phase detector. Note that additional clock inputs for the Si5348 (IN3 and IN4) are not included in this diagram.

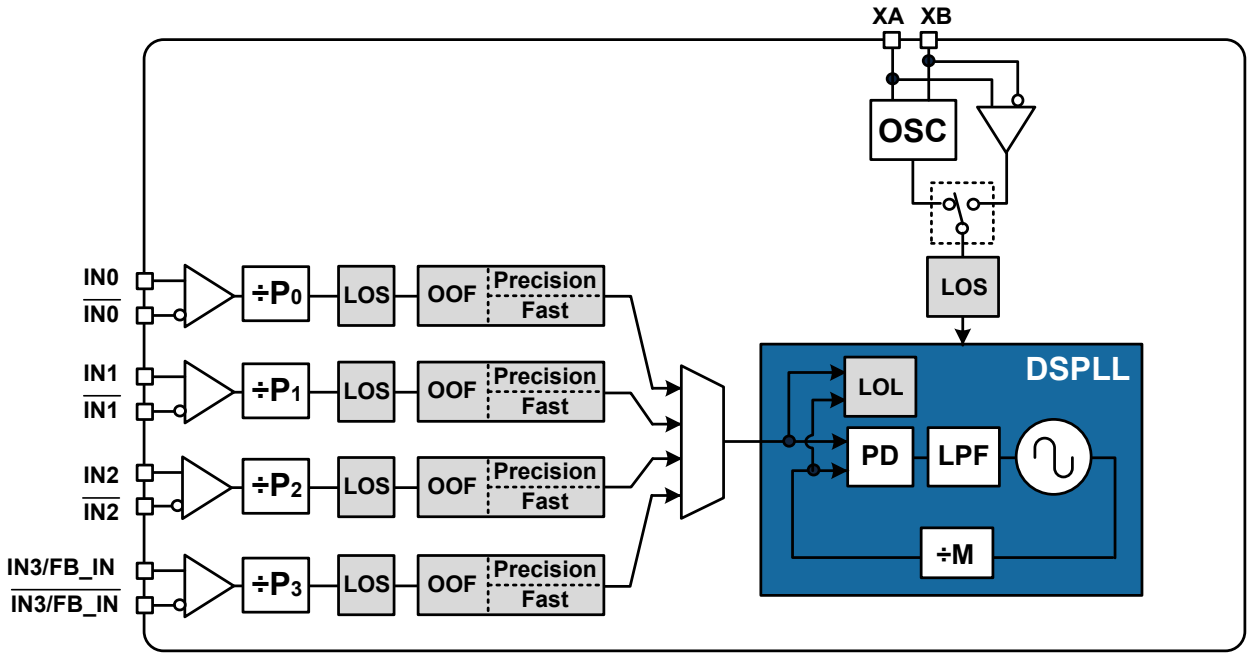


Figure 1.1. LOS, OOF, and LOL Alarms

The following figure shows the flow from the input mux through the phase detector, VCO, and M feedback divider and how LOL is generated.

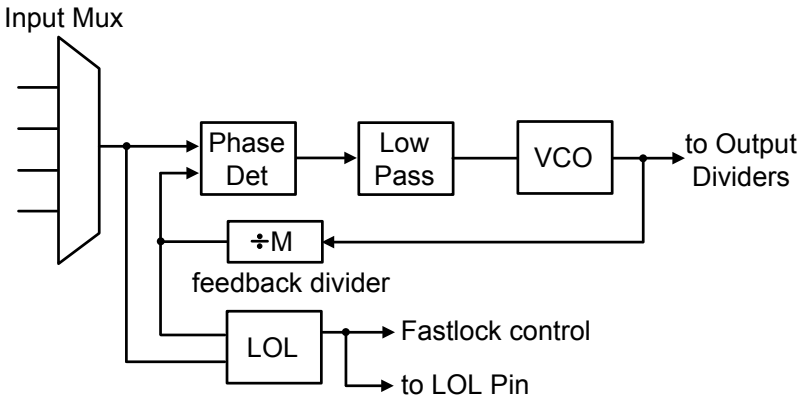


Figure 1.2. Logical Flow of LOS/OOF Status Bits from Input Clocks to Phase Detector

1.1 Acronyms

This white paper uses the following acronyms:

- LOS—Loss of signal
- OOF—Out of frequency
- LOL—Loss of lock
- HSW—Hitless switching
- VCO—Voltage-controlled oscillator
- Fpfd—Frequency at the phase/frequency detector
- CBPro—ClockBuilder Pro

1.2 Alarms, LOL, and Holdover

The LOS and OOF alarms control entry into holdover and automatic clock selection by default. For a given clock input, if one or more of its alarms are asserted, the clock input is considered to be invalid, and it will not be possible to switch to or remain connected to that clock input. In this case, the next valid clock in the automatic clock selection priority list will be selected. If no such clocks are available, the Si5395 will enter holdover and remain there until one or more clocks subsequently becomes valid.

OOF and LOS do not directly cause LOL. LOL does not cause entry into holdover. However, when in holdover, LOL is logically asserted. By default, LOL dynamically adjusts the PLL bandwidth to speed up relocking when a valid clock is presented to the PLL.

1.3 LOS

LOS is an alarm that is set when there is no signal on a given clock input. It is intended to be a fast indicator of when a clock has either appeared or disappeared.

The inputs to the LOS logic are the inputs to the phase detector, which operates at the Fpfd. The LOS assert and de-assert thresholds are programmed with respect to the Fpfd cycles. As a result, the speed of the LOS alarm depends on Fpfd. A higher Fpfd results in a faster LOS response time, which is an important consideration for HSW that will be discussed below.

The LOS alarm verifies the period between rising edges of the Fpfd rate clock. The LOS logic uses a counter that counts a fixed clock signal (~60 MHz) that is much higher in frequency than the maximum Fpfd of 2 MHz. This counter is cleared by a positive edge going into the phase detector. If the counter value at the time it is cleared is above a programmable threshold, the LOS alarm is turned on. Once the LOS alarm has been turned on, if the value of the counter at the time of the next positive edge going into the phase detector is less than a programmable value, the LOS alarm will be turned off. In this way, LOS will be asserted whenever one or more clock input edges are missing. The trailing edge of LOS assertion can be extended by a programmable amount so that there is a minimum validation time before LOS is negated. The validation time is useful when exiting holdover (see below).

LOS logic can also be asserted whenever clock edges are too close to one another. This feature was added to assist in clock switches performed externally to the Si539x device.

1.4 OOF

The Out-of Frequency (OOF) alarm is asserted when there is a signal at a given clock input, but it is not within a specific user-settable frequency tolerance. Unlike LOS, OOF can make accurate frequency comparisons but does so at the expense of increased detection time. There are two versions of OOF: precision and fast. The precision version has higher resolution but a greater detection time. OOF does not detect absolute frequencies but rather the frequency difference between two clocks. One frequency input into the OOF logic is the OOF reference for all of the clock inputs that are being OOF monitored. The OOF reference can be any one of the clock inputs or the XAXB source, which is typically crystal-referenced. The absolute accuracy of OOF depends entirely on the absolute accuracy of the OOF reference. The relative accuracy of OOF is dependent upon the OOF configuration. For obvious reasons, the OOF reference cannot monitor itself.

Unlike LOS, the inputs to the OOF logic are the raw clock inputs. The two OOF inputs need to be prescaled to be within an octave of one another because the OOF reference and the clock being OOF monitored can differ significantly in frequency. The two different prescaled clock rising edges each determine when a free-running, high-speed counter's value is sampled. The value in the OOFx_DETWIN_SEL register determines how many prescaled clocks occur between samples of the free-running, high-speed counter. The greater the value of OOFx_DEWIN_SEL, the more accurate the measurement will be and the more time it will take. The difference between the two different counter values will be proportional to the frequency difference between the OOF reference and the clock being monitored. This difference is compared to a programmable threshold value to determine whether to assert the OOF alarm. The Fast OOF and precision OOF alarm outputs are OR'd together to produce an overall OOF alarm. The table below lists samples of times and accuracies provided by precision OOF. The OOFx_DETWIN_SEL registers are at addresses 0x4E and 0x4F.

Table 1.1. OOF Detection and Clear Times

OOFX_DETWIN_SEL	Detection Window Duration		Max Trig, Clr Time	Frequency Measurement Error (ppm)	
	Min	Max		Min	Max
0	56.3 µs	138 us	276 µs	58.2	284
1	225 µs	552 µs	1.10 ms	14.6	71.1
2	900 µs	2.21 ms	4.42 ms	3.64	17.7
3	3.6 ms	8.83 ms	17.7 ms	0.909	4.44
4	14.4 ms	35.3 ms	70.7 ms	0.227	1.11
5	57.65 ms	141 ms	283 ms	0.0568	0.278
6	231 ms	565 ms	1.13 sec	0.0284	0.0694
7	922 ms	2.26 sec	4.52 sec	0.0071	0.0174

1.5 LOL

LOL is an alarm that is set whenever the DSPLL is not locked to an input clock. Unlike most LOL circuits, the Si539x LOL is not based on the phase detector but on the difference in frequency between the two inputs and the phase detector. This provides a better method of establishing programmable LOL thresholds, but it also invokes the speed-versus-accuracy tradeoff. The two inputs to the phase detector are the output of the input P divider (that is currently selected) and the output of the feedback M divider (which are the same frequency when the DSPLL is locked). Each of the two inputs to the LOL logic has its own high-speed counter driven with a fixed-frequency clock. The counters are sampled after a programmable number of input clock edges. The two values of the counters are subtracted, and the resulting value is proportional to the difference between the two LOL input frequencies. This difference is then compared to the programmable set and clear thresholds. Once LOL is set, there is a programmable timer that extends the trailing edge of LOL, if so desired.

2. Logical Consequences of LOS, OOF, and LOL

The following sections describe how LOS, OOF and LOL can affect the behavior of Si539x devices.

2.1 Holdover

Whenever there is no valid clock and the holdover history is valid and available, the Si539x will enter holdover. For automatic clock selection, the definition of “no valid clock” is when all input clocks have either an LOS or an OOF alarm. For either register- or pin-based manual clock selection, the definition of “no valid clock” occurs when the currently selected clock has either an LOS or an OOF alarm. When there are no valid clocks, the Si539x enters holdover. If a clock subsequently becomes valid (i.e., none of its alarms are asserted), the Si539x exits holdover.

When in holdover, LOL is always asserted. However, the assertion of LOL will have no effect on either entering or exiting holdover. Holdover is asserted or negated solely on the values of the input LOS/OOF alarms.

2.2 Fastlock

When an Si539x DSPLL enters Fastlock, its loop BW is temporarily increased to speed up the response time of the DSPLL. This can be important in low-loop BW applications. With a loop BW of 10 Hz or less, it can take minutes or even hours for the DSPLL to fully lock, and the proper use of Fastlock will dramatically speed up this process. If so programmed, Fastlock is entered when LOL is asserted, and it is negated when LOL is negated. This means that LOL is more than just a status/information bit, as it can affect the operation of the DSPLL. Note that the LOL extension timer was created for the purpose of lingering in Fastlock longer and ensuring quick reacquisition.

2.3 Clock Switching

As indicated in the various reference manuals, there are two modes of clock selection: Automatic and Manual. Manual clock selection can be either register-controlled or (for some devices) pin-controlled. Whether in automatic or manual mode, clock switches can be further categorized into the three types discussed below: automatic, manual and external. For a detailed discussion and some example measurements, see application note "AN1057: Hitless Switching using Si534x/8x Devices".

2.3.1 Automatic Clock Selection

For a number of reasons, automatic clock selection is by far the most popular choice. The main advantage of automatic switching is that the Si539x is at the center of the decision to make a switch, which makes it easier to implement the phase buildout. Because the implementation of phase buildout is not instantaneous, it is important to minimize the time from when an input clock disappears to when the new clock has had the phase buildout applied to it. During that time, the Si539x is effectively in holdover and, therefore, is locked to the XAXB reference. Even though it is a short period of time, if the XAXB reference drifts even a small amount, the phase buildout can become less accurate, which will add to the effective phase hit during the switch. It is for this reason that a fast LOS response is important. Since LOS operates at the phase detector frequency, a high phase detector frequency will result in a smaller phase hit during HSW.

If the CBPro “set for me” box is checked (see Figure 3.7 "Set for me" LOS Settings on page 14 for details), CBPro will set the LOS configuration for the fastest LOS response time allowed by the phase detector frequency.

2.3.2 Ramped Switching

Strictly defined, HSW with phase buildout only occurs between two clocks that are frequency locked but have an arbitrary phase relationship. When switching between clocks with frequencies that are not exactly the same but are relatively close (i.e., are plesiochronous), phase buildout is not appropriate because the phase difference between the two clock inputs is constantly changing. For Si539x devices, if the frequency difference is large enough, it is better to linearly ramp the DSPLLs VCO between the two frequencies to avoid closed loop overshoot/undershoot. The frequency difference value that determines whether to ramp or keep the loop closed is a function of the phase detector frequency and the loop BW (among other things). To help users configure the Si539x for their application, CBPro has a Hitless Input Switching Assistant (see 3.3 CBPro – Hitless Input Switching Assistant) that is highly recommended because it eliminates much of the guesswork associated with optimally configuring clock switches.

2.3.3 External Clock Switching

Unless specific precautions are taken or unless there are special circumstances, an external clock selection will not result in the same level of performance as an internal clock selection. One problem to be avoided is the glitches and runt pulses generated by external asynchronous muxes. These can be avoided by using a “glitchless mux”. The application note, "AN1111: DSPLL Input Clock Expander", provides a description and FPGA Verilog code of a glitchless mux. It also provides a description and Verilog code for expansion of the four on-chip clock inputs.

It should be noted that glitchless muxes avoid runt pulses at the expense of inserting a gap into the clock stream, which will be seen as a one-time phase transient by the Si539x. This issue can be avoided by putting the Si539x into holdover, performing the switch with a glitchless mux and then exiting holdover.

2.3.4 Manual Clock Switching

Manual clock switching requires that all of the clock selection logic be external to the Si539x. Manual clock selection can be either hitless (with phase buildout) or ramped. It can either be pin- or register-controlled. Though both can be fast, register control is almost always slower because of the speed of the serial port and any external master driving it. One of the reasons that automatic clock selection is so popular is that, in most cases, the burden of executing the clock switch falls on the Si539x and not on the external logic. Since the Si539x has greater knowledge of its own internal state, unless the application is relatively simple or has special circumstances, it is usually difficult to achieve high HSW performance using manual clock selection.

One technique that has been used is to manually switch to a spare input clock that does not have anything connected to it. This will quickly put the Si539x into holdover. When the new clock has been identified and is ready to go, it can be manually selected, and the Si539x will exit holdover.

3. CBPro Examples

The following are screenshots from CBPro, along with some notes and suggestions for its use. The screenshots are from a recent version of CBPro for the Si5395. As a result, they may change slightly for different devices in the family and might change in future CBPro revisions. In particular, the contents of Table 3.1 HSW Assistant Rules on page 11 may be slightly modified over time. CBPro has a number of “set for me” checkboxes, and they should always be checked unless there are specific and justifiable reasons for doing otherwise.

3.1 CBPro – Define Input Clocks Window

The figure below illustrates the Gapped Clock box that should be checked when an input clock is gapped. If this box is checked, CBPro will make slight corrections to the LOL and Fastlock settings to avoid false assertions caused by the gaps. For more information on gapped clocks, see application note, "AN561: Introduction to Gapped Clocks and PLLs".

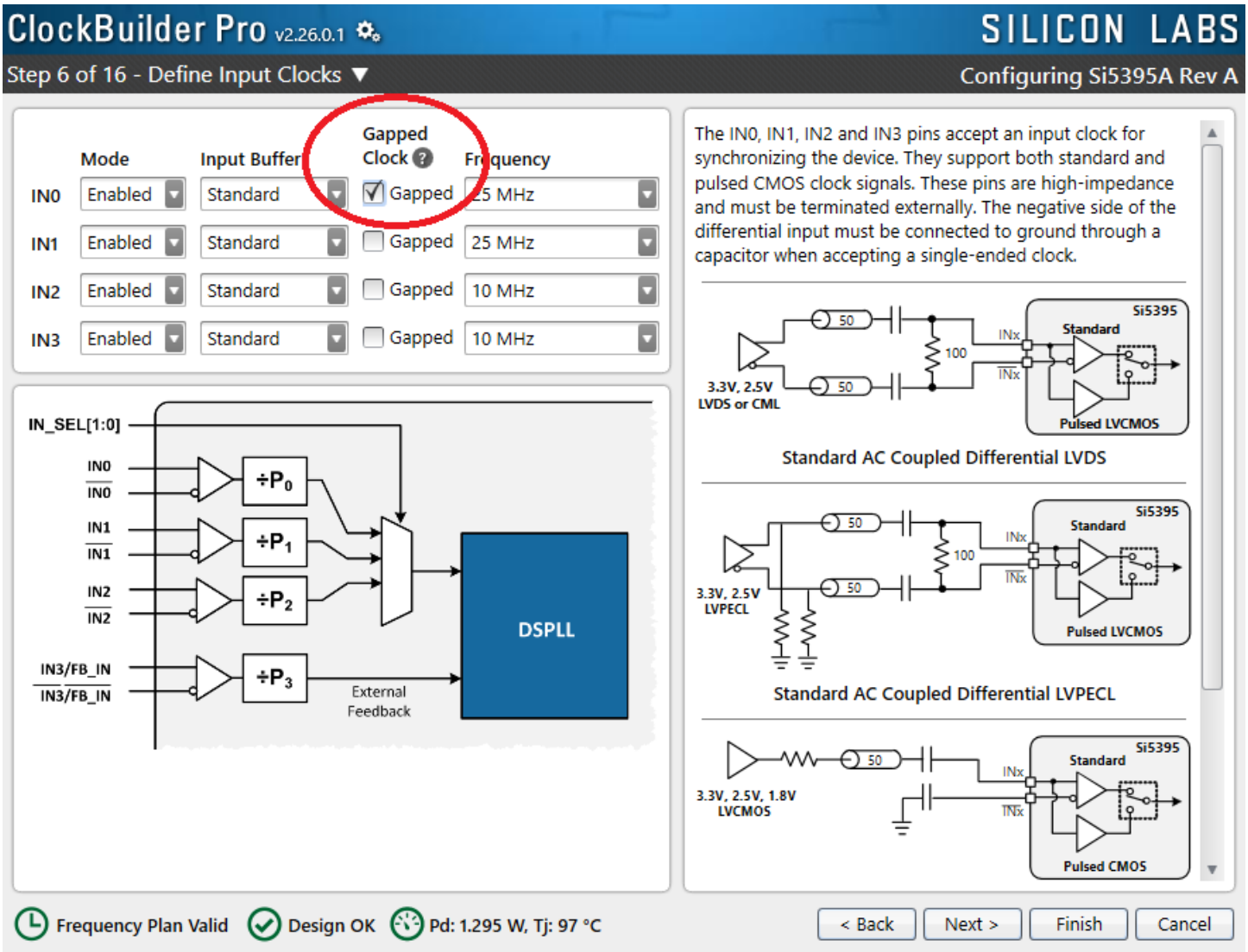


Figure 3.1. Define Input Clocks Window

3.2 CBPro – Input Clock Selection Window

When automatic clock selection is used, the user must select the priorities of the clock inputs, as shown in the upper red box in the figure below. The user can also select which of the LOS and OOF alarms will be used by the automatic clock selection logic. If a box is not checked, that alarm will be ignored during clock selection, and the alarm will effectively be disabled.

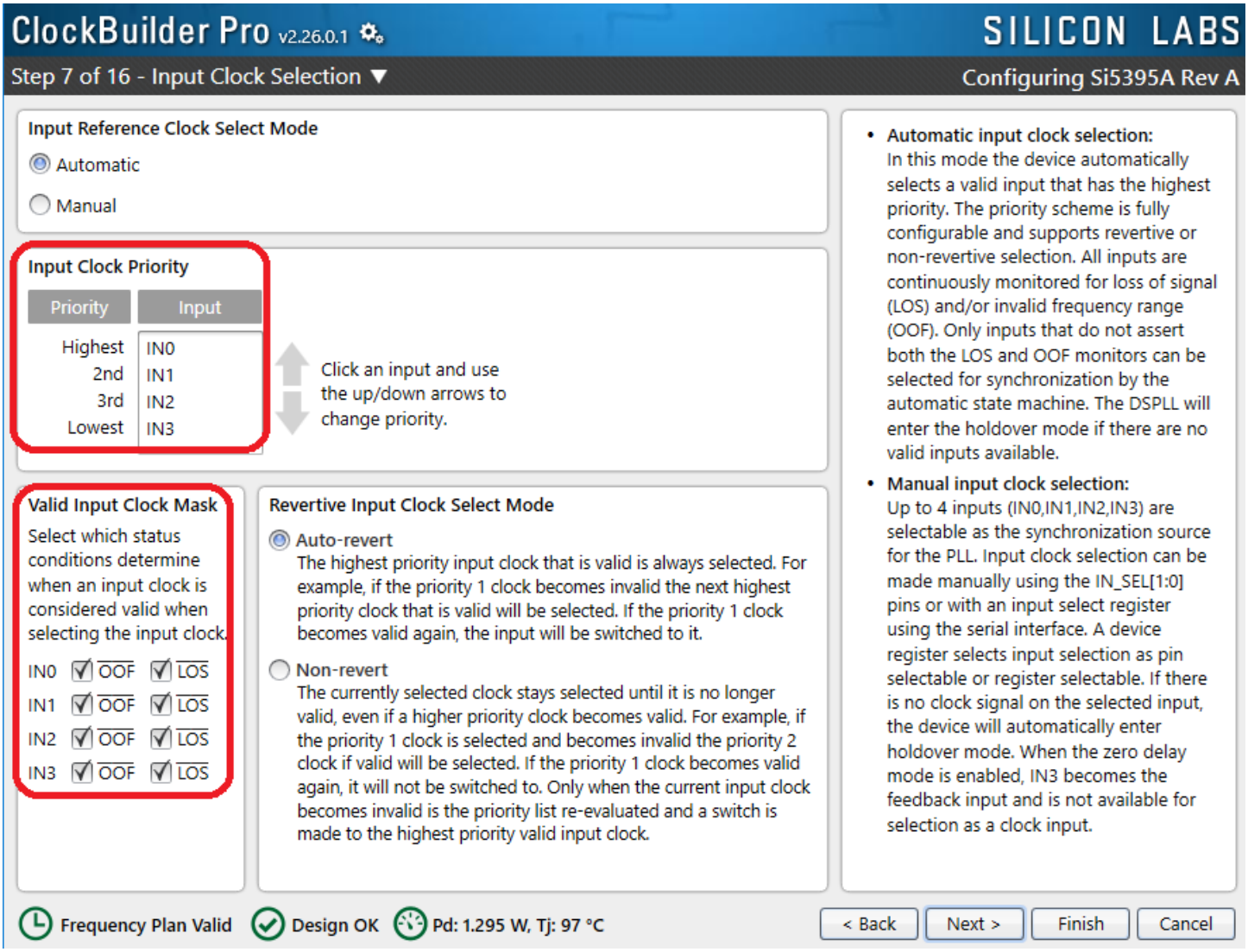


Figure 3.2. Input Clock Selection Window

3.3 CBPro – Hitless Input Switching Assistant

It is recommended that the HSW assistant be used whenever possible. It will choose appropriate settings for a number of important parameters, including HSW, Fastlock, ramping and holdover. The HSW Assistant is enabled by checking the left-hand box as shown in the figure below. If the application in question does external clock selection, checking the right-hand box will (in some circumstances) make slight modifications to the LOS settings.

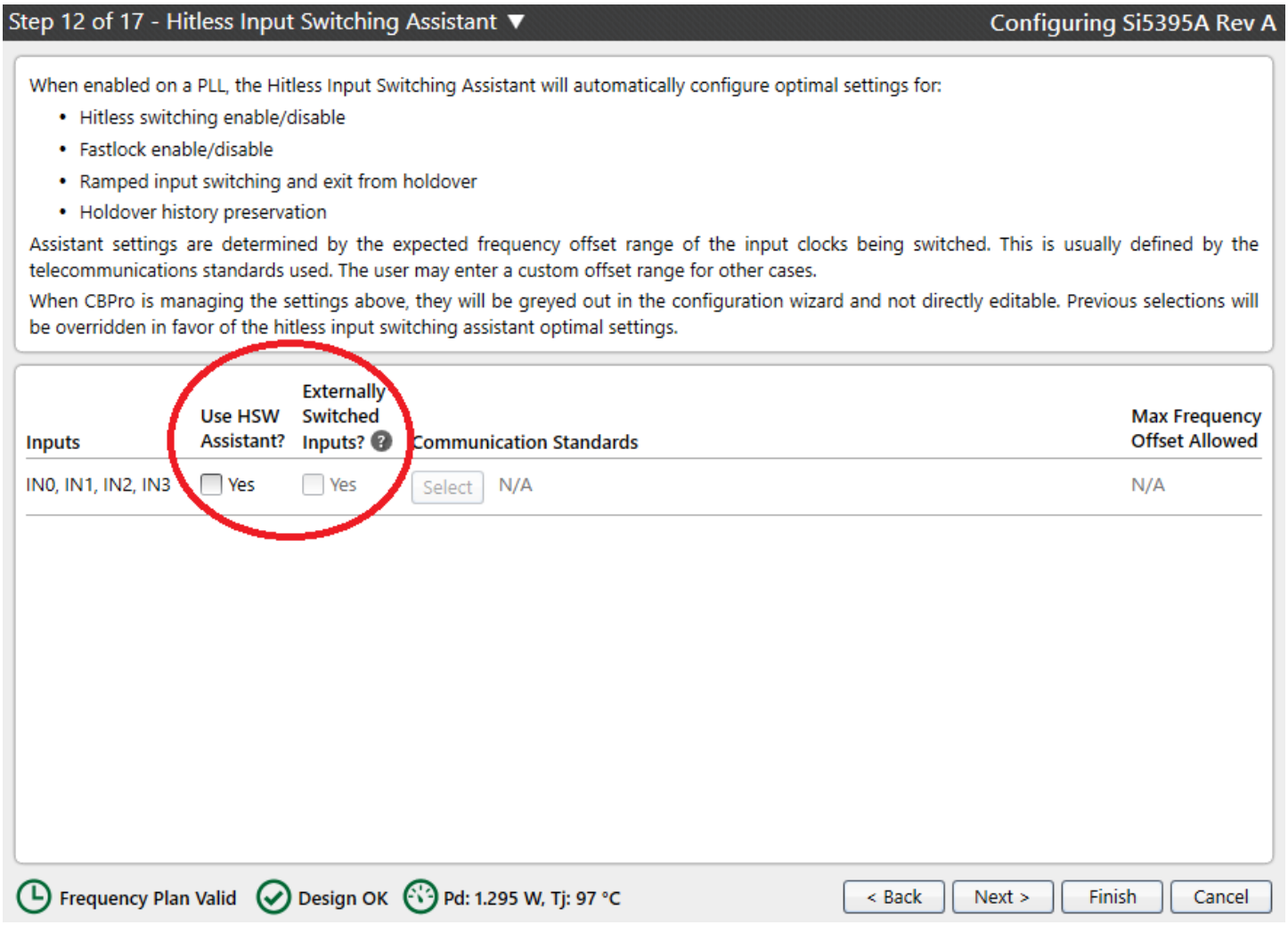


Figure 3.3. Hitless Input Switching Assistant

Once the HSW Assistant is enabled, the relevant Communications Standard should be selected. The Communication Standard limits the expected frequency difference between the two clocks involved in the clock switch. There are provisions for non-standard applications in the bottom selection box. In the example in Figure 3.4 Communication Standards on page 11 below, the Synchronous Ethernet G.8262 is selected.

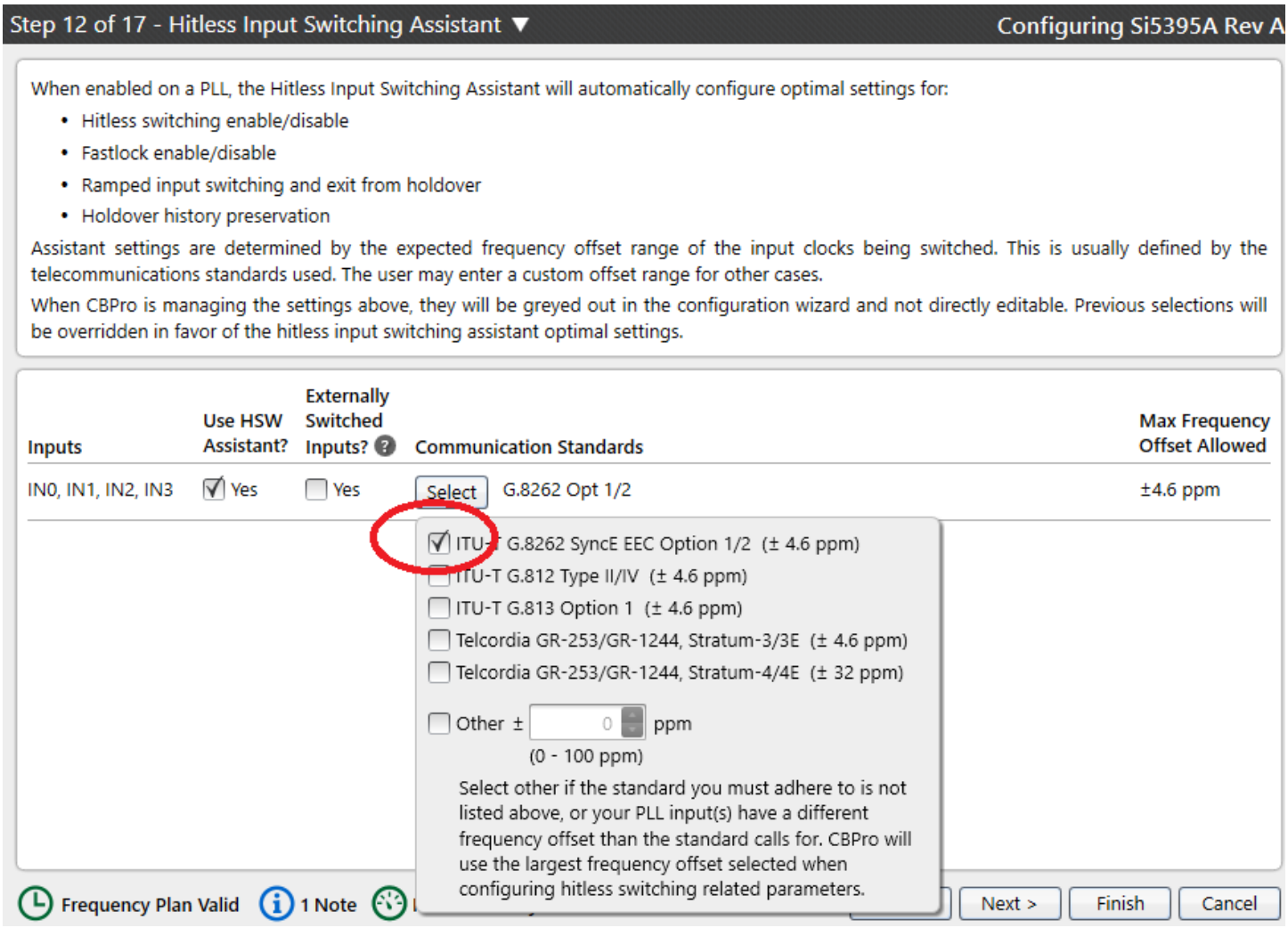


Figure 3.4. Communication Standards

The HSW Assistant implements the rules outlined in the following table.

Table 3.1. HSW Assistant Rules

Criteria					Result				
Switch Type	ID'd as Hitless?	Offset (ppm)	Fpfd (MHz)	# PLL In-put2	HSW	Ramped Input	Preserve HOH-ist	Fastlock	Loop BW Recommend
Internal	Yes	≤ 10	≥ 0.5	2-4	Enabled	Disabled	Enabled	Disabled	Higher
Internal	Yes	≤ 10	< 0.5	2-4	Enabled	Enabled	Disabled	Disabled	Higher
Internal	Yes	> 10	—	2-4	Enabled	Enabled	Disabled	Disabled	Higher
External	Yes	≤ 10	< 0.5	1, 2-4	Enabled	Disabled	Enabled	Disabled	Lower
External	Yes	≤ 10	0.5 - 1.5	1, 2-4	Enabled	Disabled	Enabled	Disabled	Lower
External	Yes	≤ 10	≥ 1.5	1, 2-4	Enabled	Disabled	Enabled	Disabled	Lower
External	Yes	> 10	—	1, 24	Enabled	Enabled	Disabled	Disabled	Lower

3.4 CBPro – DSPLL Window without the HSW Assistant

The figure below shows the DSPLL Window without the HSW Assistant enabled.

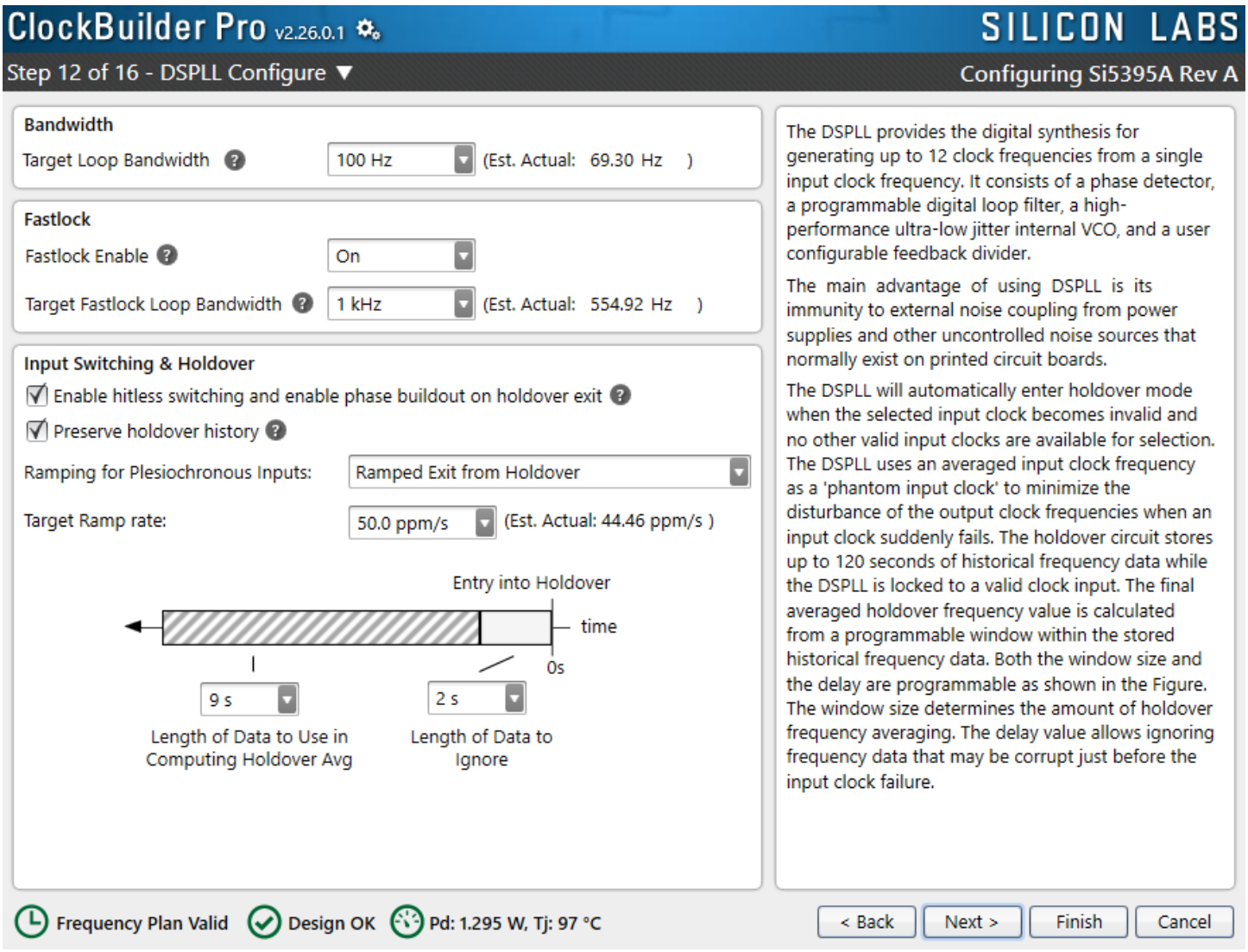


Figure 3.5. DSPLL Window without the HSW Assistant

3.5 CBPro—LOS Window with the HSW Assistant

Because it is difficult to choose between the various interacting parameters, it is recommended that the HSW Assistant be used so that the greyed-out entries are predetermined by the HSW Assistant, as indicated by the red ovals in the figure below. Should it become necessary, disabling the HSW Assistant will unlock these parameters. Hovering the mouse over the small padlock icon to the right of these greyed-out settings shows a reminder that they are being managed by the HSW Assistant.

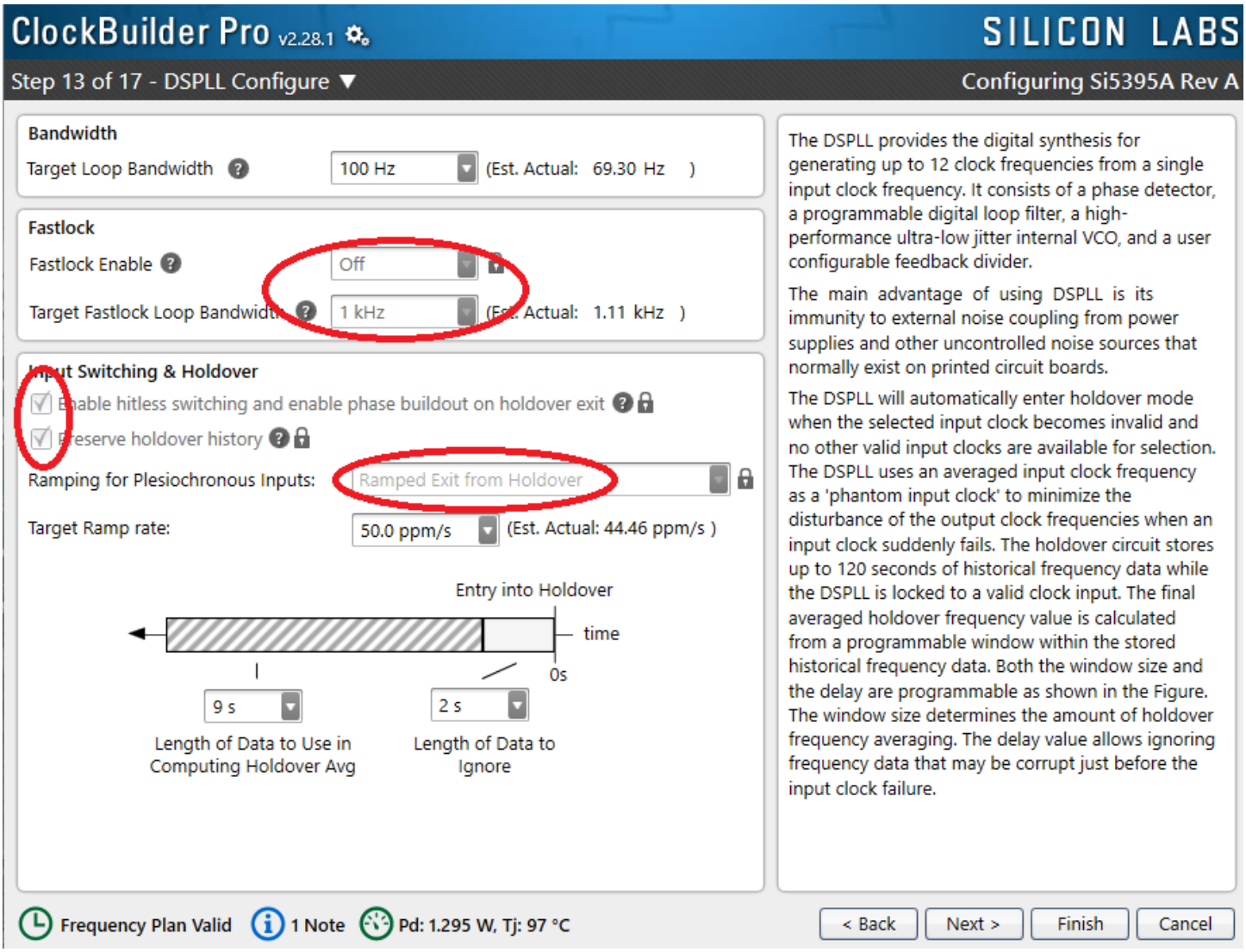


Figure 3.6. Predetermined HSW Assistant Settings

3.6 CBPro – DSPLL LOS Window

As indicated in the figure below, it is recommended that the “set for me” boxes be checked so that the LOS settings will assert LOS if the input to the phase detector has either a period that is too long or a period that is too short. An excessively long clock period is an indication of a lost clock. A period that is too short is an indication of a runt clock pulse that could be caused by an external asynchronous mux. When manually setting LOS thresholds, it is important to allow sufficient margin above and below one Fpfd period so that input clock jitter does not generate false LOS alarms.

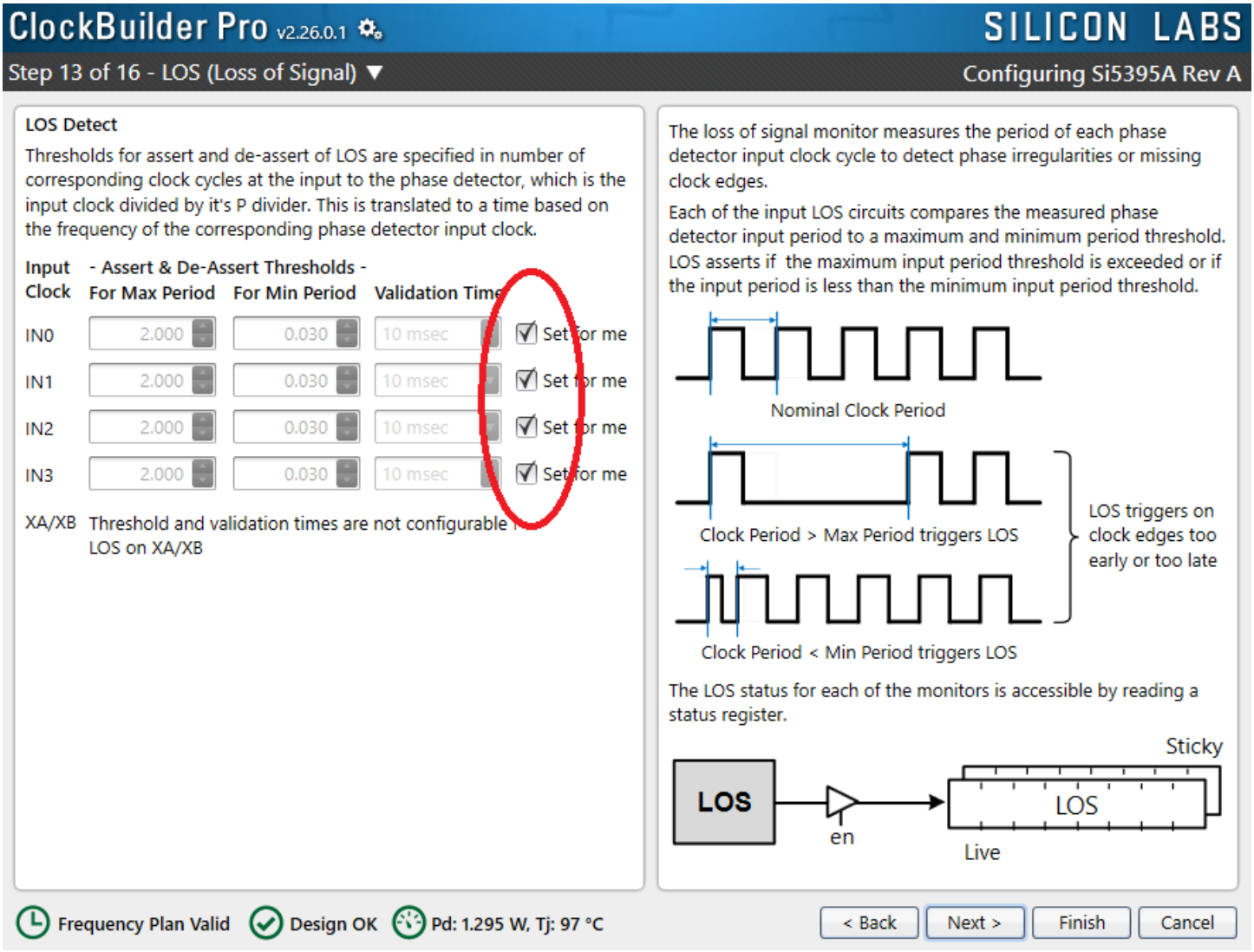


Figure 3.7. "Set for me" LOS Settings

3.7 CBPro – DSPLL Window OOF

The OOF reference is selected in the top pull-down menu shown in the figure below. Precision and Fast OOF can be independently enabled and have independent set and clear (i.e., de-assert or negate) thresholds. The set threshold should always be at least slightly greater than the negate threshold to avoid alarm chattering.

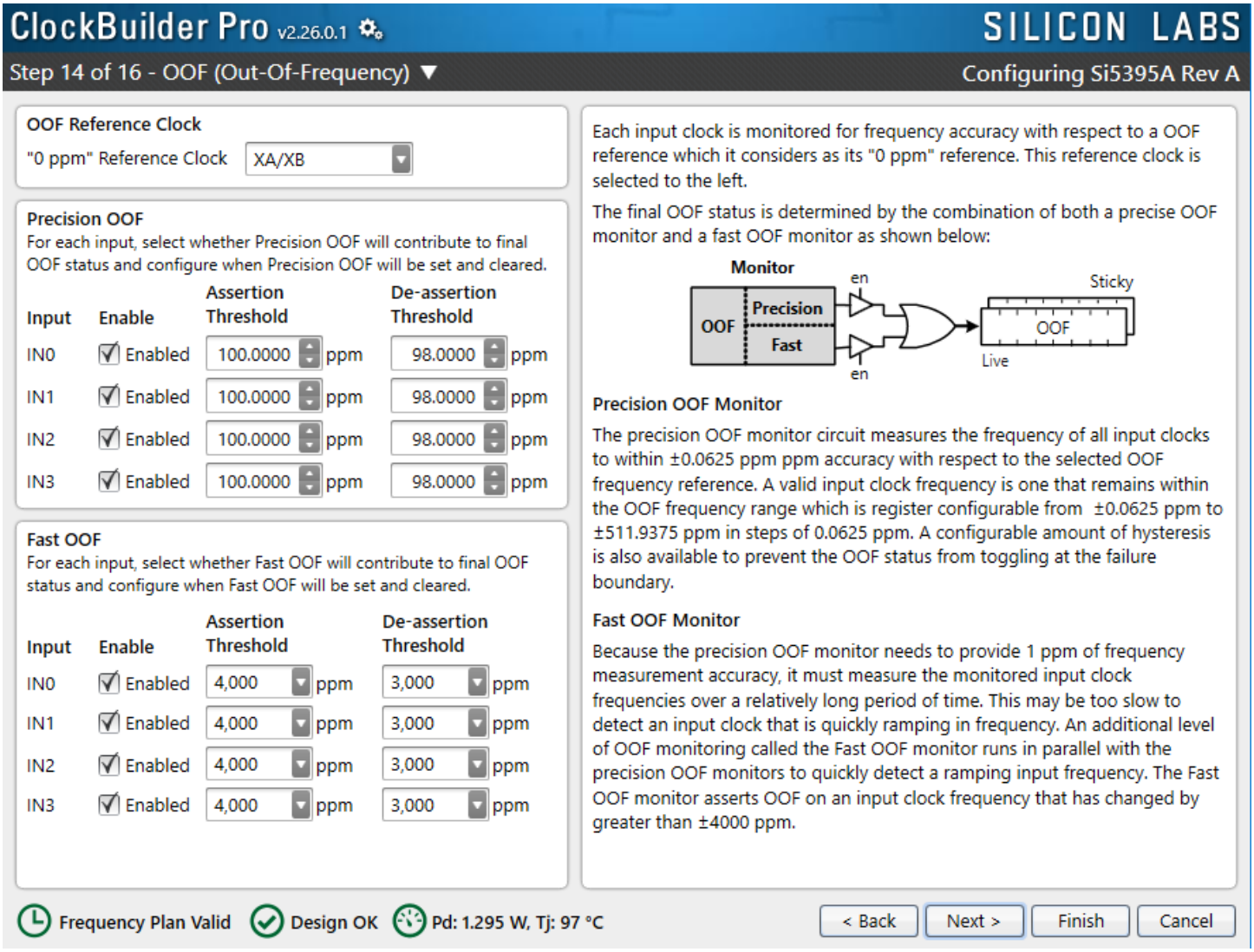


Figure 3.8. OOF Reference Window

3.8 CBPro – DSPLL Window Interrupt Pin

When the alarm register bits are read, the value of the alarm at the time of the register read will determine what is read. Each of the alarms goes to its corresponding flag bit. The flag bits are set by the alarm bit being asserted, and the flag bit will stay set until it is cleared by the serial port writing to zero to the flag bit. Each flag bit has a corresponding mask bit that will either pass the flag bit value to the interrupt pin or block it from the interrupt pin. These bits are shown in the following figure.

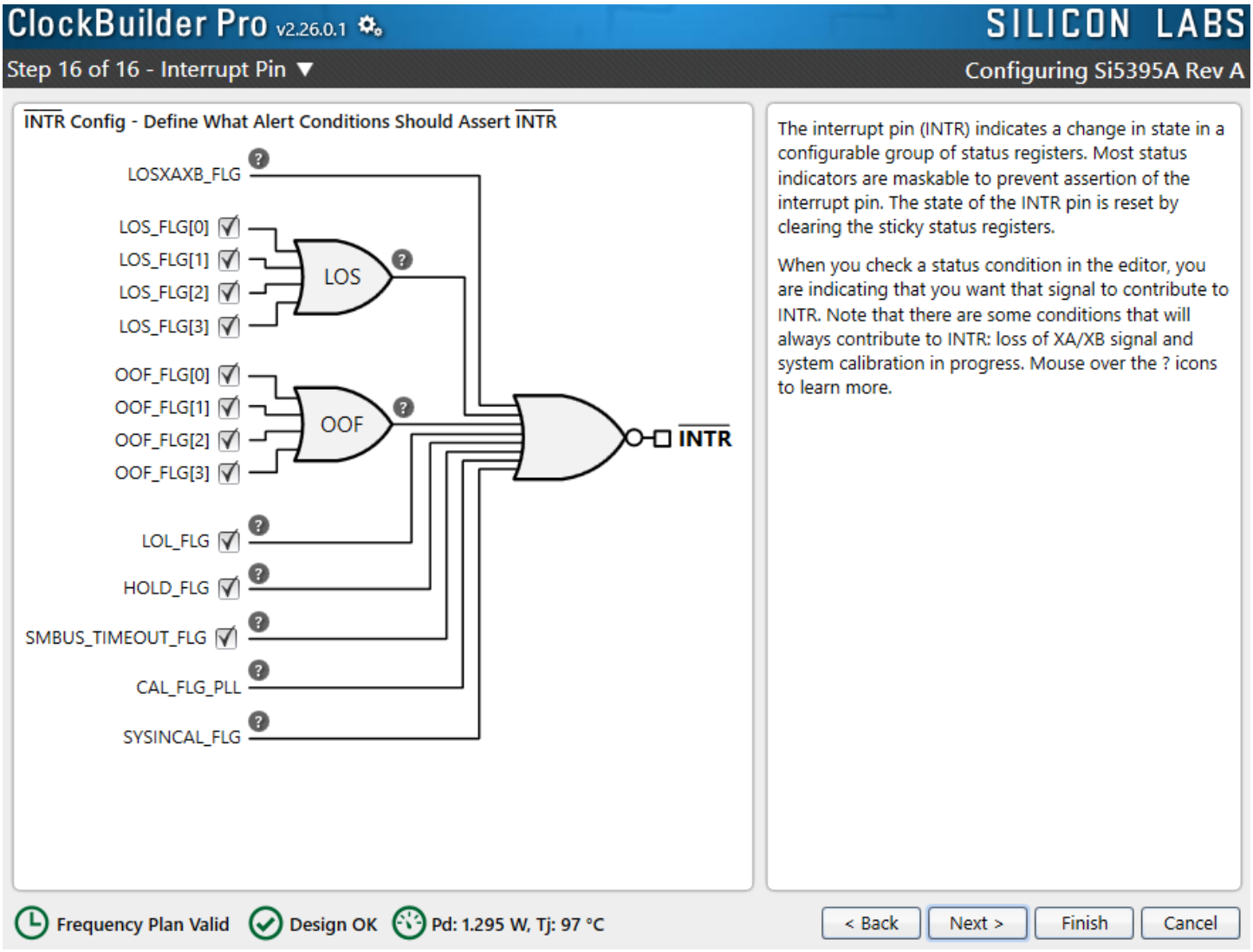
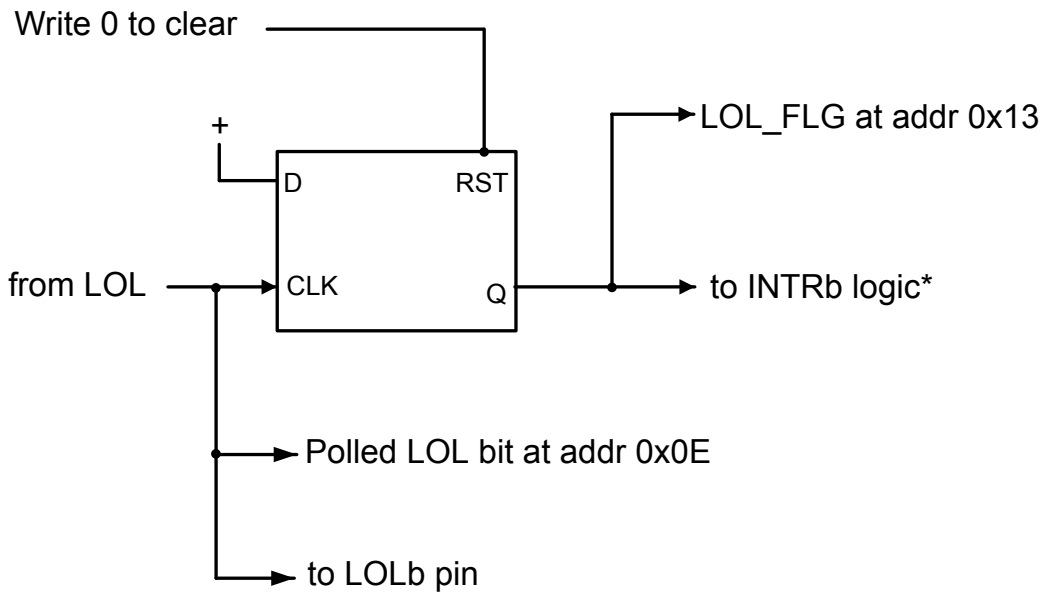


Figure 3.9. DSPLL Interrupt Window

4. Status Pins

All of the OOF, LOS, and LOL alarms have their own status flag bits that are “sticky”, i.e., once they are set, they stay set until manually cleared. As an example, the figure below explains this logic for LOL. It also applies to all of the other alarm/status bits, although some may not be connected to physical pins.



*Refer to Figure 1.2 Logical Flow of LOS/OOF Status Bits from Input Clocks to Phase Detector on page 3.

Figure 4.1. Status Pins Example

Each of the status flag bits then goes to the interrupt pin logic described in the figure above. Each flag bit can be individually masked from the interrupt pin.

5. Related Literature

This white paper references the following software and documents:

- ClockBuilder Pro (CBPro) Software
- Si5395/94/92 Family Reference Manual
- Crystal Reference Manual (Grades A/B/C/D/P only)
- AN561: Introduction to Gapped Clocks and PLLs
- AN1057: Hitless Switching using Si534x/8x Devices
- AN1111: DSPLL Input Clock Expander