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A Highly Compact 2.4GHz Passive 6-bit Phase Shifter with Ambidextrous Quadrant Selector

Mackenzie Cook, *Member, IEEE*, John W. M. Rogers, *Senior Member, IEEE*

***Abstract*—An extremely compact architecture for a passive 6-bit digital phase shifter is presented. The phase shifter has a range of 360° with 5.6° resolution at 2.4GHz. The architecture is composed of an ambidextrous quadrant selector in series with a digital fine-tuned phase shifter which makes use of high-ratio symmetrical digitally variable capacitors loading a lumped element transmission line. The phase shifter achieves a 50Ω match in all 64 states. The circuit occupies approximately 0.47mm^2 on die, and the entire test chip measured 0.84mm^2 including bond pads and ESD structures. The 1-dB compression point was +23dBm. The chip was fabricated in a commercial 0.13µm SOI (Silicon-on-Insulator) CMOS process.**

***Index Terms*—Phase Shifter, Varactor, Variable Capacitors, Quadrant Selector.**

I. Introduction

PHASE shifting is an important operation in many RF applications. Phase Shifters are commonly used in signal cancellers and equalizers [1]. Phase shifters are also used in beam steering, where a phased antenna array directs the antenna energy in a desired direction, which is commonly used in radar and non-line-of-sight (NLOS) operations [2]. In dynamic gain equalizers, phase shifters are used to fit the attenuation profile of the equalizer to a desired one to compensate for non-flat gain responses across a communication band [1].

This paper outlines the design of a highly compact phase shifter comprised of a digitally tuned transmission line and an ambidextrous quadrant selector. In section II, the basic theory surrounding lumped element transmission lines will be highlighted, paving the way for Section III where the architectures for a novel quadrant selector and a fine tuning phase shifter are explained. Section IV presents measured results and compares them to theory and other state of the art phase shifters currently in the literature.

II. Basic Theory

A lumped element quarter wave transmission line, shown in Fig. 1, has a characteristic impedance, $Z_{0,}$ given by

$$Z_0 = \sqrt{\frac{L}{C}}, \tag{1}$$

and a corner frequency, ω_o, given by

$$\omega_O = \frac{1}{\sqrt{LC}}. \tag{2}$$

A change in inductance or capacitance will change the corner frequency of the system, and thus the phase of the signal at the output will change as well. Inductance is not easily altered; however, capacitance is variable with an appropriate device, such as a MOS varactor. Therefore, in a lumped element transmission line, utilizing a variable capacitance will alter the phase of the signal at the output.

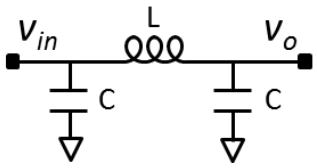

Fig. 1. A lumped element transmission line

A lumped element circuit from Fig. 1 will have a low pass response up to the corner frequency response indicated in (2). Prior to this frequency the gain response is fairly flat, but phase will be changing. As a result, the phase can be altered while the gain of the system remains relatively flat by changing the corner frequency of the system within the pass band region close to the corner frequency.

Using a fine tuning system by altering the corner frequency of a circuit similar to Fig. 1 will enable fine tuning. In order to cover 360°, a coarse tuning will be needed as well. A logical choice for coarse phase shifting is 90°. With a fixed L, C and Z_0, the electrical length of a lumped transmission line will be constant at a given frequency. Using several fixed quarter wave (90°) transmission lines, different quadrants (0°, 90°, 180°, 270°) can be selected using switches to obtain the coarse phase shift. This would yield 360° total range when paired together with a variable capacitor loaded transmission line.

III. Architecture

A. Ambidextrous Quadrant Shifter

A simple way to design a quadrant shifter is to construct it using fixed quarter wave transmission lines can be switched in or out to select the quadrant desired. To select the four quadrants, one would need three quarter wave sections selectable by switches. With three sections, there would be three inductors which are the main area consumer in this circuit.

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The architecture shown in Fig. 2 employs extensive inductor reuse in combination with switches to accomplish the same goal with two inductors instead of three. It does so by electrically reconfiguring the circuit's inductors between series and parallel connections to make use of left handed lumped transmission lines, which provide the opposite phase shift of the right handed version shown in Fig. 1. The architecture selects between bypass, single right handed quarter wave, double right handed quarter wave, and single *left handed* quarter wave states, which provides 0°, –90°, –180°, and +90° of phase shift respectively. The architecture is shown in Fig. 2, followed by a description of each quadrant state.

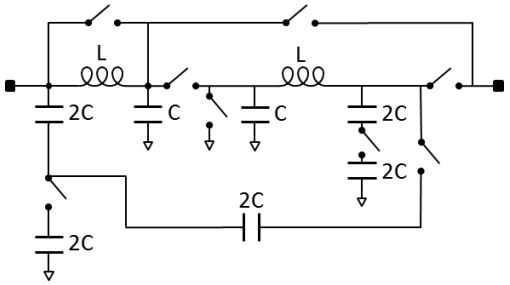

Fig. 2. An ambidextrous quadrant selector, L=3.32nH, C=1.32pF

1) *Bypass, 0°*
   In the bypass state, shown in Fig. 3a, both bypass switches are on and all others are opened. Note that one shunt capacitor C to ground could also be removed with another switch, but in practice this proved to be unnecessary.
2) *Single Quarter Wave Transmission Line, –90°*
   A single right handed transmission line in Fig. 3b is formed by creating a shunt C at the input, and activating the bypass switch at the output.
3) *Double Quarter Wave Transmission Line, –180°*
   Both bypass switches are opened and two series quarter wave transmission lines are formed to produce a 180° phase shift, seen in Fig. 3c.
4) *Left-Handed Quarter Wave Transmission Line, +90°*
   Both inductors are shunted to ground from the input and output using a switch to ground in the middle of the circuit. A series capacitance C is created using the series combination of the capacitance 2C at the input and 2C connecting to the output through a closed switch. The previously shunted capacitance 2C to ground is disconnected by opening the shunt switch at the input. This creates a left handed transmission line with two series capacitors of 2C, creating C, and two shunt inductors to ground. This is shown in Fig. 3d.

In addition to a significant area reduction, this design will also provide a more consistent loss between states and a lower maximum loss than the simple method of three quarter wave transmission lines. This architecture would have the most loss in the double transmission line state, rather than triple in the other method.

B. Fine Phase Shifter

The fine tuning phase shifter is comprised of two series lumped element transmission lines from Fig. 1, where the capacitors are replaced with variable capacitors to enable tuning. This is shown in Fig. 4.

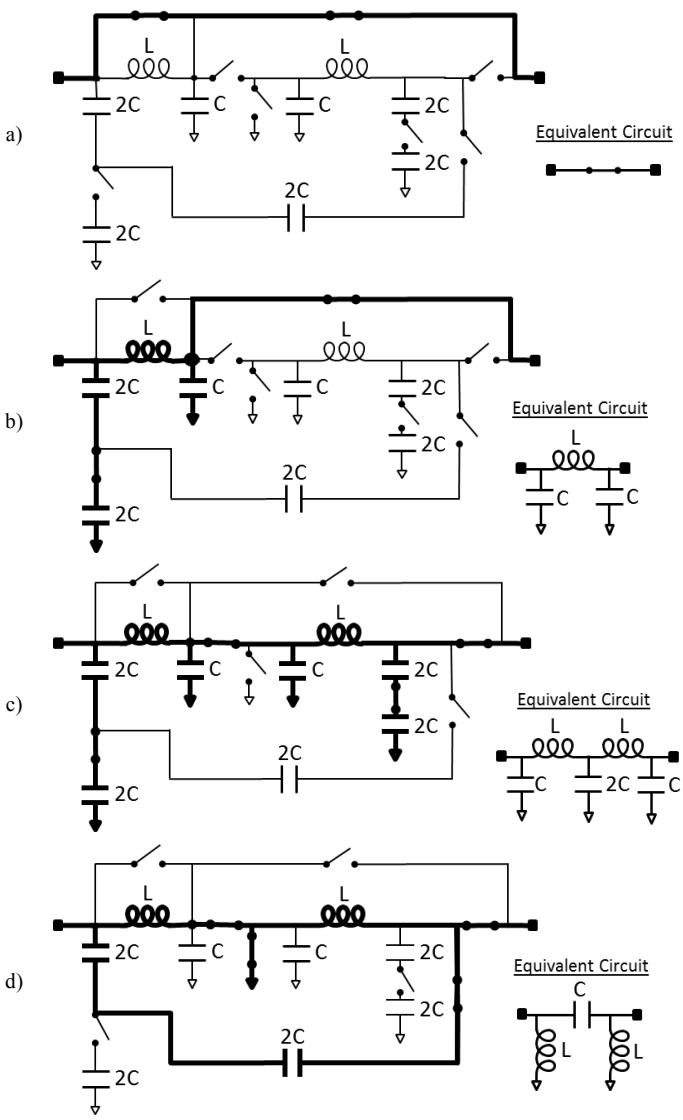

Fig. 3. Quadrant selector state and equivalent circuit of: a) Bypass, b) –90°, c) –180° , and d) +90°

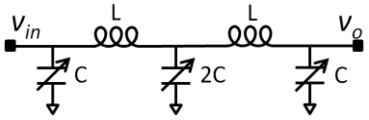

Fig. 4. Fine Shifter architecture composed of dual tuned transmission lines. L=3.32nH

The architecture makes use of high-ratio variable capacitors described in the next section in order to achieve 90° of total phase shift while maintaining a 50Ω match with only two inductors. The capacitors are 4-bit, enabling approximately 6° resolution for 90° of total phase shift.

The theoretical phase shift vs. capacitance can be derived from Fig. 4 using Kirchoff's Voltage Law. Assuming a 50Ω voltage source at V_{in} and 50Ω load at V_0, the transfer function V_{out}/V_{source} can be expressed in terms of impedances in (3). When substituting $Z_C = (sC)^{-1}$ and $Z_L = sL$ into (3), the Laplace transfer function in (4) is obtained. Finally, substituting $s = j\omega$ and factoring into Cartesian form in the denominator, (5) is obtained.

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Using (1) and (2), and assuming a 50Ω transmission line at 2.4GHz, will yield L = 3.32nH and C = 1.32pF for a fixed quarter wave transmission line. Using this inductance value at 2.4GHz, the phase shift is found by solving (5) for the angle of V_{OUT}/V_{IN} at various capacitances. This is illustrated in Fig. 5. Note that angles have been artificially constrained to ±180°, the circuit does not advance the phase.

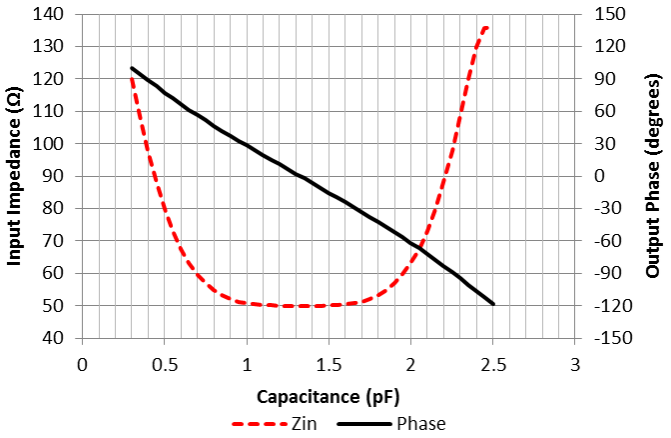

Fig. 5. The input impedance and output phase of the fine shifter versus capacitance

The resulting phase shift is quite linear with respect to capacitance over a large range, which will allow for a binary weighted digital capacitor to control the phase shift in a linear fashion.

As an example, using ideal devices in Fig. 5, 90° of phase occurs between 0.5pF and 1.5pF, for a C_{MAX}:C_{MIN} of 3:1, similar to MOS varactors [3]. For a 360° application paired with a quadrant selector, some margin would be needed to ensure no gaps occur from using real components and due to process variation, so a target starting design of at least 100° is selected. In addition, on chip devices are far from ideal, therefore a variable capacitance with a ratio larger than 3:1 will be needed to reach 90° with two transmission line segments.

The input match is extremely important for RF applications. Using Fig. 4, Z_{IN}, which is equal to Z_{OUT}, can be found as:

$$Z_{IN} = Z_C \parallel \left(Z_L + \left(\frac{Z_C}{2} \parallel \left(Z_L + (Z_C \parallel 50) \right) \right) \right) \quad (6)$$

When (6) is simplified into Cartesian form and solved for magnitude, the input impedance for the 2.4GHz phase shifter is shown in Fig. 5.

For RF applications this design is advantageous due to a consistent 50Ω match over a large range of capacitance values.

C. *High Ratio Switched Variable Capacitors*

This design aimed to have a very low area use. Traditional MOS varactors typically have a C_{MAX}:C_{MIN} near 3:1 [3]. By using real components with MOS varactors instead of ideal components as previously explored, the capacitance ratio would be insufficient to achieve greater than 90° of phase shift with two transmission line segments. Such a design would therefore require three series transmission lines to reach 90° of phase shift. However, if there were a variable capacitance with a higher ratio, a larger phase shift would be attainable and using two sections would become feasible. This would reduce the area considerably by being able to use two sections instead of three as compared to using MOS varactors.

A switchable capacitance is shown in Fig. 6. By using switches which are DC decoupled with fixed capacitors in parallel, capacitance can be added or removed digitally. The switches are *cross biased* [4], where the channel and gate are biased to opposite potentials using an inverter and large resistors as seen in in grey in Fig. 6.

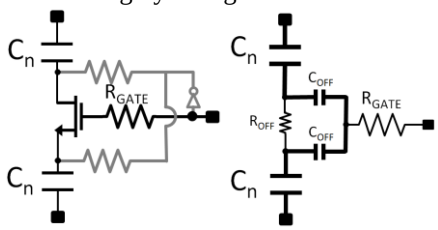

Fig. 6. A cross-biased switch, left, where gate and channel are inversely biased via an inverter, and equivalent circuit when gate is low (off), right. R_{GATE} = 10kΩ

The benefit to this technique is maximizing the power handling capability of the switch [4], while presenting a desired capacitance step ($C_{ON} - C_{OFF}$). The gate and channel (drain/source) are always biased to opposite potentials. This enables high and consistent linearity in both closed and open states. When comparing to a single capacitor on the drain, with source grounded directly, the linearity in the open state is degraded by 10-20dB in simulation (depending on drain bias level V_D) compared to the cross biased case. This is due to the open state having $V_{GS} = -V_{DD}$ and $V_{DS} = 0$ while cross biased, compared to $V_{GS} = 0$ and $V_{DS} = V_D$ in the single capacitor architecture. In other words, $V_{GS}–V_{th}$ is much more negative while cross biased than with a single capacitor, allowing for a much larger signal at the drain before the FET turns on. This architecture would also be highly useful in differential applications. An example of this occurs in [5], where this topology is used to improve VCO switched tuning.

In a case where the linearity is less important, a designer will gain significant area efficiency by using a single capacitor instead of two.

The architecture of a 4-bit variable capacitor is shown in Fig. 7.

$$\frac{V_{out}}{V_{in}} = \left(\frac{Z_C \parallel 50}{Z_L + Z_C \parallel 50} \right) \left(\frac{\frac{Z_C}{2} \parallel (Z_L + (Z_C \parallel 50))}{Z_L + \left(\frac{Z_C}{2} \parallel (Z_L + (Z_C \parallel 50)) \right)} \right) \left(\frac{Z_C \parallel \left(Z_L + \left(\frac{Z_C}{2} \parallel (Z_L + (Z_C \parallel 50)) \right) \right)}{50 + Z_C \parallel \left(Z_L + \left(\frac{Z_C}{2} \parallel (Z_L + (Z_C \parallel 50)) \right) \right)} \right) \quad (3)$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{25}{2500C^3L^2s^5 + 100C^2L^2s^4 + (7500C^2L + CL^2)s^3 + 200CLs^2 + 5000Cs + Ls + 50} \quad (4)$$

$$\frac{V_{out}}{V_{in}} = \frac{25}{100C^2L^2\omega^4 - 200CL\omega^2 + 50 + j(2500C^3L^2\omega^5 - (7500C^2L + CL^2)\omega^3 + (5000C + L)\omega)} \quad (5)$$

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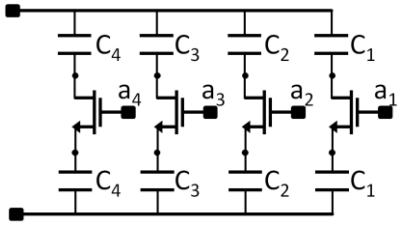

Fig. 7. A 4-bit symmetric digitally variable capacitor. C_1=200fF, C_2=350fF, C_3=730fF, C_4=1.35pF. L=120nm, $W_{1,2}$=100µm, $W_{3,4}$=300µm.

In Fig. 7, a change in capacitance, ΔC_n, is toggled using the control signal a_n at the gate of a respective switch. The desired capacitance step is the difference between two C_n in series with the R_{ON} of the switch, and two C_n and two C_{OFF} in series as seen in Fig. 6. The latter assumes a large R_{GATE} resistor and a large R_{OFF} of the switch. C_{OFF} is the capacitance between source/drain and gate when the switch is off as shown in Fig. 6. The difference ΔC_n can be expressed as:

$$\Delta C_n = \frac{C_n}{2} - \frac{C_n C_{OFF}}{2(C_n + C_{OFF})} \quad (7)$$

C_n can be chosen to provide the desired capacitance steps, and the number of bits is fully expandable. This design would have a C_{MAX}:C_{MIN} dependent of the selected C_n and only limited at the low end by C_{OFF}. Therefore, a large highly-linear capacitance ratio can be achieved using this architecture.

D. Complete Phase Shifter

The complete phase shifter is comprised of the Ambidextrous Quadrant Selector in Fig. 2 in series with the fine shifter in Fig. 4. The design is 6-bit for a total of 64 phases across 360°. The circuit is entirely passive and only draws current when changing states.

IV. Measured Results

The measured performance of the phase shifter was obtained with a network analyzer. The micrograph of the fabricated chip is shown in Fig. 8. The on chip area is approximately 0.47mm^2, and the total area of the test die including bond pads and ESD is 0.84mm^2. The dimensions are 1400µm x 600µm.

The phase shift performance at 2.4GHz is shown in Fig. 9. The phase shifter achieves linear monotonic phase shift with an average phase step of 5.84° and a total phase range of 372°. S_{21}(dB) performance is shown in Fig. 10. S_{21} is fairly consistent, varying between -3.5 and -7.1dB at its extremes, or 5.3±1.8dB. The RMS amplitude error between 2.2GHz and 2.7GHz is 1.72±0.02dB. The return loss performance is shown in Fig. 11. The phase shifter remains well matched at 2.4GHz over all phases at both the input and the output terminals. The frequency response for STEP=0 is shown in Fig. 12. The phase shifter is well matched (< −10dB) in this state from 1.7GHz to 2.8GHz and has a pass band of 400MHz – 2.8GHz.

The RMS phase error is shown in Fig. 13. This phase shifter was designed for accurate quadrants with less importance on quadrant to quadrant accuracy. As a result, the quadrant RMS phase error is also included. The RMS error of each quadrant ranges from 0.5^0 to 1.7^0 in each quadrant at 2.4GHz, with the full range having 3.6^0 RMS phase error at 2.5GHz. The phase shifter is effective over a range of 2.3-2.6GHz. Although the quadrant error remains low at 2.2GHz, the quadrants diverge significantly, contributing to a high total RMS error.

The power handling capability is shown in Fig. 14. The measured single tone 1-dB compression point is +23dBm.

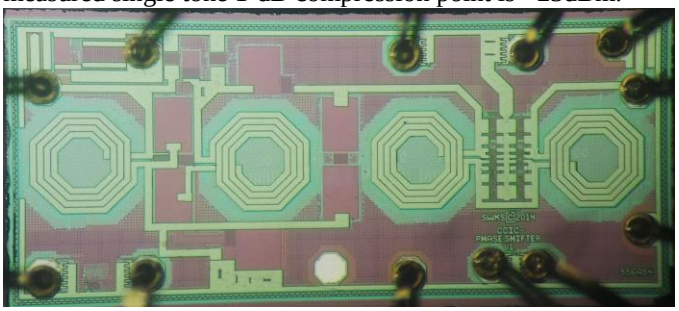

Fig. 8. Phase shifter micrograph

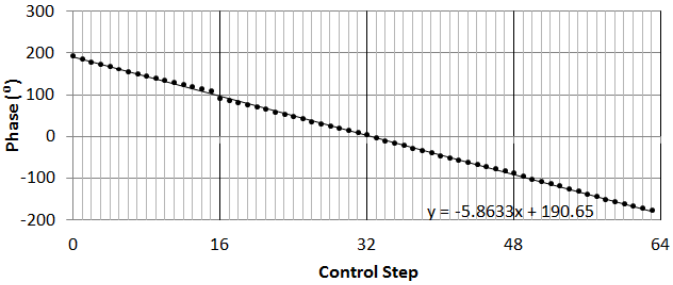

Fig. 9. The measured phase shift (S_{21} phase) vs. control step with trend-line

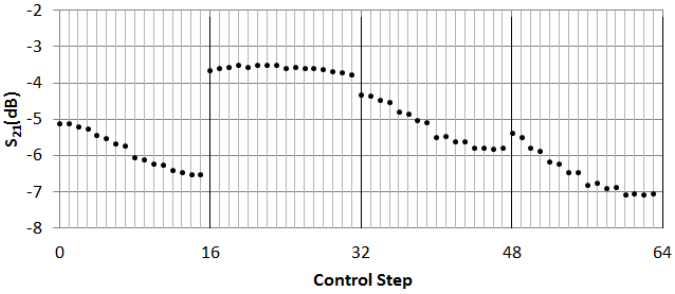

Fig. 10. The measured S_{21}(dB) performance vs. control step

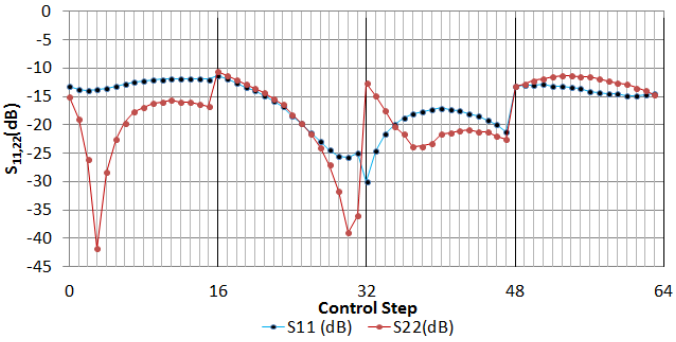

Fig. 11. The measured phase shifter return loss (dB) vs. control step

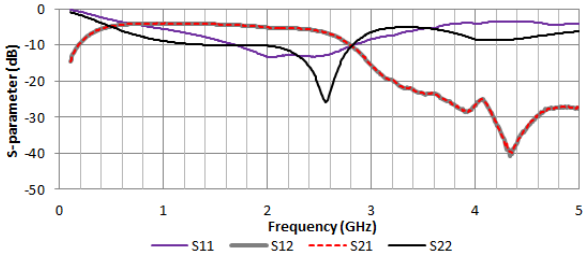

Fig. 12. The measured frequency response (STEP=0) from 100MHz to 5GHz

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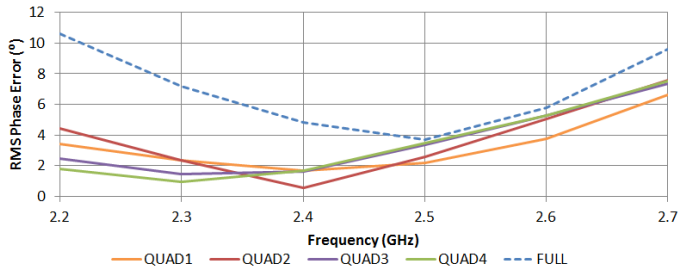

Fig. 13. The measured RMS phase error of each quadrant and over the full range.

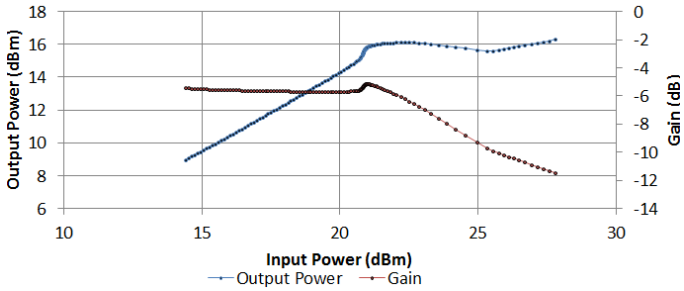

Fig. 14. Output power and gain versus input power (STEP=0) at 2.4GHz. The measured P_{1dB} was +23dBm.

A comparison of this work to state of the art published works is found in Table I. The presented phase shifter has competitive but not state-of-the-art insertion loss. However, for all compared digital phase shifters, this work occupies nearly six times less area than the best of all works found and presents a significant advancement in area efficiency for passive digital phase shifters at 2.4GHz. When comparing to the most area efficient work in similar frequency ranges of at least 6 bits, [7] occupies the least area at 3.1mm^2. This work is an approximate 600% improvement in area efficiency over the previous state of the art.

TABLE I
PHASE SHIFTER PERFORMANCE COMPARISON

	Freq. (GHz)	No. of Bits	Insertion Loss (dB)	Area (mm^2)	Technology
----	**2.3-2.6**	**6**	**5.3±1.8**	**0.47**	**130nm SOI CMOS**
[7]	2.5-3.2	6	13*	3.1**	180nm CMOS
[8]	1.4-2.4	6	3.8±0.4	3.8	0.5µm GaAs pHEMT
[9]	1.4-2.4	4	3.8±0.4	2.6	400nm GaAs
[6]	1.4-1.7	9	9.3±3.3	5.94	250nm SOS
[6]	1.8-2.4	10	5.1±2.2	3.4	250nm SOS

*Without amplification (active), **Estimate taken from [6] based on die photograph in [7]

SOS = Silicon on Sapphire, pHEMT = p-High Electron Mobility Transistor

Binarily increasing passive phase shift circuits are switched in and out in [8], resulting in a low phase error and wide bandwidth in exchange for large area consumption. This work has comparable phase error but over a much lower bandwidth. The 2.6mm^2 circuit in [9] had the smallest area found, however this was a 4-bit phase shifter. The work also implemented fixed phase shift segments, resulting in high area consumption but wideband operation. Additionally, by using fixed instead of variable cells, the corner frequencies can be designed such that no adverse insertion loss reduction occurs, unlike this work. In exchange for high tuning range, which required near-corner tuning, this work suffers from larger and more variable insertion loss compared to [8] and [9].

The designs in [6], in contrast, were similar to this work. The authors utilized a capacitively loaded lumped element transmission line with switchable capacitors to facilitate the phase shift instead of fixed phase shift segments. These works have a larger area, insertion loss, and lower bandwidth than [8] and [9], but obtain higher resolution. The fixed 45° phase sections with a variable phase network are very similar to this work, however the variable shift of 22.5° with several fixed 45° sections requires many inductors. The higher resolution is a result of using a finer resolution capacitor array, something not focused on in this work. An extended version of this work, with higher resolution capacitors, would be able to achieve the claimed resolution in [6] with lower area consumption due to its extremely economical use of inductors.

There have been a number of noteworthy 60GHz phase shifters recently designed [10–12], however, for the purposes of worthwhile comparison to this work, only phase shifters near the band of interest are compared.

V. CONCLUSION

An extremely compact yet high performance 6-bit phase shifter has been designed. It offers performance comparable to other state of the art phase shifters yet occupies more than 80% less area. This work presents a significant advancement in area efficiency while providing excellent matching, low RMS phase error, and low insertion loss.

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