

AN699: FPGA Reference Clock Phase Jitter Specifications

Driven by market demand for ever-increasing network bandwidth, high-speed digital communications equipment manufacturers look to communication semiconductor suppliers for the latest in high-speed standards-based digital communications protocol building blocks. Several Field Programmable Gate Array (FPGA) vendors have taken up this challenge and produced products specifically targeted to various segments of high-speed serial digital communications designs. As a result, communications and embedded computing product designs are increasingly utilizing FPGAs with embedded serializer-deserializers (SerDes) for critical high-speed transceiver and serial protocol processing. Within high-speed serial digital communications, controlling, reducing, and maintaining low jitter in signal path is a paramount concern, especially as bit rates increase into the multi-gigabit realm and beyond. FPGA vendors and system designers alike have become increasingly aware that low jitter digital communications absolutely require low or ultra-low jitter clocks. Skyworks timing solutions can easily meet the low jitter clocking requirements for high-speed serial digital communications.

KEY POINTS

- Phase noise masks for Intel/Xilinx FPGAs with phase noise performance of Skyworks timing devices
- Phase noise comparison plots of different Skyworks devices
- Guide to choose a timing chip to meet performance requirements for specific FPGAs

Table of Contents

- 1. FPGA Clock Jitter Requirements 3
- 2. Recommendations 20

1. FPGA Clock Jitter Requirements

The vast majority of the FPGA market share is split between two companies, Xilinx and Intel (formerly Altera). These two companies have FPGA products that specifically address various high-speed serial digital communications market segments. As a result of this market focus, these FPGA companies have published specifications for input reference clock jitter requirements that allow their FPGA based products to implement spec-compliant serial digital communications protocols.

The two documents below summarize recommended Skyworks timing solutions for FPGA families vs. Industry Standard Interfaces.

- [Timing Solutions for Xilinx FPGAs](#)
- [Timing Solutions for Intel FPGAs](#)

Although clock jitter can be specified in different forms, the almost universally accepted format for high-speed serial digital communications links is that of a phase noise (jitter) mask in the frequency domain. (For an excellent technical explanation of jitter and phase noise, refer to Skyworks' application note "[AN687: A Primer on Jitter, Jitter Measurement and Phase-Locked Loops](#)".) Tables 1.1, 1.2, 1.3 and 1.4 below provide the input reference clock phase noise mask specifications published by the two main FPGA vendor's products targeted for use in high-speed serial digital communications. In addition to these phase noise requirements, the tables also provide the phase noise performance for various Skyworks' timing devices.

As shown in the following tables, the specified Skyworks timing devices meet the FPGA's input reference clock jitter requirements often with substantial margin and are well suited for use in high-speed digital serial communications applications.

The selected devices include the Si540/545 XO, Si53x/Si570 any frequency programmable XO, Si56x VCXO, the Si5332/35/38/40/41/Si5391P any frequency, any-output clock generators, Si5342/44/45/46/47/Si5392/94/95/96/97 any-frequency jitter attenuating clocks and the Si5348/Si5383/89/M88 IEEE 1588 module network synchronizers.

Table 1.1. Xilinx FPGA Specifications vs Skyworks Clock Generators, Jitter Attenuators & Network Synchronizers

Xilinx FPGA			Clock Generator			Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)		
			Si5332	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module		
Xilinx ULTRASCALE+ VIRTEX / KINTEX GTY CPLL/QPLL VIRTEX GTM LCPLL			Skyworks									
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-112	-128	-136	-136	-137	-134	-136	-136	-137	
		100	-128	-135	-144	-148	-144	-144	-144	-144	-143	
		1000	-149	-149	-151	-153	-151	-151	-151	-151	-151	-150
		5000	-145 / CPLL only	-154	-164	-164	-164	-160	-163	-160	-160	-160
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-103	-122	-131	-130	-131	-130	-130	-131	-131	
		100	-123	-129	-136	-140	-138	-139	-139	-139	-138	
		1000	-143	-143	-146	-146	-145	-145	-150	-145	-145	-144
		5000	-145 / CPLL only	-153	-162	-162	-162	-157	-159	-157	-157	-157

Xilinx FPGA				Clock Generator			Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)
				Si5332	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-98	N/A	-124	-125	-125	-123	-124	-124	-124
		100	-117	N/A	-133	-135	-133	-133	-134	-133	-133
		1000	-140	N/A	-136	-140	-139	-139	-137	-144	-138
		5000	-144 / CPLL only	N/A	-159	-159	-158	-154	-154	-154	-154
Xilinx ULTRASCALE+ KINTEX GTH CPLL/ QPLL				Skyworks							
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-105	-122	-131	-130	-131	-130	-130	-131	-131
		100	-124	-129	-136	-140	-138	-139	-139	-139	-138
		1000	-130	-143	-146	-146	-145	-145	-150	-145	-144
		5000	-140 / CPLL only	-153	-159	-161	-159	-156	-159	-156	-156
Xilinx ULTRASCALE VIRTEX/ KINTEX GTH QPLL/ CPLL				Skyworks							
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-105	-122	-131	-130	-131	-130	-130	-131	-131
		100	-124	-129	-136	-140	-138	-139	-139	-139	-138
		1000	-130	-143	-146	-146	-145	-145	-150	-145	-144
		50000	-140 / CPLL only	-156	-162	-162	-162	-157	-162	-157	-157
Xilinx ULTRASCALE VIRTEX GTY CPLL/ QPLL				Skyworks							
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-112	-128	-136	-136	-137	-134	-136	-136	-137
		100	-128	-135	-144	-148	-144	-144	-144	-144	-143
		1000	-145	-149	-151	-153	-151	-151	-151	-151	-150
		50000	-145 / CPLL only	-157	-164	-164	-164	-160	-164	-160	-160
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-103	-122	-131	-130	-131	-130	-130	-131	-131
		100	-123	-129	-136	-140	-138	-139	-139	-139	-138
		1000	-143	-143	-146	-146	-145	-145	-150	-145	-144
		50000	-145 / CPLL only	-156	-162	-162	-162	-157	-162	-157	-157

Xilinx FPGA				Clock Generator			Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)
				Si5332	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-98	N/A	-124	-125	-125	-123	-124	-124	-124
		100	-117	N/A	-133	-135	-133	-133	-134	-133	-133
		1000	-140	N/A	-136	-140	-139	-139	-137	-144	-138
		50000	-144 / CPLL only	N/A	-159	-159	-158	-154	-158	-154	-154
Xilinx Series 7 GTX/GTH QPLL				Skyworks							
Ref Clock Frequency 100 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-126	-133	-139	-140	-139	-140	-140	-138	-140
		100	-130	-140	-148	-150	-147	-148	-148	-148	-148
		1000	-134	-153	-154	-155	-153	-154	-153	-154	-154
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-123	-130	-138	-138	-137	-138	-137	-138	-138
		100	-129	-137	-146	-148	-144	-147	-146	-146	-145
		1000	-133	-150	-153	-154	-151	-152	-152	-153	-153
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-122	-128	-136	-136	-137	-134	-136	-136	-137
		100	-127	-135	-144	-148	-144	-144	-144	-144	-143
		1000	-132	-149	-151	-153	-151	-151	-151	-151	-151
Ref Clock Frequency 250 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-119	-124	-131	-132	-133	-131	-131	-132	-131
		100	-126	-132	-137	-140	-137	-137	-137	-138	-137
		1000	-131	-145	-147	-148	-145	-147	-146	-147	-146
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-115	-122	-131	-130	-131	-130	-130	-131	-131
		100	-124	-129	-136	-140	-138	-139	-139	-139	-138
		1000	-130	-143	-146	-146	-145	-145	-150	-145	-144
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-110	N/A	-124	-125	-125	-123	-124	-124	-124
		100	-116	N/A	-133	-135	-133	-133	-134	-133	-133
		1000	-120	N/A	-136	-140	-139	-139	-137	-144	-138
Xilinx Series 7 GTX/GTH/GTP CPLL				Skyworks							

Xilinx FPGA				Clock Generator			Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)
				Si5332	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module
Ref Clock Frequency 100 (MHz)	Frequency	10	-126	-133	-139	-140	-139	-140	-140	-138	-140
	Offset (kHz)	100	-132	-140	-148	-150	-147	-148	-148	-148	-147
	Phase noise dBc/Hz	1000	-136	-153	-154	-155	-153	-154	-153	-154	-153
Ref Clock Frequency 125 (MHz)	Frequency	10	-123	-130	-138	-138	-137	-138	-137	-138	-138
	Offset (kHz)	100	-131	-137	-146	-148	-144	-147	-146	-146	-145
	Phase noise dBc/Hz	1000	-135	-150	-153	-154	-151	-152	-152	-153	-151
Ref Clock Frequency 156.25 (MHz)	Frequency	10	-121	-128	-136	-136	-137	-134	-136	-136	-137
	Offset (kHz)	100	-129	-135	-144	-148	-144	-144	-144	-144	-143
	Phase noise dBc/Hz	1000	-133	-149	-151	-153	-151	-151	-151	-151	-150
Ref Clock Frequency 250 (MHz)	Frequency	10	-119	-124	-131	-132	-133	-131	-131	-132	-131
	Offset (kHz)	100	-126	-132	-137	-140	-137	-137	-137	-138	-137
	Phase noise dBc/Hz	1000	-132	-145	-147	-148	-145	-147	-146	-147	-146
Ref Clock Frequency 312.5 (MHz)	Frequency	10	-116	-122	-131	-130	-131	-130	-130	-131	-131
	Offset (kHz)	100	-124	-129	-136	-140	-138	-139	-139	-139	-138
	Phase noise dBc/Hz	1000	-131	-143	-146	-146	-145	-145	-150	-145	-144
Ref Clock Frequency 625 (MHz)	Frequency	10	-110	N/A	-124	-125	-125	-123	-124	-124	-124
	Offset (kHz)	100	-119	N/A	-133	-135	-133	-133	-134	-133	-133
	Phase noise dBc/Hz	1000	-127	N/A	-136	-140	-139	-139	-137	-144	-138
Xilinx Spartan 6				Skyworks							
Ref Clock Frequency 100 (MHz)	Frequency	10	-112	-133	-139	-140	-139	-140	-140	-138	-140
	Offset (kHz)	100	-130	-140	-148	-150	-147	-148	-148	-148	-147
	Phase noise dBc/Hz	1000	-130	-153	-154	-155	-153	-154	-153	-154	-153
		10000	-135	-159	-165	-164	-164	-160	-164	-161	-161

Xilinx FPGA			Clock Generator				Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)
			Si5332	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module	
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-120	-130	-138	-138	-137	-138	-137	-138	-138
		100	-130	-137	-146	-148	-144	-147	-146	-146	-145
		1000	-130	-150	-153	-154	-151	-152	-152	-153	-151
		10000	-135	-158	-164	-164	-164	-160	-164	-161	-160
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-120	-128	-136	-136	-137	-134	-136	-136	-137
		100	-130	-135	-144	-148	-144	-144	-144	-144	-143
		1000	-130	-149	-151	-153	-151	-151	-151	-151	-150
		10000	-135	-157	-164	-164	-164	-160	-163	-160	-160

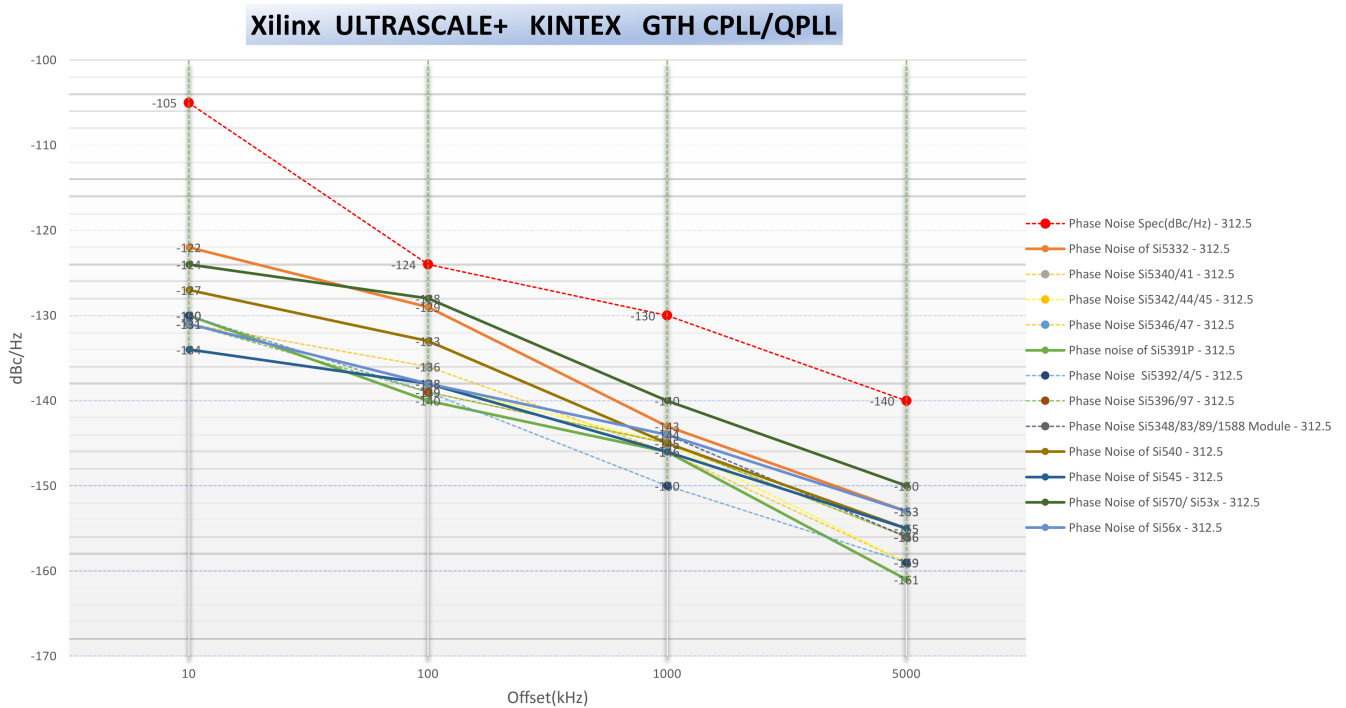
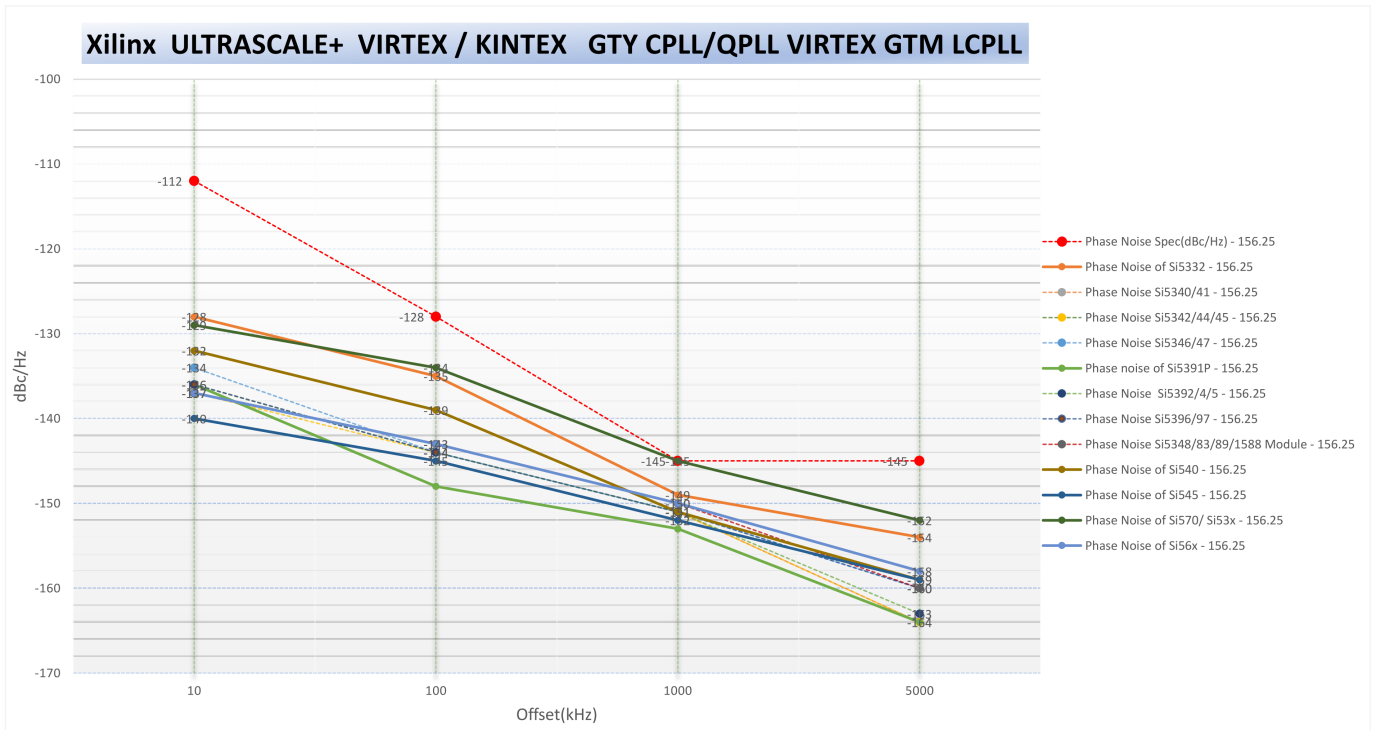
Table 1.2. Xilinx FPGA Specifications vs Skyworks XOs and VCXOs

Xilinx FPGA				XO			VCXO
				Si540	Si545	Si570/ Si53x	Si56x
Xilinx ULTRASCALE+ VIRTEX / KINTEX GTY CPLL/QPLL VIRTEX GTM LCPLL				Skyworks			
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-112	-132	-140	-129	-137
		100	-128	-139	-145	-134	-143
		1000	-145	-151	-152	-145	-150
		5000	-145 / CPLL only	-159	-159	-152	-158
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-103	-127	-134	N/A	-131
		100	-123	-133	-138	N/A	-138
		1000	-143	-145	-146	N/A	-144
		5000	-145 / CPLL only	-155	-155	N/A	-153
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-98	-121	-128	N/A	N/A
		100	-117	-127	-132	N/A	N/A
		1000	-140	-140	-140	N/A	N/A
		5000	-144 / CPLL only	-154	-154	N/A	N/A
Xilinx ULTRASCALE+ KINTEX GTH CPLL/QPLL				Skyworks			
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-105	-127	-134	-124	-131
		100	-124	-133	-138	-128	-138
		1000	-130	-145	-146	-140	-144
		5000	-140 / CPLL only	-155	-155	-150	-153
Xilinx ULTRASCALE VIRTEX/ KINTEX GTH QPLL/ CPLL				Skyworks			
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-105	-127	-134	-124	-131
		100	-124	-133	-138	-128	-138
		1000	-130	-145	-146	-140	-144
		50000	-140 / CPLL only	-158	-157	-154	-156
Xilinx ULTRASCALE VIRTEX GTY CPLL/QPLL				Skyworks			
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-112	-132	-140	-129	-137
		100	-128	-139	-145	-134	-143
		1000	-145	-151	-152	-145	-150
		50000	-145 / CPLL only	-160	-160	-156	-160

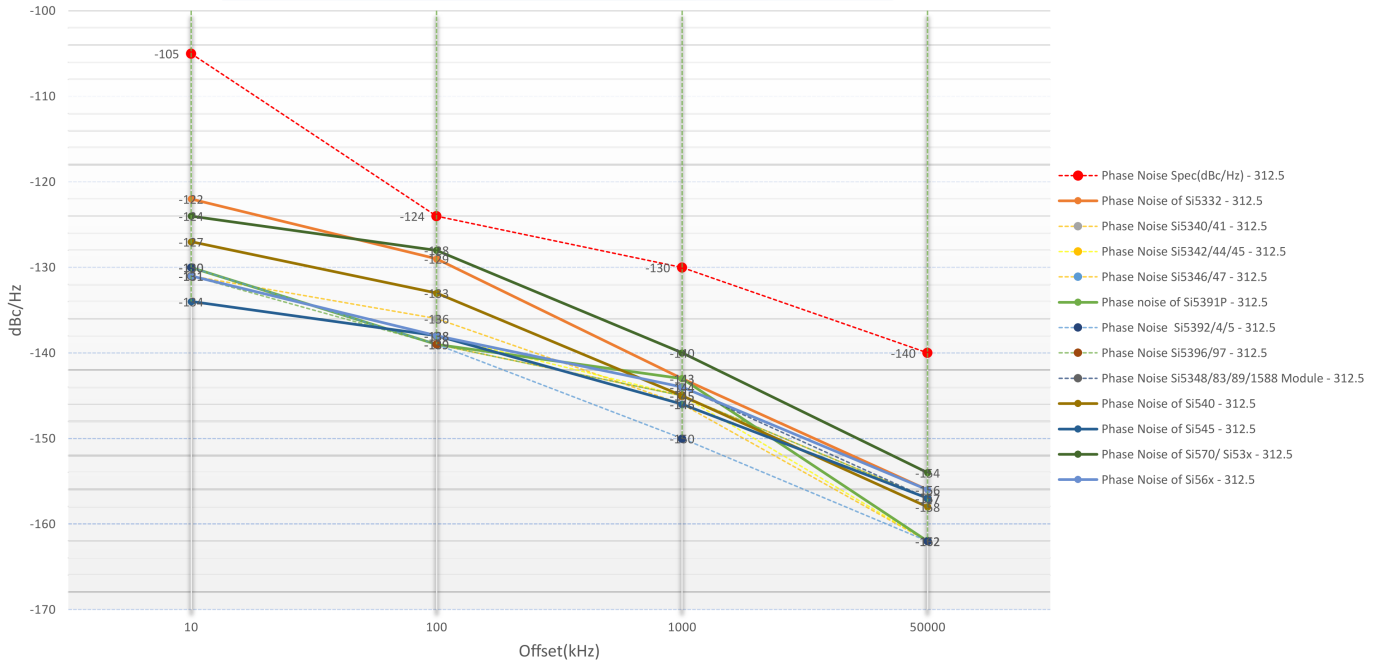
Xilinx FPGA				XO			VCXO
				Si540	Si545	Si570/ Si53x	Si56x
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-103	-127	-134	N/A	-131
		100	-123	-133	-138	N/A	-138
		1000	-143	-145	-146	N/A	-144
		50000	-145 / CPLL only	-158	-157	N/A	-156
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-98	-121	-128	-117	N/A
		100	-117	-127	-132	-122	N/A
		1000	-140	-140	-140	-134	N/A
		50000	-144 / CPLL only	-154	-154	-151	N/A
Xilinx Series 7 GTX/GTH QPLL				Skyworks			
Ref Clock Frequency 100 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-126	-137	-144	-133	-141
		100	-130	-143	-148	-138	-148
		1000	-134	-154	-155	-148	-153
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-123	-134	-141	-125	-140
		100	-129	-141	-146	-136	-146
		1000	-133	-152	-153	-146	-152
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-122	-132	-140	-129	-137
		100	-127	-139	-145	-134	-143
		1000	-132	-151	-152	-145	-150
Ref Clock Frequency 250 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-119	-128	-136	-124	-133
		100	-126	-134	-140	-129	-140
		1000	-131	-147	-148	-141	-146
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-115	-127	-134	-124	-131
		100	-124	-133	-138	-128	-138
		1000	-130	-146	-145	-140	-144
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-110	-121	-128	-117	-126
		100	-116	-127	-132	-122	-132
		1000	-120	-139	-140	-134	-139
Xilinx Series 7 GTX/GTH/GTP CPLL				Skyworks			
Ref Clock Frequency 100 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-126	-137	-144	-133	-141
		100	-132	-143	-148	-138	-148
		1000	-136	-154	-155	-148	-153
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-123	-134	-141	-125	-140
		100	-131	-141	-146	-136	-146
		1000	-135	-152	-153	-146	-152

Xilinx FPGA				XO			VCXO
				Si540	Si545	Si570/ Si53x	Si56x
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-121	-132	-140	-129	-137
		100	-129	-139	-145	-134	-143
		1000	-133	-151	-152	-145	-150
Ref Clock Frequency 250 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-119	-128	-136	-124	-133
		100	-126	-134	-140	-129	-140
		1000	-132	-147	-148	-141	-146
Ref Clock Frequency 312.5 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-116	-127	-134	-124	-131
		100	-124	-133	-138	-128	-138
		1000	-131	-145	-146	-140	-144
Ref Clock Frequency 625 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-110	-121	-128	-117	-126
		100	-119	-127	-132	-122	-132
		1000	-127	-139	-140	-134	-139
Xilinx Spartan 6				Skyworks			
Ref Clock Frequency 100 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-112	-137	-144	-133	-141
		100	-130	-143	-148	-138	-148
		1000	-130	-154	-155	-148	-153
		10000	-135	-159	-159	-155	-159
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-120	-134	-141	-125	-140
		100	-130	-141	-146	-136	-146
		1000	-130	-152	-153	-146	-152
		10000	-135	-160	-159	-152	-159
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-120	-132	-140	-129	-137
		100	-130	-139	-145	-134	-143
		1000	-130	-151	-152	-145	-150
		10000	-135	-160	-160	-155	-160

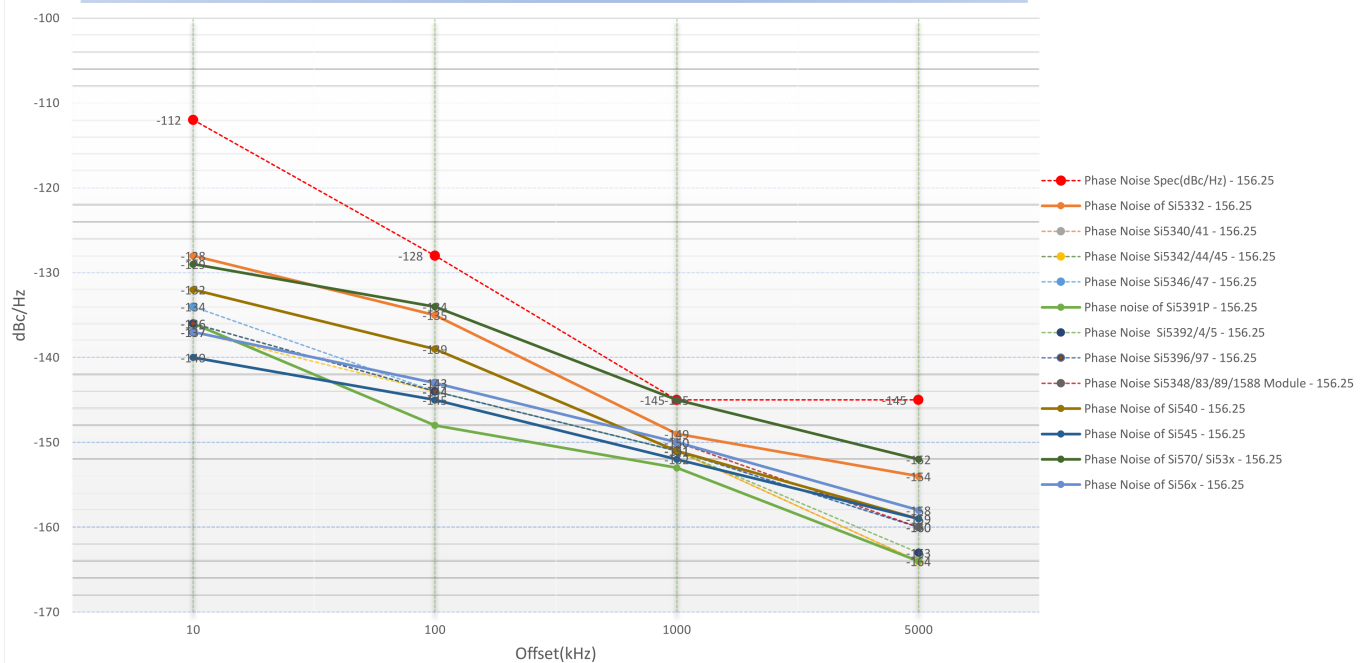
The following graphs show a visual representation of the Xilinx phase noise requirement mask (in red) and the measured data that is contained in the tables.



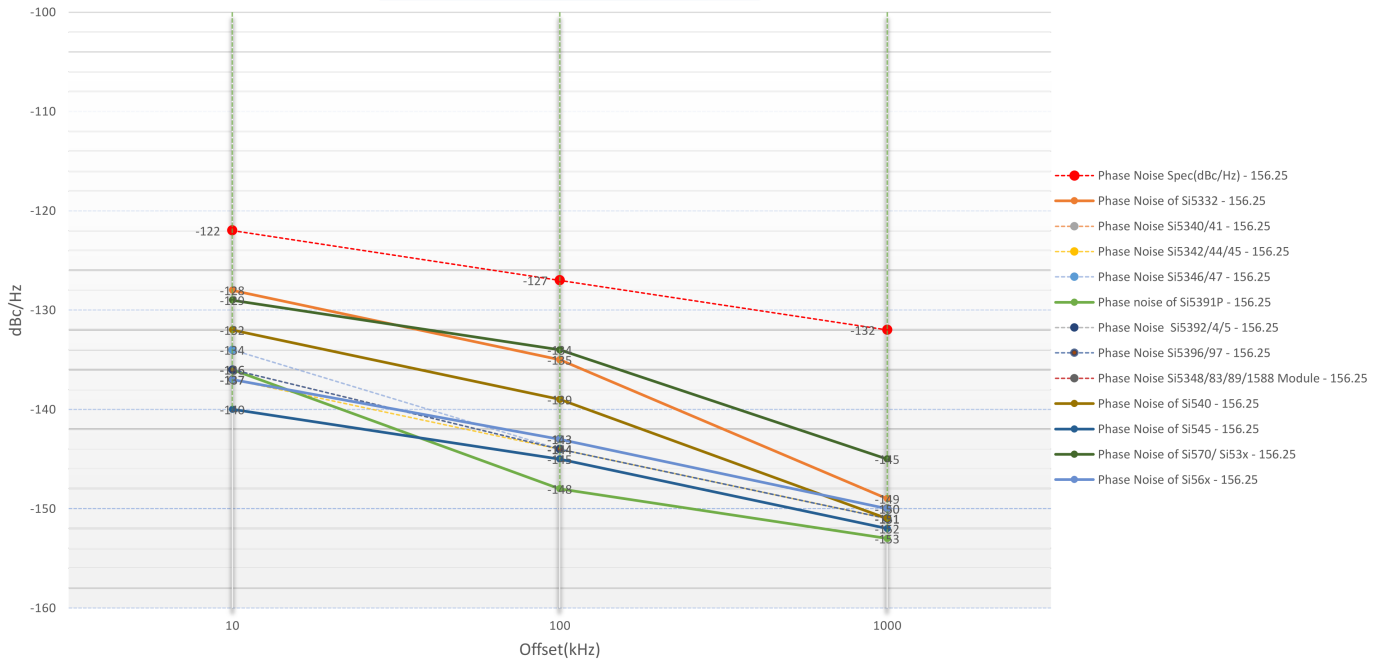
Xilinx ULTRASCALE VIRTEX/ KINTEX GTH QPLL/ CPLL



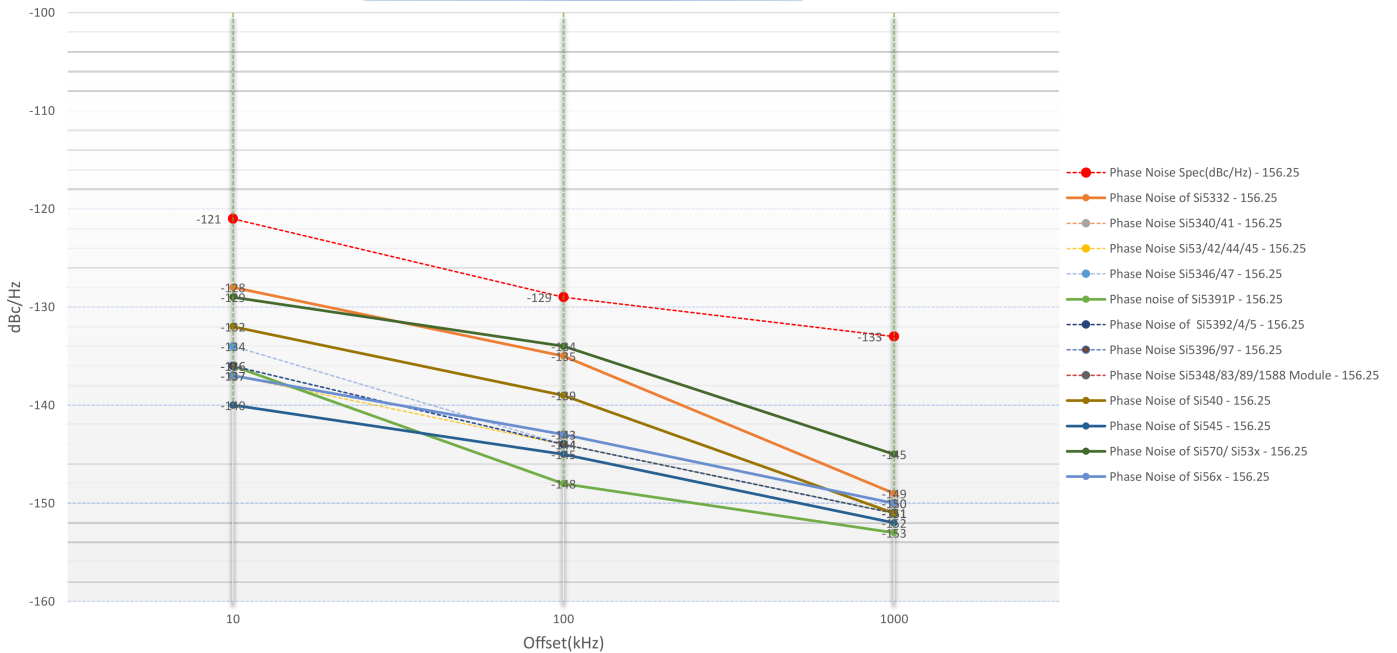
Xilinx ULTRASCALE+ VIRTEX / KINTEX GTY CPLL/QPLL VIRTEX GTM LCPLL



Xilinx Series 7 GTX/GTH QPLL



Xilinx Series 7 GTX/GTH/GTP CPLL



Xilinx Spartan 6

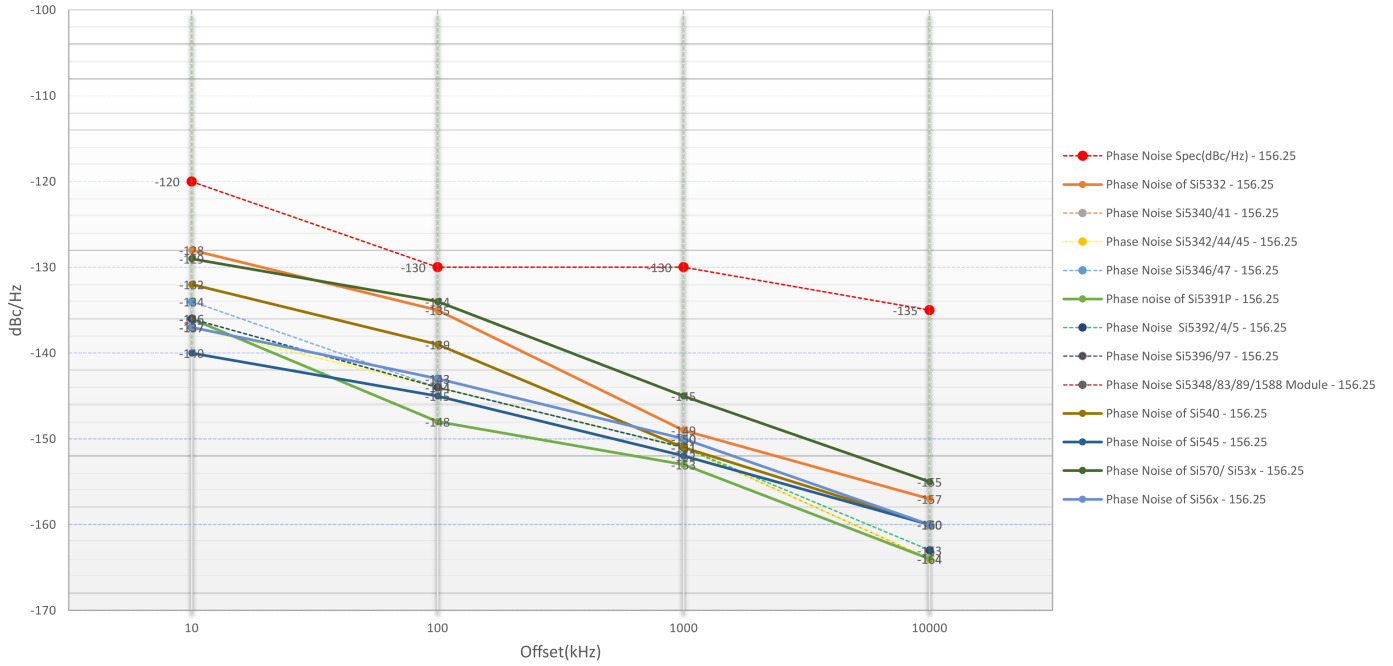


Table 1.3. Intel FPGA Specifications vs Skyworks Clock Generators, Jitter Attenuators & Network Synchronizers

Intel FPGA				Clock Generator				Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)
				Si5332	Si5335 Si5338	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module
Stratix 10 GX/SX				Skyworks								
Ref Clock Frequency 800 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.1	-70	N/A	N/A	-82	-74	-75	-75	-74	N/A	N/A
		1	-90	N/A	N/A	-106	-106	-101	-101	-105	N/A	N/A
		10	-100	N/A	N/A	-121	-121	-122	-122	-121	N/A	N/A
		100	-110	N/A	N/A	-130	-130	-130	-130	-130	N/A	N/A
		>=1000	-120	N/A	N/A	-136	-136	-137	-137	-135	N/A	N/A
Agilex , Stratix 10 (TX/MX)				Skyworks								
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-130	N/A	N/A	-136	-137	-136	-135	-136	-136	-136
		100	-138	N/A	N/A	-144	-148	-144	-144	-144	-144	-143
		500	-138	N/A	N/A	-149	-150	-149	-149	-149	-149	-148
		3000	-140	N/A	N/A	-157	-160	-159	-158	-160	-158	-158
		10000	-144	N/A	N/A	-164	-165	-164	-158	-164	-160	-160
		20000	-146	N/A	N/A	-164	-165	-164	-158	-164	-160	-160
Intel Arria V (GX/SX/GT/ST)				Skyworks								
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.01	-50	-87	-74	-66	-69	-70	-75	-78	-77	-69
		0.1	-80	-102	-105	-97	-96	-88	-90	-91	-93	-92
		1	-110	-119	-119	-123	-122	-114	-118	-120	-122	-122
		10	-120	-130	-126	-138	-138	-138	-137	-137	-137	-137
		100	-120	-137	-130	-146	-148	-144	-146	-146	-146	-145
		>=1000	-130	-150	-130	-153	-154	-151	-152	-152	-152	-151
Intel Arria V GZ				Skyworks								
Ref Clock Frequency 622 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.1	-70	N/A	-90	-84	-84	-77	-78	-78	-77	-77
		1	-90	N/A	-104	-109	-108	-105	-108	-106	-109	-108
		10	-100	N/A	-112	-124	-125	-125	-124	-124	-124	-124
		100	-110	N/A	-116	-133	-134	-133	-133	-133	-133	-133
		>=1000	-120	N/A	-120	-140	-140	-138	-139	-139	-139	-138
Arria 10 GX/SX/GT , Cyclone 10 GX				Skyworks								

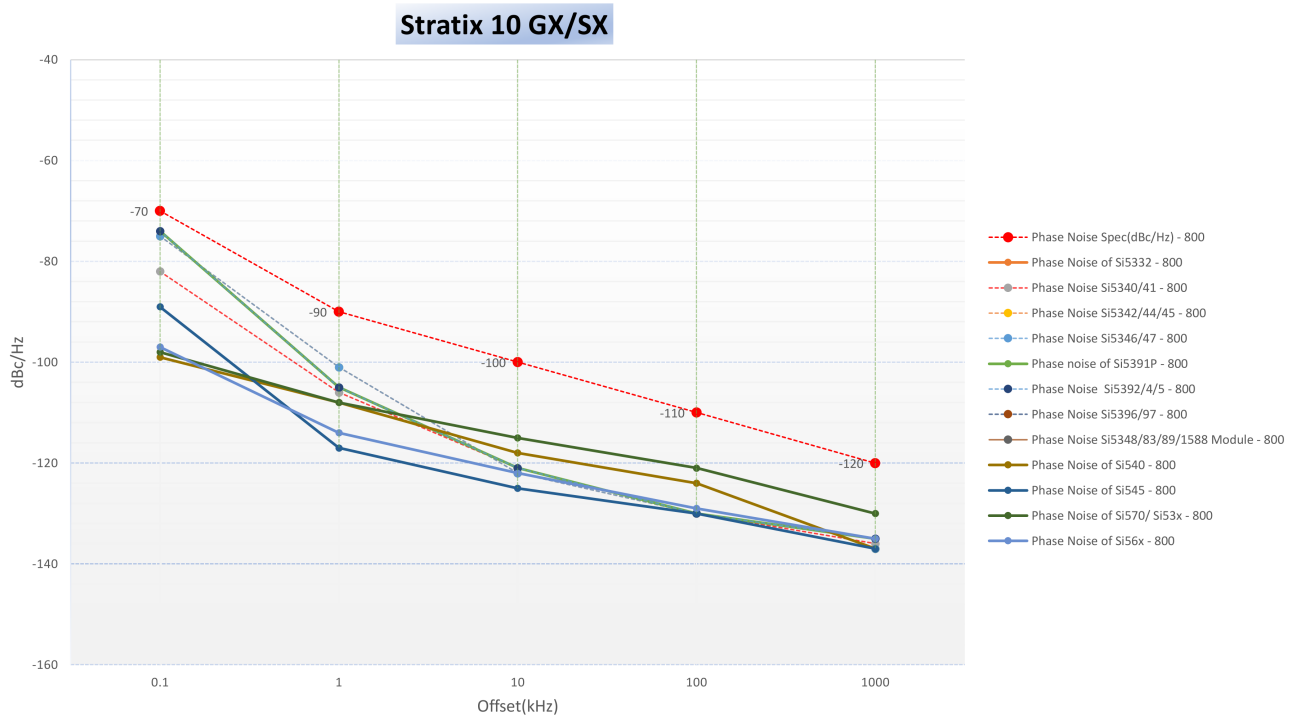
Intel FPGA				Clock Generator				Jitter Attenuating Clock				Network Synchronizer (SyncE/1588)
				Si5332	Si5335 Si5338	Si5340 Si5341	Si5391P	Si5342 Si5344 Si5345	Si5346 Si5347	Si5392 Si5394 Si5395	Si5396 Si5397	Si5348 Si5383 Si5389 M88 IEEE 1588 module
Ref Clock Frequency 622 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.1	-70	N/A	-90	-84	-84	-77	-78	-78	-77	-77
		1	-90	N/A	-104	-109	-108	-105	-108	-106	-109	-108
		10	-100	N/A	-112	-124	-125	-125	-124	-124	-124	-124
		100	-110	N/A	-116	-133	-134	-133	-133	-133	-133	-133
		>=1000	-120	N/A	-120	-140	-140	-138	-139	-139	-139	-139

Table 1.4. Intel FPGA Specifications vs Skyworks XOs and VCXOs

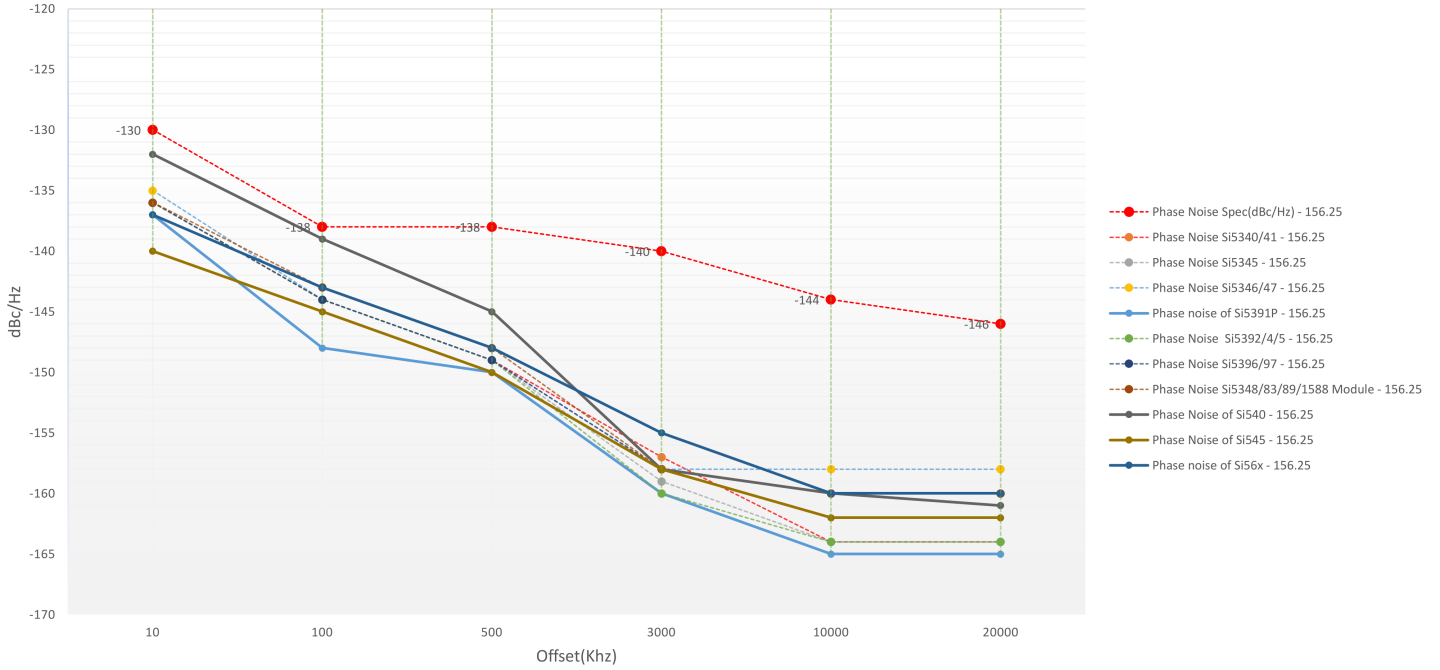
Intel FPGA				XO			VCXO
				Si540	Si545	Si570/ Si53x	Si56x
Stratix 10 GX/SX				Skyworks			
Ref Clock Frequency 800 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.1	-70	-99	-89	-98	-97
		1	-90	-108	-117	-108	-114
		10	-100	-118	-125	-115	-122
		100	-110	-124	-130	-121	-129
		>=1000	-120	-137	-137	-130	-135
Agilex , Stratix 10 (TX/MX)				Skyworks			
Ref Clock Frequency 156.25 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	10	-130	-132	-140	-129	-137
		100	-138	-139	-145	-134	-143
		500	-138	-145	-150	-140	-148
		3000	-140	-158	-158	-152	-155
		10000	-144	-160	-162	-155	-160
		20000	-146	-161	-162	-156	-160
Intel Arria V (GX/SX/GT/ST)				Skyworks			
Ref Clock Frequency 125 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.01	-50	-67	-62	-67	-79
		0.1	-80	-114	-108	-114	-113
		1	-110	-125	-131	-125	-133
		10	-120	-134	-141	-133	-140
		100	-120	-141	-146	-136	-146
		>=1000	-130	-152	-153	-146	-152

Intel FPGA				XO			VCXO
				Si540	Si545	Si570/ Si53x	Si56x
Intel Arria V GZ				Skyworks			
Ref Clock Frequency 622 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.1	-70	-101	-92	-101	-101
		1	-90	-111	-119	-108	-118
		10	-100	-121	-127	-117	-126
		100	-110	-127	-132	-122	-132
		>=1000	-120	-139	-140	-134	-138
Arria 10 GX/SX/GT, Cyclone 10 GX				Skyworks			
Ref Clock Frequency 622 (MHz)	Frequency Offset (kHz) Phase noise dBc/Hz	0.1	-70	-101	-92	-101	-101
		1	-90	-111	-119	-108	-118
		10	-100	-121	-127	-117	-126
		100	-110	-127	-132	-122	-132
		>=1000	-120	-139	-140	-134	-138

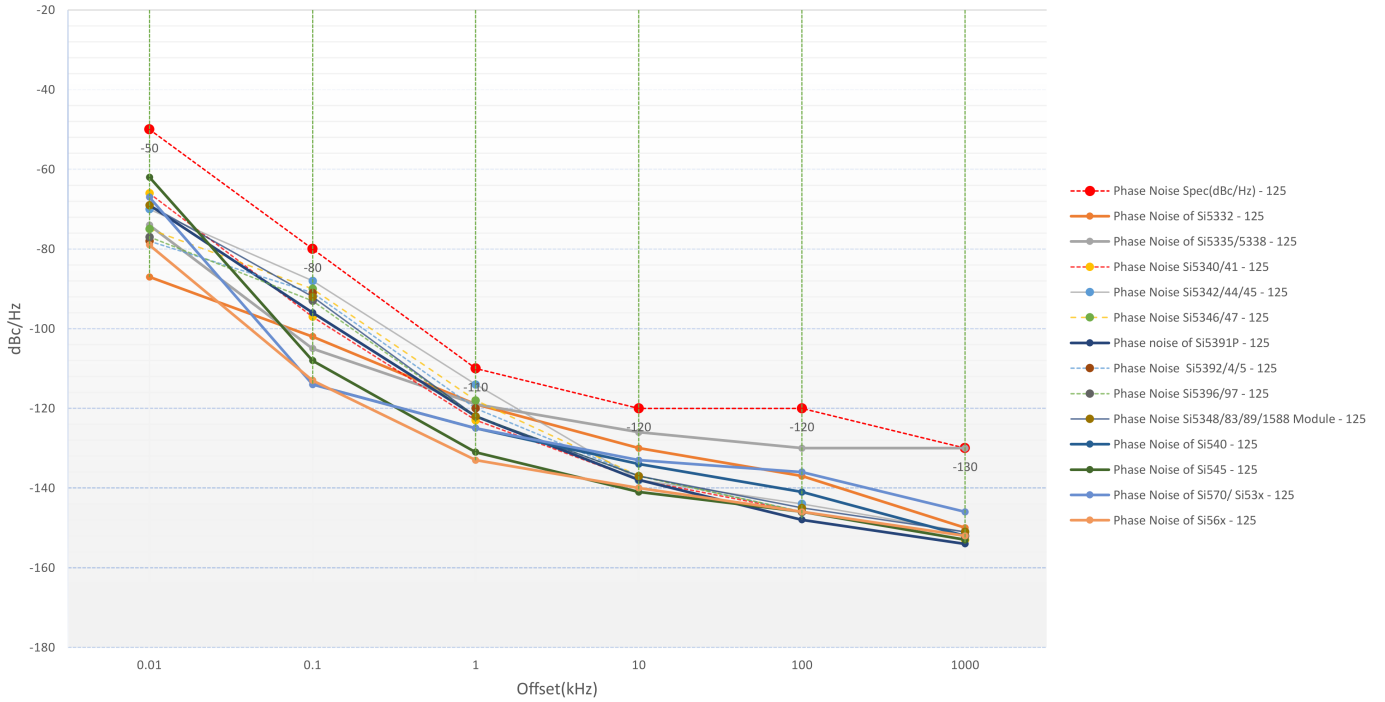
The following graphs show a visual representation of the Intel phase noise requirement mask (in red) and the measured data that is contained in the tables.



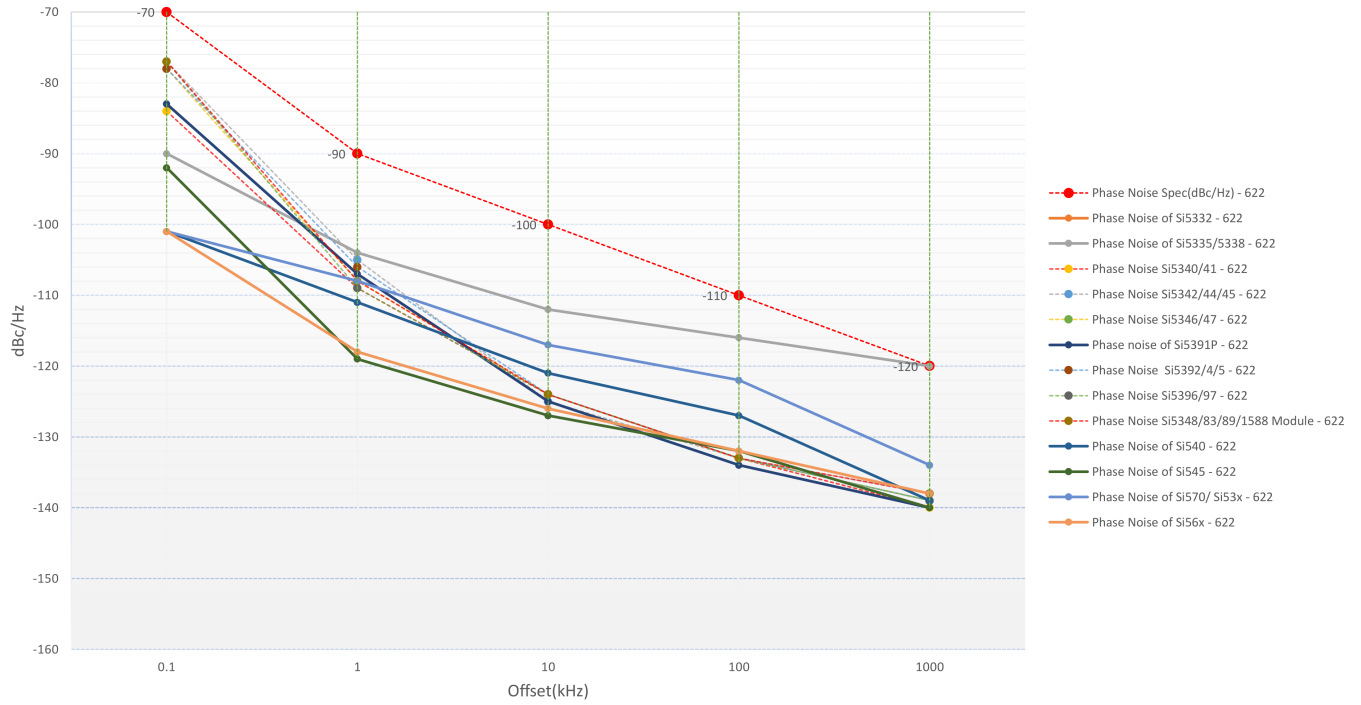
Agilex , Stratix 10 (TX/MX)



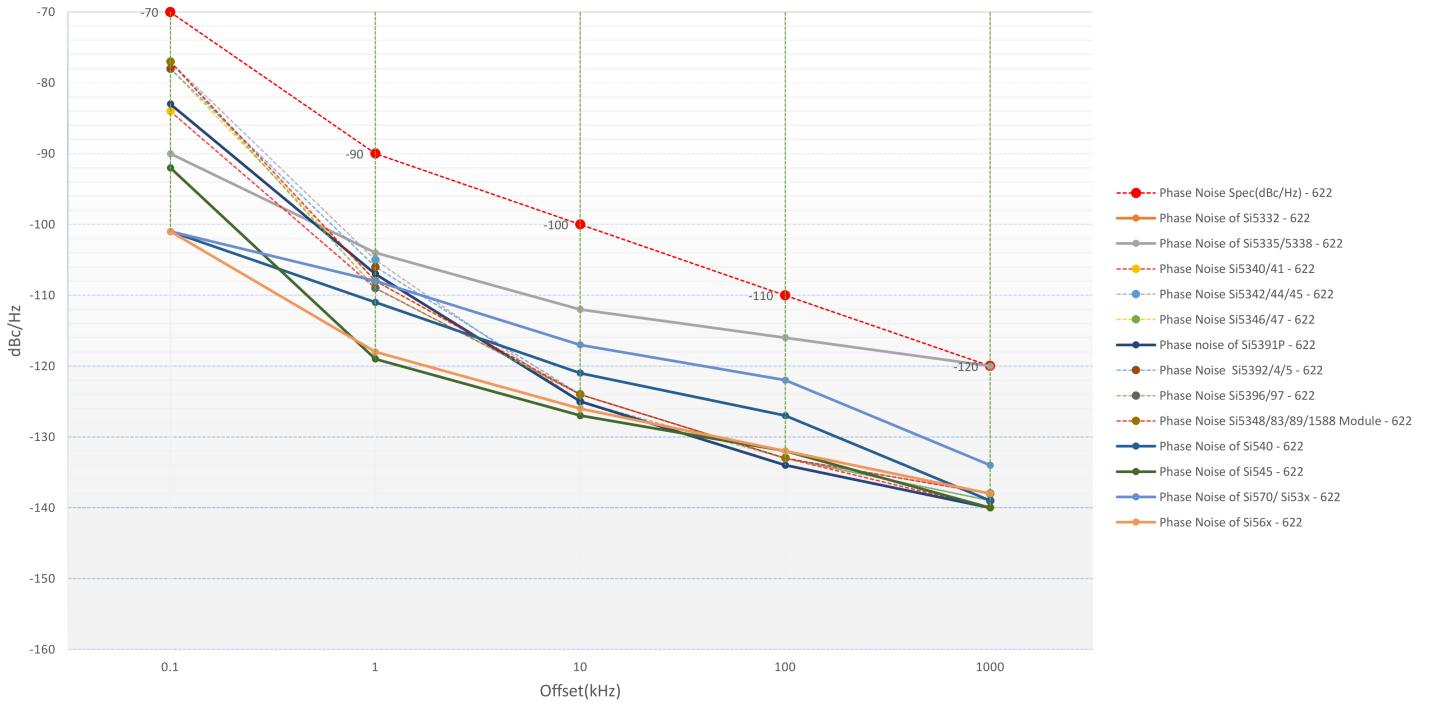
Intel Arria V (GX/SX/GT/ST)



Intel Arria V GZ



Arria 10 GX/SX/GT , Cyclone 10 GX



2. Recommendations

Skyworks timing devices are well suited for use as reference clock sources for FPGAs with embedded SerDes in high-speed serial digital communications applications. With additional built-in features such as any-frequency programmability with 0 ppm frequency error, superior PSRR, and jitter attenuation with digitally-programmable loop bandwidth, Skyworks timing products provide real system benefits over simple PLL clock solutions.

This application note provides an overview of the reference clock requirements for FPGA SerDes, which in most designs is the most stringent in terms of phase noise and/or RMS phase jitter requirements. But in addition to that, most designs will need additional reference clocks for endpoints other than the FPGA transceiver, and Skyworks has many clocking solutions including Si5332/Si5338 clock generators, Si51x/Si59x/Si540/545 XOs, Si53x/Si570 any frequency programmable XOs, Si55x/56x VCXOs, and finally the Si5330x Universal Buffers that can consolidate all of those reference clocks together, many of which are used for these exact purposes on the FPGA reference designs.



SKYWORKS®

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro



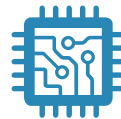
Portfolio

www.skyworksinc.com/ia/timing



SW/HW

www.skyworksinc.com/CBPro



Quality

www.skyworksinc.com/quality



Support & Resources

www.skyworksinc.com/support

Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, Clockbuilder®, DSPLL®, ISOModem®, ProSLIC®, and SiPHY® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.