



## VCXO TUNING SLOPE (Kv), STABILITY, AND ABSOLUTE PULL RANGE (APR)

### 1. Introduction

VCXO devices are typically used in phase lock loop (PLL) circuits to generate an output clock signal that is phase locked to a reference clock signal. One of the key design parameters for a PLL circuit is the range over which it can track variations in the reference clock frequency. The PLL tracking range is dictated by the "absolute pull range" (APR) of the VCXO. The APR is a function of the VCXO's total frequency stability and the VCXO's pullability, or "pull range." The VCXO pullability, in turn, is a function of the VCXO's "tuning slope" (Kv). This application note discusses the relationship between the tuning slope (Kv), the pullability, the frequency stability, and the APR specifications for VCXO devices. It is important to understand the relationship between these specifications in order to effectively compare competing VCXO devices or to properly specify a VCXO for a particular application.

### 2. VCXO Tuning Slope (Kv)

A voltage controlled crystal oscillator (VCXO) is a crystal oscillator whose output frequency can be adjusted by varying the voltage applied to a  $V_{CONTROL}$  input pin.

The "tuning slope", or voltage-to-frequency gain, of the VCXO specifies the amount of frequency change that results from a given change in the control voltage. A frequency vs. control voltage curve that is representative of a traditional VCXO device is depicted in Figure 1.

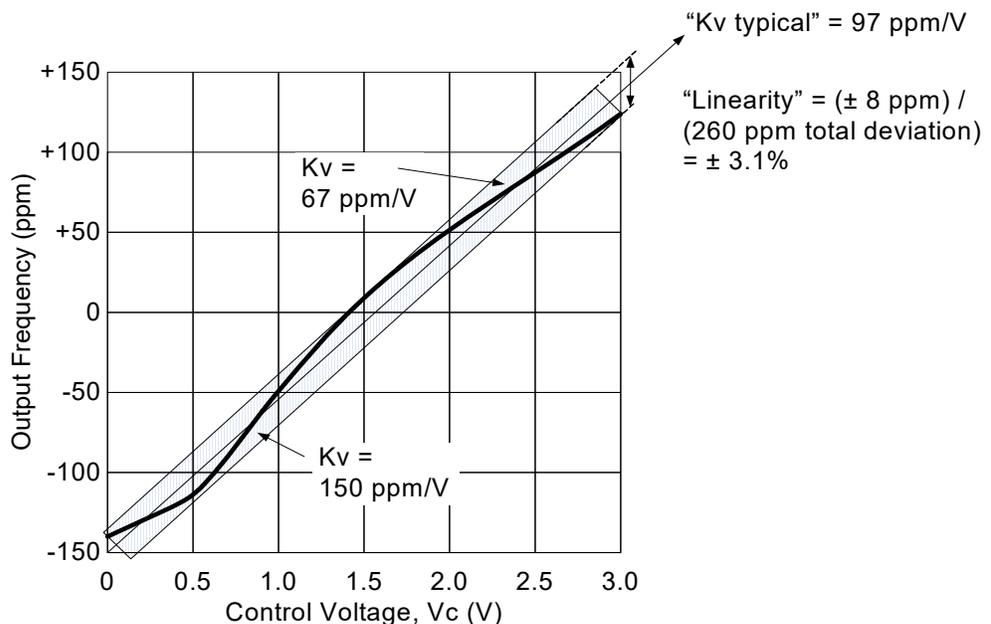


Figure 1. Traditional VCXO Output Frequency vs. Control Voltage Plot

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The slope of this curve is equal to the voltage-to-frequency gain of the VCXO and is often referred to as the “tuning slope” of the VCXO. The VCXO tuning slope is often represented by the symbol "Kv" and is typically expressed in units of ppm/V. VCXO data sheets generally give only a typical value for Kv. Data sheets may also give a “Linearity” specification associated with the tuning slope. Linearity is calculated by first finding a best straight line (BSL) fit to the frequency vs. voltage curve, and then measuring the maximum deviation of the curve to the BSL. This measured deviation is expressed as a percentage of the total frequency deviation of the curve. For example, in Figure 1, the maximum deviation of the frequency vs. voltage curve from the BSL is about  $\pm 8$  ppm, and the total deviation of the curve is roughly 260 ppm; so, the linearity is about 3.1%. Note, however, that linearity is not necessarily a good indicator of how well the actual gain at a specific operating point (sometimes referred to as the “incremental gain”) matches the specified Kv typical value. Traditional VCXO devices use a varactor diode to vary the capacitive loading on the crystal resonator as a function of the applied control voltage. Changing the capacitive loading on the crystal changes, or “pulls”, the frequency at which the crystal resonates. The resulting relationship between control voltage and frequency is not linear, and the incremental Kv for traditional VCXO devices can vary significantly from the average value, as illustrated in Figure 1.

It should be noted that Skyworks Solutions' Si55x series VCXO devices do not depend on "pulling" of the crystal resonator for frequency variation, and the frequency vs. control voltage curves for these devices show much less deviation in incremental Kv than traditional VCXO devices. This is important in PLL applications, because the PLL loop bandwidth and jitter peaking characteristics are directly affected by the incremental Kv of the VCXO.

### 3. VCXO Pullability Requirements in PLL circuits

VCXOs are typically used in phase-locked loop (PLL) circuits to produce an output clock that is phase locked to the PLL's reference clock. A simplified block diagram for a PLL circuit is given in Figure 2.

The phase-frequency detector (PFD) block generates an output current or voltage signal that is proportional to the difference in phase and/or frequency between the reference clock and the VCXO output clock. The PFD output signal is smoothed by the low-pass filter to create the slowly-varying control voltage,  $V_C$ , that is applied to the VCXO  $V_{CONTROL}$  pin in order to shift the output frequency as needed to maintain a "locked" phase/frequency relationship between the output and the reference. A divider is included in the feedback loop between the VCXO output and the PFD input in applications where the PLL output frequency is a multiple of the reference clock input frequency.

For example, a PLL in a SONET/SDH optical networking application might have an output frequency of 622.08 MHz and a reference clock frequency of 19.44 MHz. This PLL would have a divide-by-32 block in the feedback path. Under ideal conditions, with an

input reference clock at exactly 19.44 MHz, the PLL would be locked, with an output frequency of 622.08 MHz. If operating at ambient temperature, we would expect the control voltage at the VCXO  $V_{CONTROL}$  pin to be at its mid-range value (this might be 1.65 V for a VCXO with 3.3 V supply). Now, if the reference clock drifted up in frequency by 20 ppm, the PFD output would increase, causing the control voltage,  $V_C$ , to increase up to the point where the VCXO output frequency had also increased by 20 ppm. Alternatively, if the reference remained at exactly 19.44 MHz but the temperature began rising above ambient, the resonant frequency of the crystal resonator in the VCXO would increase, causing the VCXO output frequency to rise (with no change in control voltage). The PFD would respond to this change by decreasing its output, which would, in turn, decrease the control voltage so as to maintain the output frequency at 622.08 MHz.

It can be seen intuitively from this example that in order for the PLL to remain locked, the VCXO must provide a sufficiently wide frequency adjustment range to accommodate any variation in the reference clock frequency as well as any drift of the VCXO's own center frequency over normal operating conditions.

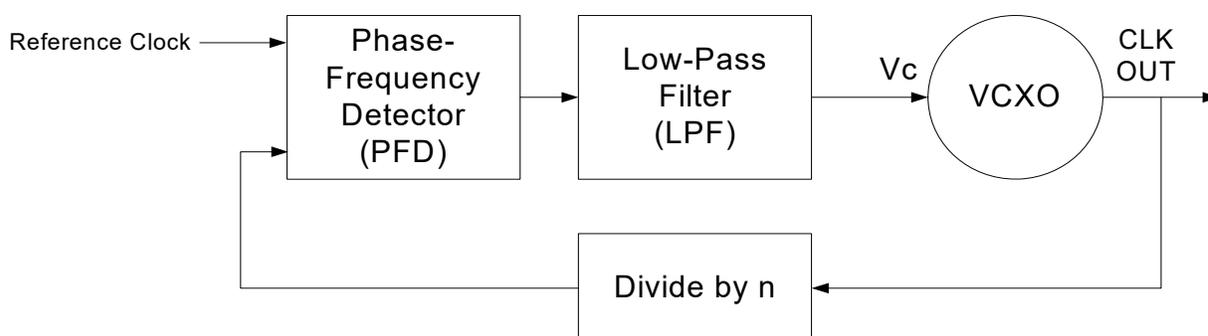


Figure 2. Simplified PLL Block Diagram

## 4. VCXO Pullability

The Pullability, or Pull Range, of a VCXO specifies the total amount of frequency variation that can be achieved by varying the voltage on the  $V_{\text{CONTROL}}$  pin. The pullability may or may not be specified on the data sheet. If not, it can be estimated by observing the frequency vs. control voltage curve (if provided) or by multiplying the tuning slope (Kv) by the control voltage range as follows:

Pullability  $\approx$  Kv x ( $V_{\text{CONTROL}}$  voltage range)

For example, a 3.3 V VCXO will often specify an operating control voltage range of 0.3 V to 3.0 V. Looking at Figure 1, it can be seen that varying the control voltage from 0.3 V to 3.0 V results in an output frequency change from about -125 ppm to about +125 ppm; so, the device that corresponds to this curve would have a total pull range of 250 ppm or  $\pm 125$  ppm. Alternatively, the pullability could be estimated by multiplying the typical tuning slope (97 ppm/V) by the control voltage range (2.7 V). This yields a pull range estimate of  $97 \text{ ppm/V} \times 2.7 \text{ V} = 262 \text{ ppm}$ , or  $\pm 131 \text{ ppm}$ . As noted in the previous paragraph, the pullability of the VCXO must be large enough to accommodate both the drift of the VCXO's center frequency over all operating conditions (i.e., the "total frequency stability" of the VCXO), as well as the worst case frequency variation of the PLL reference clock (the PLL "tracking range").

## 5. Total Frequency Stability

The "Total Frequency Stability" for a VCXO specifies the maximum amount that the VCXO's center frequency can drift from its nominal value over all operating conditions, with the voltage applied to the  $V_{\text{CONTROL}}$  pin held constant at its nominal value. A total stability specification would typically include an allowance for the initial frequency accuracy of the oscillator plus allowances for frequency drift due to temperature variation, aging, supply variation, load variation, reflow soldering, and shock and vibration. The initial frequency accuracy for a VCXO is typically in the  $\pm 10$  ppm range, and temperature stability typically ranges from  $\pm 10$  ppm to  $\pm 100$  ppm. Aging typically ranges from  $\pm 1$  to  $\pm 5$  ppm/year and is generally highest in the first year of operation. Supply variation, load variation, reflow soldering, and shock/vibration are less significant factors, typically in the 0.1 ppm range, and these stability factors are often omitted from VCXO data sheets. VCXO data sheets may or may not provide a total frequency stability specification. In cases where total frequency is not specified, the sum of the initial accuracy, the frequency stability, and the aging specifications can be used as an estimate of total stability.

## 6. Absolute Pull Range (APR)

One of the key parameters for PLL design is the range of reference clock frequency variation that the PLL is required to track. This PLL reference "tracking range" is essentially a function of the VCXO pullability and the VCXO total frequency stability. The difference between the VCXO's total pull range and the total frequency stability indicates how much of the pull range is available for tracking of the PLL reference clock, after allowing for the frequency stability of the VCXO over all operating conditions. This "tracking range" is often referred to as the "Absolute Pull Range" (APR) of the VCXO, and the APR is specified on some manufacturer's data sheets. In cases where APR is not specified directly, it can be estimated by subtracting the VCXO's total stability from the total pull range as follows:

$$\text{APR} = (\text{Total Pull Range}) - (\text{Total Stability})$$

For example, consider an Si550 VCXO device with the following options:

Supply voltage: 3.3 V

Temperature stability:  $\pm 100$  ppm

Tuning slope (Kv): 90 ppm/V

The Si550 has an initial accuracy specification of  $\pm 1.5$  ppm, and an aging specification of  $\pm 10$  ppm total for 15 years. The total stability can therefore be estimated to be:

$$\text{Total Stability} = (\pm 1.5 \text{ ppm initial}) + (\pm 100 \text{ ppm temp}) + (\pm 10 \text{ ppm aging}) = \pm 111.5 \text{ ppm}$$

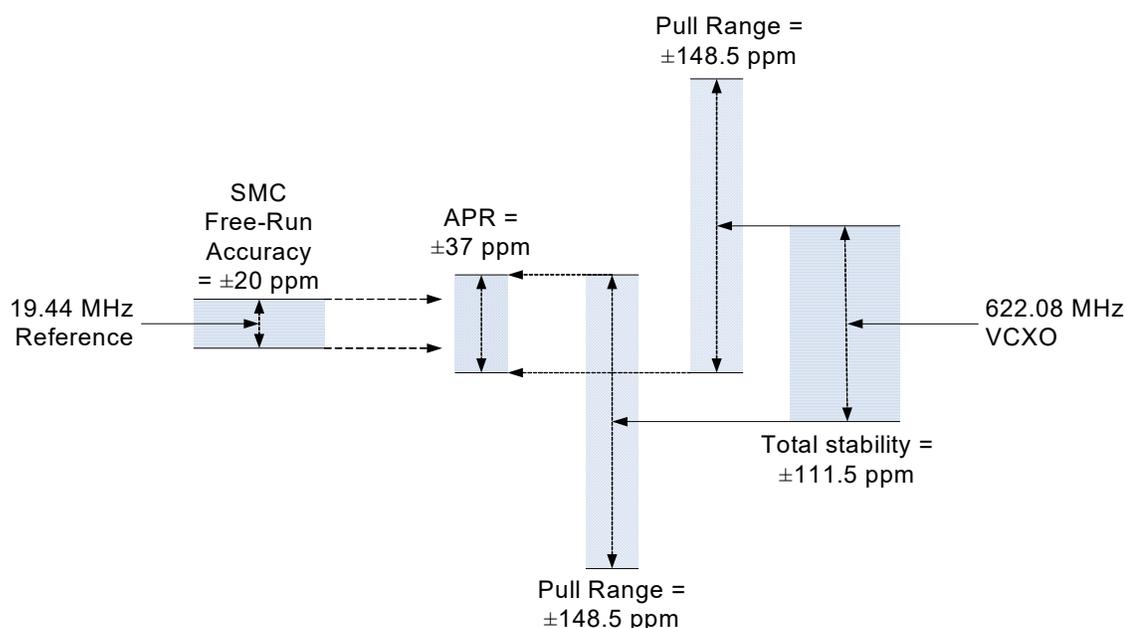
The specified control voltage range for the Si550 is 0 V to  $V_{DD}$  (3.3 V total), and the tuning slope in this case is 90 ppm/V; so, the pull range is calculated to be:

$$\text{Total Pull Range} = 3.3 \text{ V} \times 90 \text{ ppm/V} = \pm 0.5 \times 3.3 \text{ V} \times 90 \text{ ppm/V} = \pm 148.5 \text{ ppm}$$

The APR for the Si550 with these selected options is then calculated to be:

$$\text{APR} = (\pm 148.5 \text{ ppm}) - (\pm 111.5 \text{ ppm}) = \pm 37 \text{ ppm}$$

This APR example is shown graphically in Figure 3, using typical SONET frequencies for the VCXO and for the reference clock. This graphic is laid out with the reference clock on the left and the VCXO frequency on the right, corresponding with the PLL block diagram of Figure 2. However, this graphic is best examined from right to left, as follows:



**Figure 3. APR Graphic Representation**

The VCXO has a specified nominal center frequency of 622.08 MHz and a total frequency stability of  $\pm 111.5$  ppm. This means that over the 15 year life of this application, and under any operating conditions, the VCXO center frequency (with  $V_{\text{CONTROL}} = V_{\text{DD}}/2$ ) may drift as high as 622.08 MHz + 111.5 ppm, or as low as 622.08 MHz – 111.5 ppm. The pull range of the VCXO is 148.5 ppm. Therefore, if the VCXO center frequency does ever drift to the maximum possible value, the PLL will still be able to pull the output frequency down to as low as  $(622.08 \text{ MHz} + 111.5 \text{ ppm}) - 148.5 \text{ ppm} = 622.08 \text{ MHz} - 37 \text{ ppm}$ . Similarly, if the VCXO center frequency reaches its minimum value of 622.08 MHz – 111.5 ppm, the PLL will still be able to pull the output frequency up to 622.08 MHz + 37 ppm. Thus, the PLL will be able to track variations in the reference clock of up to  $\pm 37$  ppm under any operating conditions for at least 15 years. Since this tracking range, or APR, exceeds the expected reference variance of  $\pm 20$  ppm by a reasonable design margin, this looks like a good solution for this SONET application.

## 7. Kv and Noise Sensitivity

The minimum APR required for a PLL design depends on the nature of the application. For example, in telecommunications systems, the maximum frequency deviation expected from a free-running SONET Minimum Clock (SMC) reference timing signal is  $\pm 20$  ppm. VCXOs used for PLLs in SONET systems must have an APR of at least  $\pm 20$  ppm, and APR specifications of  $\pm 30$  to  $\pm 50$  ppm are common for these telecommunications applications. In data communications applications, such as 10 Gigabit Ethernet, Gigabit Ethernet, and FibreChannel transport, APR specifications in the  $\pm 100$  ppm range would be more common.

The minimum tuning slope (Kv) required for a VCXO to achieve a given APR depends on the total frequency stability of the VCXO. A device with poorer frequency stability must have a higher Kv in order to achieve the same APR as a device with better stability. For example, a VCXO device with typical frequency stability may need a tuning slope of 50 to 100 ppm/V in order to provide an APR in the  $\pm 50$  ppm range. Voltage-Controlled SAW Oscillators (VCSOs) typically have poorer initial accuracy and poorer temperature stability characteristics than VCXOs and may need Kv values in the 200 to 400 ppm/V range to achieve the same  $\pm 50$  ppm APR.

Noise sensitivity in a PLL design can be minimized by selecting a VCXO with the lowest Kv that still provides the APR required for the application. This is because conducted or radiated noise that is coupled into the  $V_{\text{CONTROL}}$  pin of the VCXO will be converted into output jitter with a voltage-to-frequency gain equal to Kv. The PLL designer should be careful not to overlook this factor when selecting a VCXO device. VCXO data sheets typically give specifications for intrinsic jitter and/or phase noise under ideal operating conditions (no noise on the supply or  $V_{\text{CONTROL}}$  pins). However, it is impossible to design a system with no conducted and radiated noise. In practice, selection of a device with very low intrinsic jitter specifications but large Kv may result in higher overall system jitter than a device with slightly higher intrinsic jitter but smaller Kv, if there is a moderate amount of noise in the system.

**NOTES:**



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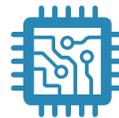
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