
JITTER ATTENUATION—CHOOSING THE RIGHT PHASE-LOCKED LOOP BANDWIDTH

1. Introduction

Clock signals provide reference timing to every integrated circuit and electrical system. While consumer applications typically use simple quartz crystals for reference clock generation, other applications have much more sophisticated timing requirements and often require a combination of clocks to provide synchronization, generation and distribution. In applications like wireless infrastructure and medical imaging, which require high fidelity analog to digital signal conversion, next-generation designs require higher resolution and faster data transmission rates. Next-generation, high-performance networking and communications applications require faster transmission rates and higher speed data processing. In these applications, clock signals play a vital role in the overall architecture. If not designed properly, the system-level performance of these applications can be limited by the performance of the underlying timing solution. Special care must be taken during the device selection and hardware design process to ensure that the clocking design maximizes system performance.

2. Phase Noise and Jitter

The quality of a clock signal is heavily dependent on its phase noise and jitter. An ideal clock source would generate a pure sine wave. All signal power would be generated at one frequency. However, in actuality, all clock signals have some degree of phase-modulated noise. This noise spreads the power of the clock signal to adjacent frequencies, resulting in noise sidebands. The phase noise is typically expressed in dBc/Hz and represents the amount of signal power at a given sideband or offset frequency from the ideal clock frequency. Radio frequency (RF) and analog-to-digital data conversion (ADC) applications require very low phase noise clocks. In RF applications, increased phase noise can create channel-to-channel interference, degrading RF signal quality. In ADC applications, increased phase noise can limit the signal-to-noise ratio (SNR) and equivalent number of bits (ENOB) of the data converter.

Phase noise is the frequency domain representation of clock noise. Phase jitter, on the other hand, is the time domain instability of the clock signal and is typically expressed in picoseconds (ps). Jitter can be described as the random variation in the actual clock signal's edges versus its ideal waveform. Phase jitter is the figure of merit in high-speed digital applications including data communications, networking and high-definition video transmission. These applications require multi-gigabit data transmission rates as high as 40 Gbps. Physical-layer transceivers used in networking and HD video rely on low jitter reference clocks that are internally multiplied within the transceiver to clock the high-speed data transmitted from the device. Excessive jitter can lead to higher bit-error rates that may exceed system-level requirements.

3. PLL Bandwidth Optimization

Managing phase noise and jitter in these high-performance applications is a necessity. Often, a jitter attenuating clock IC or discrete phase-locked loop (PLL) is used to produce low jitter clocks. A traditional PLL architecture is comprised of a phase frequency detector (PFD), loop filter (LF) and voltage-controlled oscillator (VCO) as shown in Figure 1. Often the PLL filter is implemented using discrete components. One of the more challenging elements in designing with high-performance PLLs is how to choose the "right" loop bandwidth for a given application. As with many engineering challenges, this is a tradeoff decision that has to be made at the application level.

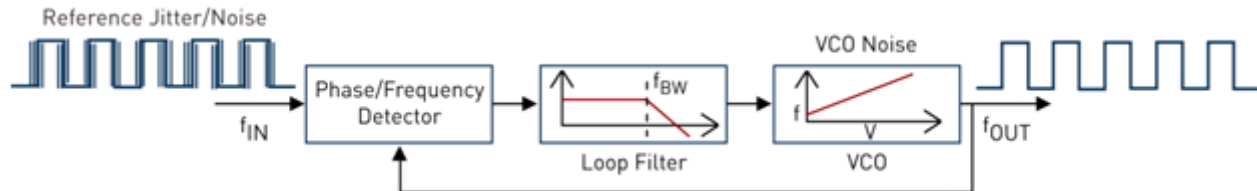


Figure 1. PLL Output Jitter Sources

As shown in Figure 1, PLL output jitter is dominated by two sources: transferred reference noise and internal VCO noise. Reference noise sources include jitter generated by the reference timing source, PCB noise coupling and power supply noise. VCO noise sources include loop filter components, VCO amplifier components and power supply noise.

A jitter attenuating PLL can be used to filter noise from the input clock and produce a low jitter output clock. Reducing the loop filter bandwidth increases the amount of jitter attenuation on the reference clock, transferring less jitter from the input to the output. If the reference clock has a significant amount of jitter, using a low PLL bandwidth to filter this noise is typically recommended. However, it is not always advantageous to use a very low PLL bandwidth. The chief reason for this is that the relative contribution of VCO noise to a PLL's output jitter *increases* as the loop bandwidth *decreases*. Unless the PLL has a very low noise VCO, the impact of using a low PLL bandwidth can have the detrimental effect of actually *increasing* the output clock jitter. Therein lies the tradeoff decision. The PLL bandwidth needs to be set to minimize both VCO and reference jitter. Since the reference clock jitter can vary from application to application, this is a decision that needs to be made independently on each design. This is shown in Figure 2.

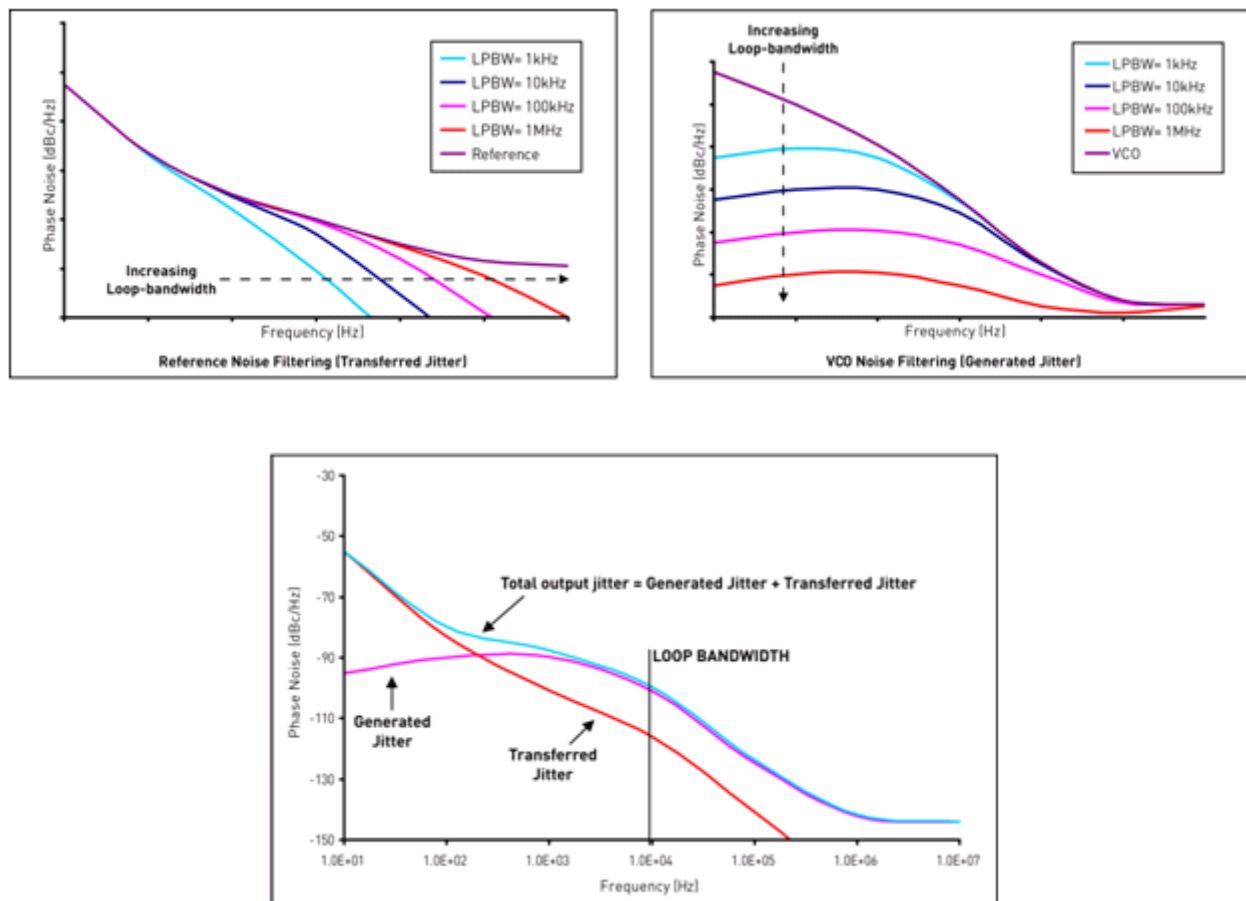


Figure 2. Balancing Jitter Transfer and Jitter Generation to Optimize PLL Jitter Performance

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A discrete PLL built using a high-quality voltage-controlled crystal oscillator (VCXO) may be used in this situation; however, the design is still sensitive to power supply switching noise, PCB noise coupling and noise introduced by the discrete loop filter components. Another option is to use a clock IC with an internal VCO, but these devices typically require external loop filter components that are sensitive to external noise sources. The interface between a PLL's loop filter and its VCO is one of the most noise-sensitive nodes in a PLL design. Noise that enters a PLL through its external loop filter components will be present on the VCO's input and will be multiplied by the VCO's gain factor, increasing the VCO noise and subsequently, the PLL noise in the design.

Solutions using discrete loop filters also increase PLL design and layout complexity. PLL stability needs to be calculated for each unique frequency plan + loop bandwidth combination to ensure there is sufficient phase margin in the design. Special PCB layout techniques such as employing guard rings around the loop filter components to provide isolation and minimize leakage current are used in some high-performance PLL designs. Since most traditional high-performance clock ICs require multiple, isolated power planes, the loop filter layout considerations add further complexity to the PCB design.

4. Using the Si5317 for In-Circuit Jitter Optimization

A better approach is shown in Figure 3. The Si5317 is a low-cost, high-performance jitter attenuating clock based on Skyworks Solutions' proven 3rd generation DSPLL technology. The device can accept a noisy reference clock at any frequency from 1 to 710 MHz and provide two ultra-low jitter (0.3 ps rms, 12 kHz to 20 MHz) output clocks at the same frequency. The device operating frequency is set using control pins, such that no microprocessor intervention is required. In addition, the device includes a fully integrated, digitally-controlled loop filter. Through simple pin control, hardware designers can pick the optimum loop filter value from up to 8 settings ranging from 60 Hz to 8.4 kHz, making it very easy to manage the tradeoff between transferred jitter and generated jitter and hence optimize jitter performance at the application level. This low cost, pin-controlled device can be added to any clock path and digitally tuned to produce the lowest possible output jitter, simplifying design in jitter sensitive applications.

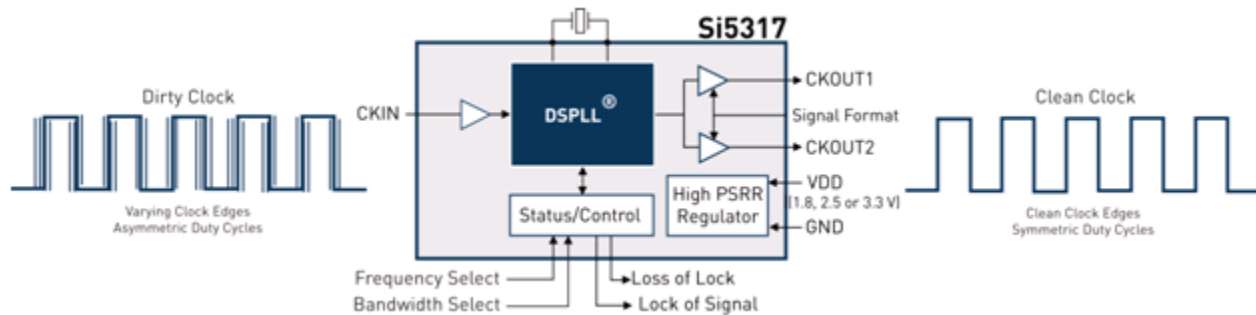


Figure 3. Si5317 Jitter Cleaning Clock

NOTES:



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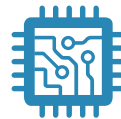
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