PCI Express 3.1 Jitter Requirements

1. Introduction

PCI Express (PCIe) is a serial point-to-point interconnect standard developed by the Peripheral Component Interconnect Special Interest Group (PCI-SIG). Although originally targeted at desktop personal computers, PCIe has been broadly adopted in many applications including blade servers, storage, embedded computing and communication networks because of its widespread use, low cost, and high data throughput. A key difference between PCIe and earlier buses (e.g., PCI/PCI-X) is PCIe is based on point-to-point serial links rather than a shared parallel bus architecture. Serial transmission was chosen over traditional parallel transmission because it eliminates the problems associated with timing skew across multiple wires and variable transmission distances. Serial transmission sends both the clock and data on the same wire allowing for scalable transmission rates and reduced complexity and cost. A typical PCIe serial architecture is illustrated in Figure 1.

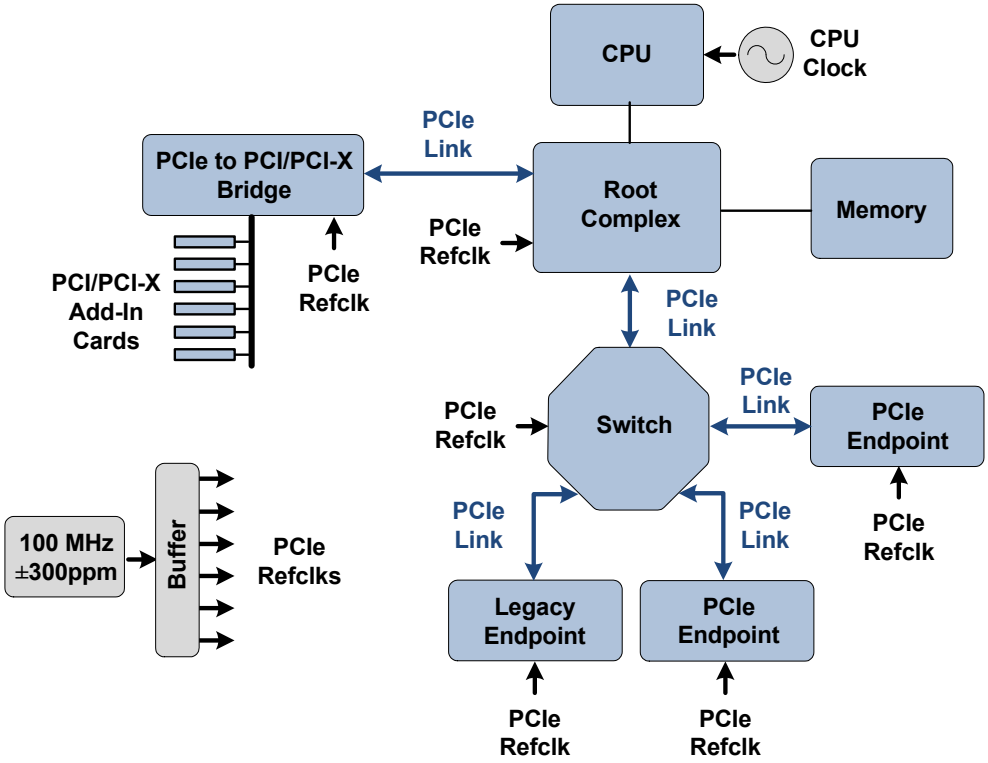
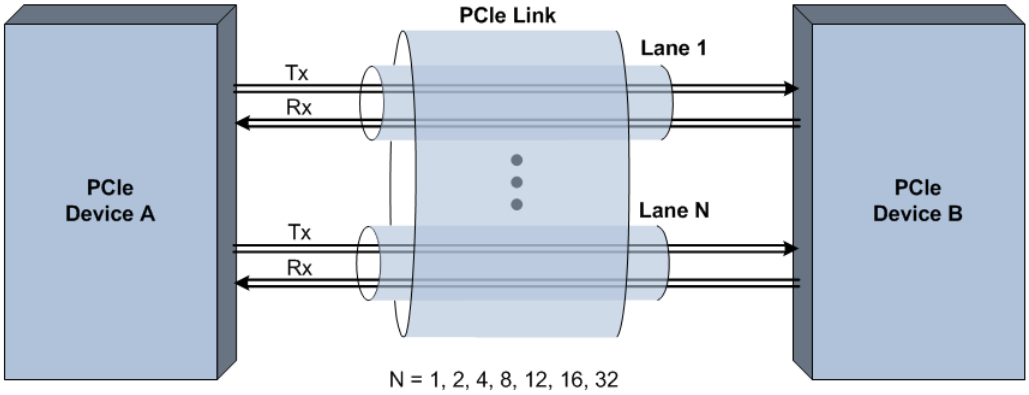


Figure 1. PCIe Architecture Components

The root complex provides a central control point in the PCIe tree topology. It manages connectivity for a PCIe port, a CPU and associated memory, and other bridging functions. A switch connects multiples endpoints to the root complex. Endpoints are peripheral I/O devices that communicate to the CPU through the switch and/or the root complex. PCIe reference clocks (Refclk) provide a stable timing reference for the serial data transmission between two PCIe devices.

2. PCI Express Link

A PCIe link is made up of one or more lanes which consists of a transmit and receive differential pair. Support for x1, x2, x4, x8, x12, x16, x32 lanes per link enables a scalable bandwidth to meet the needs of a wide variety of applications. With the introduction of PCIe 1.0 in 2003, a lane rate of 2.5 Gbps was defined, which resulted in a data throughput of 500 MBps per lane using 8B/10B encoding (2.5 Gbps ÷ 10 bits/Byte x 2 directions). In 2007, PCIe 2.0 doubled the data throughput by increasing the lane rate to 5.0 Gbps. PCIe 3.0 released in 2010 once again doubled the data throughput by increasing the lane rate to 8 Gbps and changing to a more efficient scrambling and encoding scheme (128B/130B). Figure 2 illustrates the flexible data throughput of the PCIe link for the three PCIe standards.



	Number of Lanes per PCIe Link						
	x1	x2	**x4**	**x8**	x12	**x16**	x32
PCIe 1.1	500 MBps	1 GBps	2 GBps	4 GBps	6 GBps	8 GBps	16 GBps
PCIe 2.1	1 GBps	2 GBps	4 GBps	8 GBps	12 GBps	16 GBps	32 GBps
PCIe 3.1	2 GBps	4 GBps	8 GBps	16 GBps	24 GBps	32 GBps	64 GBps

Total Data Throughput per PCIe Link

Figure 2. PCIe Link and Effective Data Throughput

3. Refclk and Clocking Architectures

An external clock reference clock (Refclk) is required for transmitting data between two PCIe devices. A Refclk frequency of 100 MHz ±300 ppm is specified for all three line rates (2.5 Gbps, 5.0 Gbps, 8.0 Gbps). The burden has been placed on the TX PLL to multiply the 100 MHz Refclk frequency to the desired data rate. Although the Refclk frequency has remained the same, the jitter performance requirements of the Refclk have improved to support the higher data rates prevalent with PCI Express 2.1 and 3.1. We will look at the Refclk jitter requirements in the following sections.

The PCIe standards allow for some flexibility in how Refclk is distributed to the PCIe devices in a system. The three supported clocking architectures are illustrated in Figure 3. The *Common Clock RX Architecture* is the simplest and most widely used form of clock distribution between PCIe devices. In this architecture the same 100 MHz Refclk source is distributed to both the transmitting and receiving PCIe device. In the *Data Clocked RX Architecture*, the receiving device does not require a Refclk. Instead it recovers the clock embedded in the transmitted datastream. The *Separate Clocking Architecture* uses different clocks for the transmitting and receiving devices. This is possible because the standard allows up to 600 ppm of frequency separation between the transmitter and receiver.

Among the deciding factors in selecting the best clocking architecture are system partitioning and Refclk jitter performance requirements. We will explore these factors in the following sections.

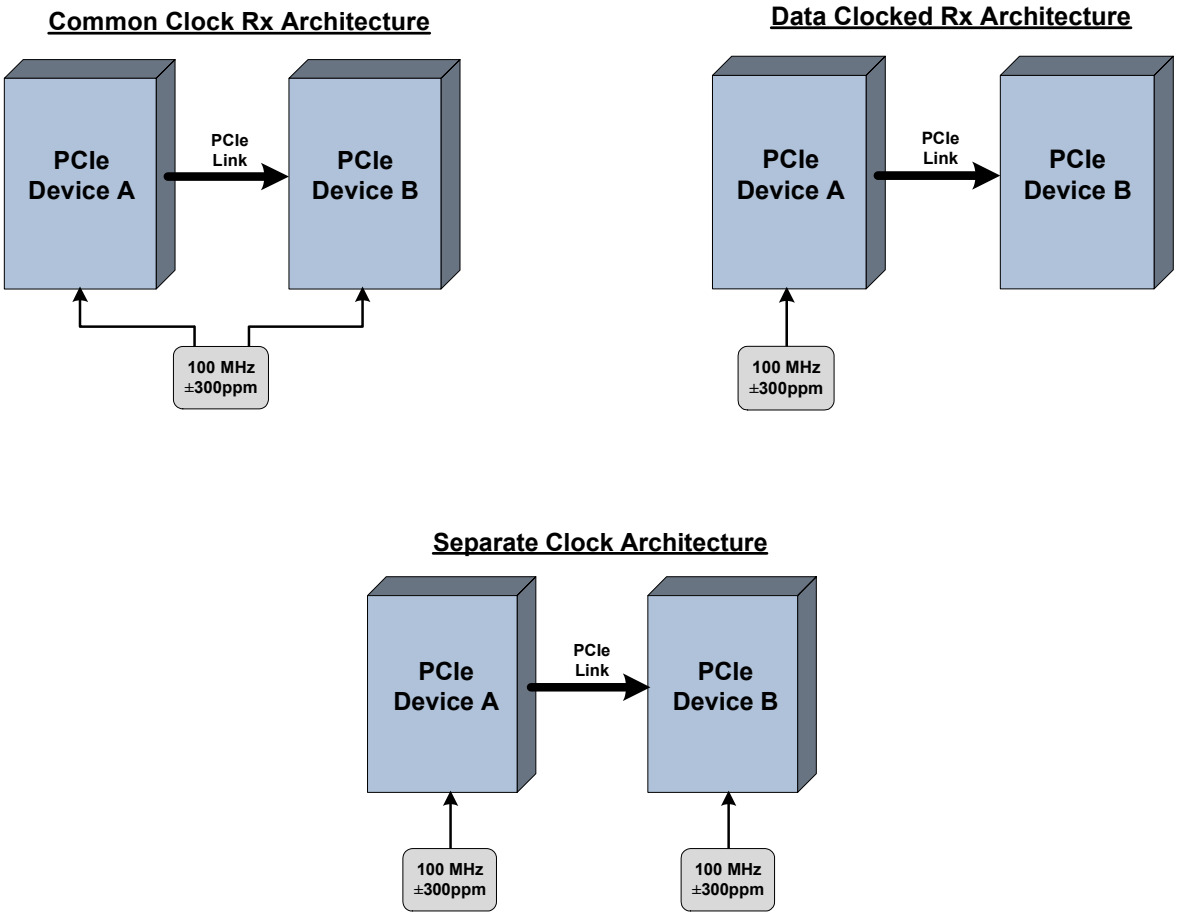


Figure 3. PCIe Clock Architectures

4. Refclk Jitter Requirements

Jitter of the reference clock has a direct impact on the efficiency of the data transfer between two PCIe devices. The data recovery process is able to track a portion of the jitter frequencies that are within its bandwidth, but it is the jitter frequencies that it cannot track that must be limited. This untrackable jitter spectrum is easily defined using a series of transfer functions that represent the loop bandwidths of the PLLs and the Clock Data Recovery (CDR) that affect the data recovery process. The PCIe standards defines the overall transfer function, parameters (bandwidth and peaking), and jitter limits for each of the three clocking architectures.

4.1. Filtering Applied to Refclk Measurements

PCI-Express specifications include and require multiple filtering operations to be performed on the Refclk data in order to obtain the jitter results at the CDR latch. The reason for this is because some of the jitter will be tracked by the TX and RX PLLs and some will be removed, so the final result at the CDR latch is the only jitter that will impact the performance of recovering data. In revision 3.1 of the PCI-Express base specification, five filtering operations are applied to the data: SSC Separation, 0.01 – 1.5 MHz step band pass filter (BPF), 1.5 MHz step High Pass Filter (HPF), edge filtering, and architecture specific PLL difference functions.

SSC Separation

Spread Spectrum Clocking (SSC) separation is intended to remove the energy associated with the spread spectrum in the low frequency range (0.01-1.5 MHz) in order to define separate low frequency Rj and Dj components.

0.01-1.5 MHz Step BPF

The intent of having a 0.01 MHz step on the low end of this band pass filter is to eliminate any 1/f noise in the clock data since that noise is 100% tracked by the CDR. This band also eliminates the high frequency jitter components 1.5 MHz and beyond that may not be tracked by the CDR. This range is where the low frequency Rj specification is defined.

1.5 MHz Step HPF

This filter completely removes the low frequency jitter components, taking into account the high frequency components that may or may not be tracked by the CDR. This jitter will be the dominant jitter seen by the CDR latch causing system performance degradation.

Edge Filtering

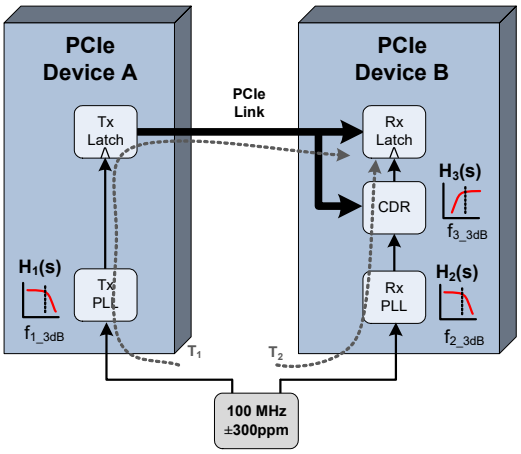
The data taken for the reference clock jitter measurements is typically done on real time oscilloscopes that will have noise due to the scopes' limitations from the finite sampling and voltage resolution aperture. A voltage averaging process should be applied at 5 GHz. This application can be done most accurately with a Fourier Transform filter, but can also be effectively achieved through a voltage averaging process if the FFT method is too computationally intensive. Most O-scopes allow you to change the effective bandwidth as well.

PLL Difference Function and Max PLL Band Width Function

The bulk of this application note pertains to the associated PLL difference and Max PLL BW functions for any given architecture. The intent of the jitter measurements for PCI-Express reference clocks is to determine what the jitter is that is seen by the data latch at the CDR. Clock jitter at this latch will directly impact how much margin the CDR has to the incoming degraded data stream. A typical PCI-Express system is the common clocked architecture that considers a TX and RX PLL as well as a CDR. All three of these have a characteristic transfer function associated with it that determines how much noise on the clock is either transmitted, tracked, or attenuated.

4.2. Jitter Requirements for the Common Refclk RX Architecture

Since the reference clock for the *Common Clock RX Architecture* is distributed to both the transmit and receive PCIe devices, its overall transfer function, H(s), becomes the difference between the transfer functions of the transmit path and receive paths. The transfer functions relevant to the PCIe 1.1, 2.1, and 3.1 standards for the Common Clock RX Architecture are shown in Figure 4.



	PLL and CDR Transfer Functions
Tx PLL	$H_1(s) = \frac{2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}{s^2 + 2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}$
Rx PLL	$H_2(s) = \frac{2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}{s^2 + 2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}$
CDR	$H_3(s) = \frac{s}{s + \omega_{n3}}$ $\omega_{n3} = 2 \cdot \pi \cdot f_{3\_3dB}$
Refclk Path Delay Difference: T = | T1 – T2 |	

	Overall Jitter Transfer Functions	Transfer Function Parameters Defined		
PCIe 1.1	$H(s) = \left(H_1(s) - H_2(s) \cdot e^{-s \cdot T}\right) \cdot H_3(s)$ where T = 10 ns max	f_{1_3dB} 22.0 MHz	3.0 dB Peaking $\omega_{n1} = 11.83 \cdot 2\pi$ Mrad/s $\zeta_1 = 0.54$	
		f_{2_3dB} 1.5 MHz	3.0 dB Peaking $\omega_{n2} = 0.807 \cdot 2\pi$ Mrad/s $\zeta_2 = 0.54$	
		f_{3_3dB} 1.5 MHz		
PCIe 2.1	$H(s) = \left(H_1(s) \cdot e^{-s \cdot T} - H_2(s)\right)$ where T = 12 ns max		1.0 dB Peaking	3.0 dB Peaking
		f_{1_3dB} 5.0 MHz	$\omega_{n1} = 1.82 \cdot 2\pi$ Mrad/s $\zeta_1 = 1.16$	
		f_{1_3dB} 8.0 MHz		$\omega_{n1} = 4.31 \cdot 2\pi$ Mrad/s $\zeta_1 = 0.54$
		f_{2_3dB} 16.0 MHz	3.0 dB Peaking $\omega_{n2} = 8.61 \cdot 2\pi$ Mrad/s $\zeta_2 = 0.54$	
PCIe 3.1	$H(s) = \left(H_1(s) \cdot e^{-s \cdot T} - H_2(s)\right) \cdot H_3(s)$ $H'(s) = \left(H_2(s) \cdot e^{-s \cdot T} - H_1(s)\right) \cdot H_3(s)$ where T = 12 ns max		0.01 dB Peaking	2.0 dB Peaking
		f_{1_3dB} 2.0 MHz	$\omega_{n1} = 0.448$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 6.02$ Mrad/s $\zeta_1 = 0.73$
		f_{1_3dB} 4.0 MHz	$\omega_{n1} = 0.896$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 12.04$ Mrad/s $\zeta_1 = 0.73$
			0.01 dB Peaking	1.0 dB Peaking
		f_{2_3dB} 2.0 MHz	$\omega_{n2} = 0.448$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 4.62$ Mrad/s $\zeta_2 = 1.15$
		f_{2_3dB} 5.0 MHz	$\omega_{n2} = 1.12$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 11.53$ Mrad/s $\zeta_2 = 1.15$
		f_{3_3dB} 10.0 MHz	64 Combinations	

Figure 4. Jitter Transfer Functions For The Common Clocked RX Architecture

Using PCIe 1.1 as an example, the overall transfer function H(s) becomes a bandpass filter as shown in Figure 5. The area under the curve becomes the untracked jitter that needs to be limited to ensure efficient data transmission.

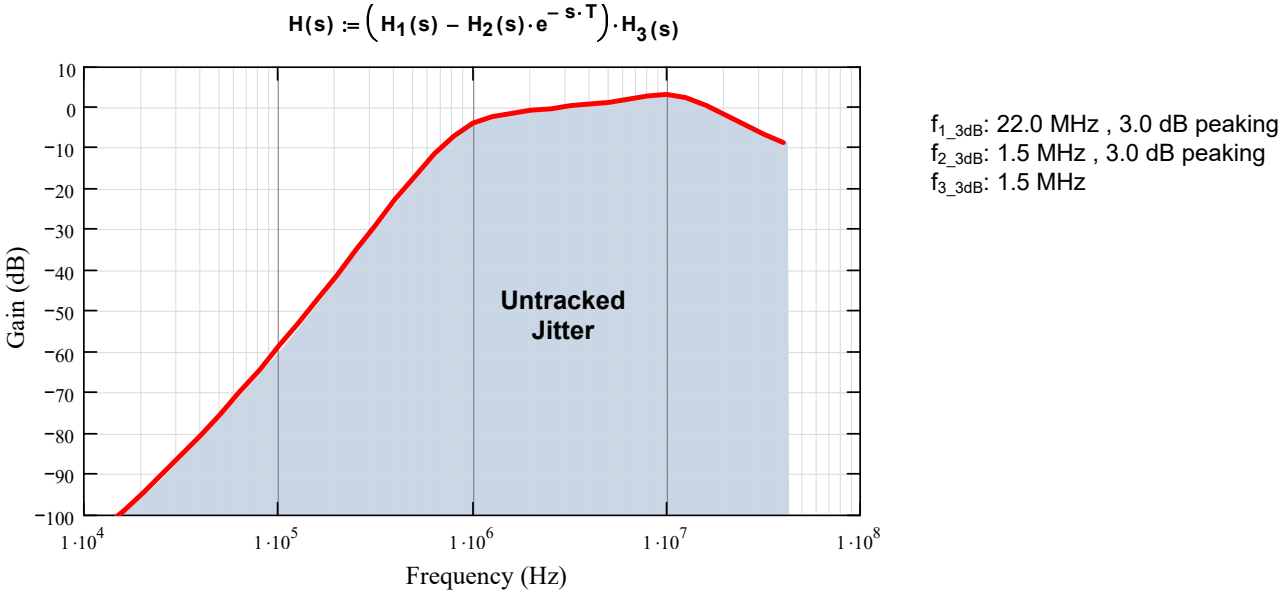


Figure 5. PCIe 1.1 Overall Transfer Function for the Common Clock RX Architecture

As shown in Figure 4 there are two possible TX PLL bandwidths available for PCIe 2.1, so we need to compute the worst case Refclk jitter using the two different bandwidth combination. PCIe 3.1 standard allows even more TX PLL and RX PLL bandwidth flexibility with 16 different bandwidth combinations and two transfer functions resulting in 32 unique combinations. Again, the resulting worst case jitter from these 32 combinations must be below the jitter limits specified by the PCIe standards. Refer to the Appendices at the end of this document for a listing of all possible parameter combinations and associated transfer functions.

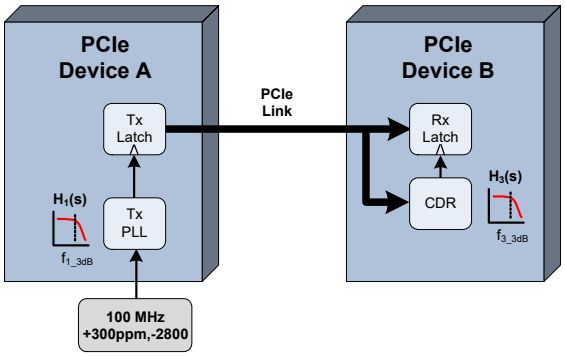
The Refclk jitter limits for all three PCIe standards after the overall transfer function(s) have been applied are shown in Table 1.

Table 1: Common Refclk RX Architecture Jitter Limits

	Description	Symbol	Limit	Units
PCIe 1.1	Random Jitter	R_j	4.7	ps pk-pk
	Deterministic Jitter	D_j	41.9	ps pk-pk
	Total Jitter where Tj = Dj + 14.069 x Rj (for BER 10^{-12})	T_j	108	ps pk-pk
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK} \div 2$)	J_{RMS-HF}	3.1	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	3.0	ps RMS
PCIe 3.1	Random Jitter	J_{RMS}	1.0	ps RMS
Note: All jitter measurements are filtered using the overall transfer function(s) defined in Figure 4 after all combinations of parameters have been exercised. See Appendix A–D.				

4.3. Jitter Requirements for the Data Clocked RX Architecture

The Refclk transmission path in a data clock RX architecture is much simpler than in the common clocked RX architecture since it only has one path. With this single path, the TX PLL and CDR do not share a common Refclk so the jitter transfer function only has the TX PLL transfer function plus the low pass characteristic of the CDR. This architecture requires the CDR to track all low frequency jitter including SSC. The jitter transfer functions for PCIe 2.1 and 3.1 are shown in Figure 7. The data clocked RX architecture is not defined for PCIe 1.1. Jitter limits are determined using all possible parameter combinations as outlined in Appendix A. The jitter limits for the data clocked RX architecture are shown in Table 2.



	PLL and CDR Transfer Functions
Tx PLL	$H_1(s) = \frac{2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}{s^2 + 2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}$
CDR 3.1	$H_3(s) = \frac{2 \cdot s \cdot \zeta_3 \cdot \omega_{n3} + \omega_{n3}^2}{s^2 + 2 \cdot s \cdot \zeta_3 \cdot \omega_{n3} + \omega_{n3}^2}$

	Overall Jitter Transfer Functions	Transfer Function Parameters
PCIe 1.1	Not defined in PCIe standards	
PCIe 2.1	$H(s) = H_1(s) \cdot H_{CDR}(s)$	f_{1_3dB} 16.0 MHz: 0.5 dB Peaking: $\omega_{n1} = 8.61 \cdot 2\pi$ Mrad/s, $\zeta_1 = 1.75$; 3.0 dB Peaking: $\omega_{n1} = 8.61 \cdot 2\pi$ Mrad/s, $\zeta_1 = 0.54$ $H_{CDR}(s) = \frac{s^2}{s^2 + 2\zeta\omega_m s + \omega_m^2}$ $\omega_m = 2\pi f_m \zeta = 0.707$, and $f_m = \frac{2x5MHz}{\sqrt{1+2\zeta 2+\sqrt{1+(1+(2\zeta^2)^2}}}$
PCIe 3.1	$H(s) = H_1(s) \cdot (1 - H_3(s))$	f_{1_3dB} 2.0 MHz: 0.01 dB Peaking: $\omega_{n1} = 0.448$ Mrad/s, $\zeta_1 = 14$; 1.0 dB Peaking: $\omega_{n1} = 4.62$ Mrad/s, $\zeta_1 = 1.15$ f_{1_3dB} 2.0 MHz: 2.0 dB Peaking: $\omega_{n1} = 6.02$ Mrad/s, $\zeta_1 = 0.73$ f_{1_3dB} 4.0 MHz: 0.01 dB Peaking: $\omega_{n1} = 0.896$ Mrad/s, $\zeta_1 = 14$; 2.0 dB Peaking: $\omega_{n1} = 12.04$ Mrad/s, $\zeta_1 = 0.73$ f_{1_3dB} 5.0 MHz: 0.01 dB Peaking: $\omega_{n1} = 1.12$ Mrad/s, $\zeta_1 = 14$; 1.0 dB Peaking: $\omega_{n1} = 11.53$ Mrad/s, $\zeta_1 = 1.15$ f_{3_3dB} 10 MHz: 0.5 dB Peaking: $\omega_{n3} = 16.57$ Mrad/s, $\zeta_3 = 1.75$; 2.0 dB Peaking: $\omega_{n3} = 33.8$ Mrad/s, $\zeta_3 = 0.73$

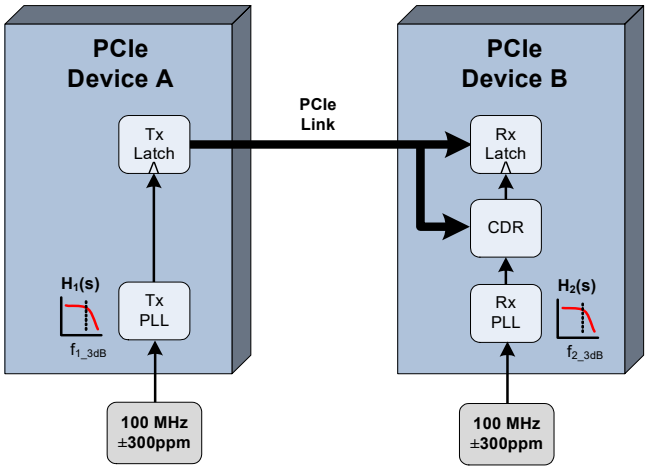
Figure 6. Jitter Transfer Functions for the Data Clocked RX Architecture

Table 2: Data Refclk RX Architecture Jitter Limits

	Description	Symbol	Limit	Units
PCIe 1.1	Not defined in PCIe standards			
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK} \div 2$)	J_{RMS-HF}	4.0	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	7.5	ps RMS
PCIe 3.1	Random Jitter	J_{RMS}	1.0	ps RMS
Note: All jitter measurements are filtered using the overall transfer function(s) defined in Figure 4 after all combinations of parameters have been exercised. See Appendix A.				

4.4. Jitter Requirements for the No SSC Separate Clock Architecture (SRNS)

The separate clock architecture uses two independent reference clocks for the transmitting and receiving PCIe devices as shown in Figure 7. Using two separate Refclks of 100 MHz ±300 ppm is possible because the PCIe standards allow for up to 600 ppm frequency separation between clocks. The consequence of using the entire frequency margin is that spread spectrum must be turned off for both Refclk sources.



$$H_1(s) := \frac{2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}{s^2 + 2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}$$

$$H_2(s) := \frac{2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}{s^2 + 2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}$$

	3.0 dB Peaking
f_{1_3dB} 16.0 MHz	$\omega_{n1} := 8.61 \cdot 2\pi$ Mrad/s $\zeta_1 := 0.54$

	3.0 dB Peaking
f_{2_3dB} 16.0 MHz	$\omega_{n2} := 8.61 \cdot 2\pi$ Mrad/s $\zeta_2 := 0.54$

$$X(s) := \sqrt{\left(X_1(s) \cdot H_1(s)\right)^2 + \left(X_2(s) \cdot H_2(s)\right)^2}$$

where, $X(s)$ – Total Jitter
$X_1(s)$ – Tx Refclk Jitter
$X_2(s)$ – Rx Refclk Jitter

Figure 7. Separate Clock Architecture

There is no overall jitter transfer function defined in the PCIe standards for this architecture. Since both Refclks are independent, their phase jitter is passed through the TX and RX PLLs independently and a maximum PLL bandwidth of 16 MHz with 3.0 dB of peaking should be assumed. Since both Refclks are independent, the random jitter components of each clock are added as a root sum square (RSS).

The PCIe standards do not specify jitter limits for this clock architecture, although it states that jitter must be considerably tighter than for the other two architectures. Ultimately the jitter limits will depend on the TX and RX PCIe device specifications.

5. Gen2 (5GB/s) and Gen3 (8GB/s) Jitter Requirements for the Separate Refclk with Independent SSC (SRIS)

Similar to the SRNS architecture at 5 Gb/s and 8 Gb/s, it is now a possibility that spread spectrum clocking can be independently applied via the refclk for the TX and RX as diagrammed in Figure 7. This architecture now burdens the RX with tracking and rejecting the phase shift between the RX and TX that is inherent in the two independent refclks with SSC. The ability to support this architecture requires the CDR to have a second order high-pass filter in the transfer function in order to reject the phase shift that is inherent in the independent SSC implementation. Equations 1 and 2 are the CDR transfer functions that should be used in the Gen2 and Gen3 systems respectively.

$$H_{CDR}(S) = \frac{s^2}{s^2 + 2\zeta\omega_m s + \omega^2 m}$$

Equation 1. Gen2 (5Gb/s) SRIS CDR Transfer Function

Where:

$$\omega_m = 2\pi f_m, \zeta = 0.70, \text{and } f_m = \frac{2 \times 5MHz}{\sqrt{1 + 2\zeta^2 + \sqrt{1 + (1 + 2\zeta^2)^2}}}$$

$$H_{CDR}(s) = \frac{s^2}{s^2 + sA + B} \times \frac{s^2 + 2\zeta_2\omega_0 s + \omega_0^2}{s^2 + 2\zeta_1\omega_0 s + \omega_0^2}$$

Equation 2. Gen3 (8GB/s) SRIS CDR Transfer Function

Where:

$$\zeta_1 = \frac{1}{\sqrt{2}}, \zeta_2 = 1, \omega_0 = 10^7 \times 2\pi, A = 2.2 \times 10^{12} \times 2\pi, \text{and } B = 2.2 \times 10^{12} \times 2\pi( )$$

Since the reference clocks are independent of each other and, given that their dominant jitter is random, then their combined impact on the system should be root sum square of the individual terms.

$$X_{SRIS} = \sqrt{[X_1(s) \times H_1(s) \times H_{CDR}(s)]^2 + [X_2(s) \times H_2(s) \times H_{CDR}(s)]^2}$$

Where $H_1(s)$ and $H_2(s)$ follow the same transfer functions as used in Figure 7.

Table 3. SRIS Jitter Limits for 5GB/s and 8GB/s

	Description	Symbol	Max Limit	Units
PCIe Gen2	RMS Refclk jitter for SRIS architecture at 5.0Gb/s (Gen2)	$T_{REFCLK-RMS-SRIS}$	2.0	ps RMS
PCIe Gen3	RMS Refclk jitter for SRIS architecture at 8.0Gb/s (Gen3)	$T_{REFCLK-RMS-SRIS}$	0.5	ps RMS

6. Spread Spectrum Clocking (SSC)

Spread spectrum clocking is a technique used to lower the amount of radiated electromagnetic interference (EMI) that is generated from high speed digital signals. Spread spectrum clocks use low frequency modulation of the carrier frequency to spread out the radiated energy across a broader range of frequencies. The frequency spectrum of a clock with and without spread spectrum is illustrated in Figure 8. Radiation from data lines transmitted with a device using a spread spectrum clock reference will also benefit from the same EMI reduction.

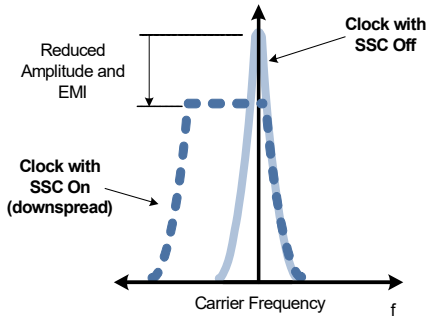


Figure 8. Spectrum Analyzer Plot of a Clock With and Without Spread Spectrum

PCIe devices are specified to reliably transmit data when using a Refclk with a spread spectrum modulation rate of 30–33 kHz and modulation amplitude of 0 to –0.5% (i.e., downspread 0.5% in reference to the carrier frequency). Because each PCIe device must transmit within a bit rate of ±300 ppm of each other, the same Refclk must be supplied to both devices if SSC is used. Therefore, in some system implementations, separate clocking architecture will not work if SSC is turned on unless both clocks are synchronized to a common source. In the case where the system is SRIS capable, the CDRs will be designed with loop filter characteristics such that the SSC can be tracked independently by the receiver allowing for SRIS support. The bandwidth of such a synchronizing clock (i.e., a phase-locked loop) must be high enough to track the 30–33 kHz modulation rate. For practical purposes, this means a TX or RX PLL must have a loop bandwidth greater than 1.5 MHz to ensure the SSC clock is tracked. Using SSC is possible for the Separate Reflck, Common Clocked RX Architecture, and Data Clocked RX Architecture.

In addition to the SSC modulation rate and modulation amplitude, there is an additional requirement for the maximum rate of change of the frequency on a Refclk with SSC active at 1250 ppm/µs. Refclks with the SSC active will need to meet additional phase jitter requirements at low frequency as shown in Table 2.

Table 4. Limits for Phase Jitter from the Reference Clock with SSC Active

Frequency	Maximum Peak to peak phase jitter (ps)
30 kHz – 33 kHz	25000
100 kHz	1000
500 kHz	25

7. HCSL Output Signal Format

The host clock signal level (HCSL) is the output signal format specified by the PCI Express Card Electromechanical Specification 2.0 for the Refclk signal and it is commonly found in the PC and Server markets. Using a standardized signaling level for Refclk ensures compatibility between PC motherboards and add-in cards manufactured by different vendors.

HCSL is a differential current mode signal that nominally swings from 0 V to 700 mV. HCSL is a point-to-point signal format meaning that a separate output driver is required to drive each PCIe device. Multidrop connections (one output driver to multiple devices) are not supported. HCSL drivers are source terminated as shown in Figure 9.

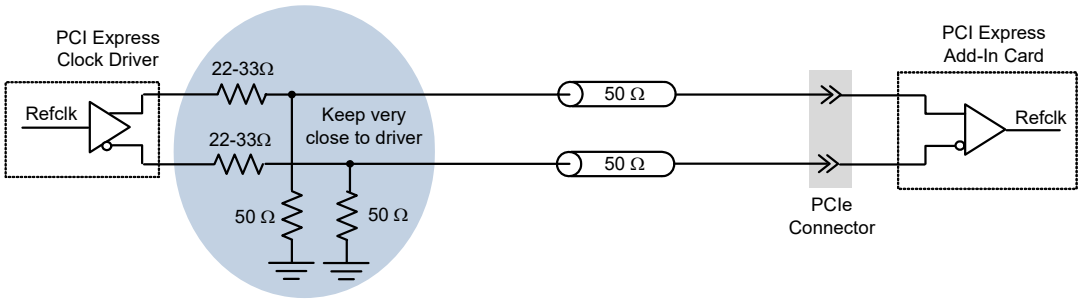


Figure 9. HCSL Output Driver Termination

Systems that don't require compatibility with PCIe add-in cards or PCIe functions implemented in FPGAs can use other Refclk signal formats. LVDS, LVPECL, and even LVCMOS are common.

8. REFCLK Test Setup

The reference clock test setup as defined in the 3.1 specification assumes that only the reference clock generator is present. It takes the approach of measuring with the worst case system degradation in place using a 12-inch differential trace that is terminated by two 2 pF capacitors.

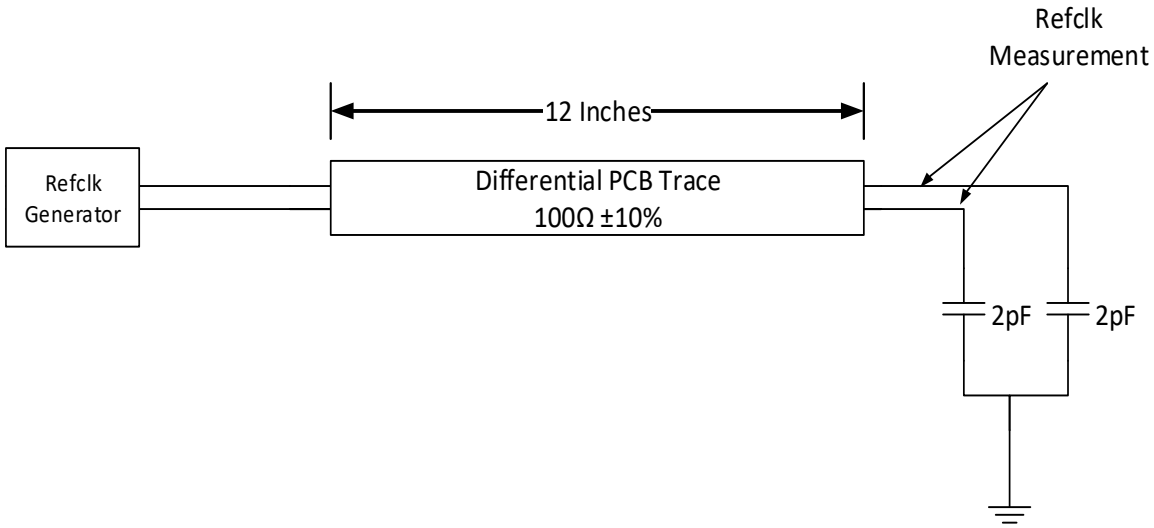


Figure 10. REFCLK Test Setup

9. A Typical PCI Express Application

Skyworks Solutions offers a variety of clock devices that allows for flexible PCIe Refclk distribution. For example, the Si5338 *I²C Programmable Any-Frequency, Any-Output Quad Clock Generator* is an ideal device for generating PCIe clocks:

- Compliant with PCI Express 3.1 and legacy standards (2.1, 1.1)
- PCI Express 3.1 jitter = 0.12 ps RMS (10x lower than the requirement)
- Generates up to four 100 MHz HCSL output clocks but is programmable with other frequencies and signal formats. This allows one clock device to generate PCIe Refclks and other board clocks of different frequencies and signal formats.
- Output frequencies are programmable per output from 5 MHz to 710 MHz.
- Independent VDDO for each output clock enables integrated level translation.
- Output signal formats are programmable per output as HCSL, LVDS, LVPECL or LVCMOS.
- Excellent jitter performance allows Refclk generation for Common Refclk RX, Data Clocked RX, and Separate Clock Architectures.
- Spread spectrum can be enabled or disabled per output with programmable modulation rate and modulation amplitude per output.
- Built-in HCSL terminations.
- Small 4x4 mm package

A typical use of the Si5338 in a PCIe application is shown in Figure 11. In this example the Si5338 replaces a 100 MHz clock oscillator with spread spectrum, a 1:2 HCSL buffer, a 66.6667 MHz clock oscillator, and a 125 MHz clock oscillator.

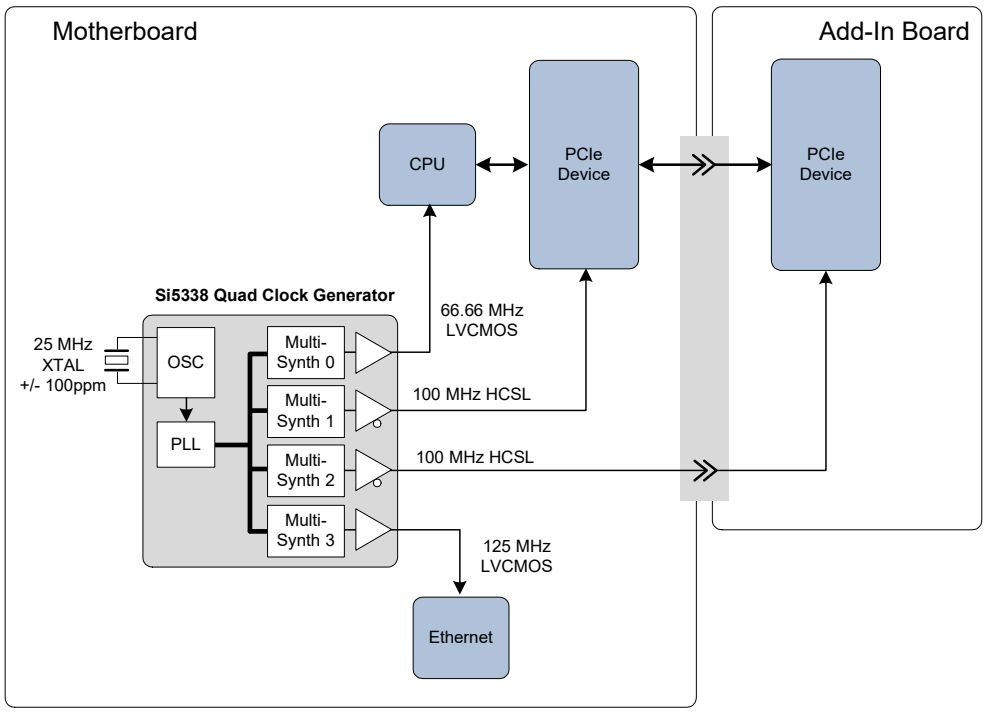


Figure 11. PCIe Application Using the Si5338 as the Refclk Generator

10. Conclusion

There are several things to consider when choosing the right reference clock for a PCI Express application. Jitter performance is a key consideration for ensuring efficient and reliable data transfer between two PCIe devices. This can only be guaranteed by choosing a device that specifies jitter across all PLL and CDR bandwidths and clocking architecture transfer functions. A clock with selectable spread spectrum can also be an important consideration for meeting EMI requirements. In some cases PCIe clocks need flexible output signal formats and frequencies other than the standard 100 MHz HCSL signal format. A clock generator like the Si5338 provides the reliability and flexibility needed to meet all PCI Express applications and requirements.

11. References

- PCI Express Base Specification Revision 1.1, March 28, 2005.
- PCI Express Jitter and BER Revision 1.0, February, 2005.
- PCI Express Card Electromechanical Specification Revision 2.0, April 11, 2007.
- PCI Express Base Specification Revision 2.1, March 4, 2009.
- PCI Express Base Specification Revision 3.1, October 8, 2014.
- Skyworks Solutions *Si5338 I^{2}C Programmable Any-Frequency, Any-Output Quad Clock Generator* data sheet.

APPENDIX A—PCIE COMPLIANCE REPORT