Si5214x and Si5315x Signal Integrity Tuning to Improve Connectivity

1. Introduction

In today's high-speed semiconductor technology, interfacing the high-speed components poses a major challenge. The output driver is one of the crucial components for determining device performance and successful interfacing. High-speed systems with tighter timing budgets require high rise and fall times (i.e., faster slew rates, specific skew requirements, and excellent signal quality).

In many high-speed integrated circuit environments, interfacing issues are faced across input-output buffers. In addition, the circuit board layout or traces are likely to add to the interfacing problems. For better performance in the end application, Skyworks Solutions products offers flexibility in adjusting slew rate (Tr, Tf), skew adjustments, and output impedance selections to improve connectivity on the application board.

Skyworks Solutions' high-speed clocks come with an option to adjust these ac parameters through I^2C/SMBus connectivity. By using the factory programming methodology of OTP programming, the specific user requirements can be made the default performance at power on. This application note discusses how to fine tune the ac parameters through I^2C/SMBus for better performance.

2. Programming AC Performance Registers

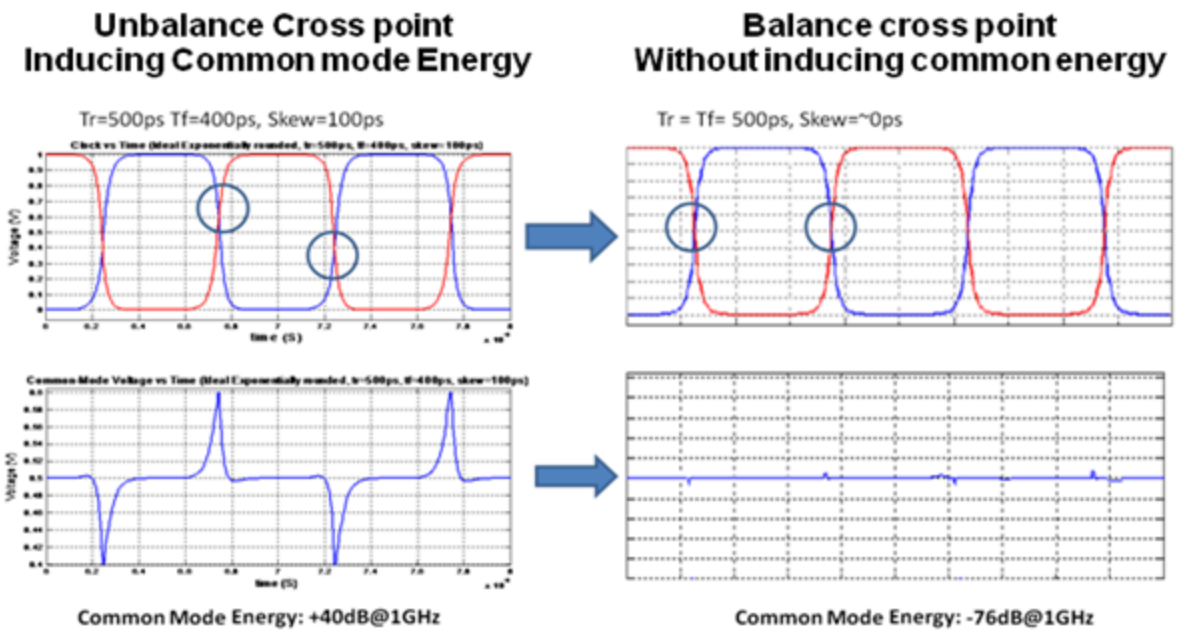
To alter the ac performance of an output, certain registers corresponding to the output need to be altered. Depending on the signaling type, there are two sets of control registers: single ended control registers and differential control registers. Differential signals have two sets of registers: Register A and Register B. Currently the PCIe products support single ended outputs at default 3.3 V and LVCMOS differential outputs only.

2.1. Slew Rate

Skyworks Solutions' PCIe clocks allow the user the option of programmable rise/fall times (slew rate) by varying the drive strength of the output buffers. It is possible to control rise times and fall times differently to suit board indiscretions or as per receiving unit's timing budget, which may be a CPU, GPU, PCI-Express controller, chipset or any other device requiring clocking input. For the differential outputs, the slew rate can be adjusted in coarse and fine regulation using Register A[bit 1].

2.2. Skew (for Differential Outputs)

The PCIe family clocks allow the user to customize the skew on the differential signal to adjust the skew with respect to other clocking signals. Also, the skew parameter on true and complement can be controlled individually to assist with cross point optimization. Unstable or unmatched cross point causes data loss and high common mode energy which induces EMI. The cross point can be balanced using this feature to minimize these imperfections by programming 0 skew between true and complement signals.



2.3. Output Impedance

The output impedance of load along with the trace may vary from what is expected and result in overshoots and undershoots or ripples in the clock output waveform. These ripples can be minimized by adjusting the output impedance of the particular clock output under consideration. Each clock output has individual impedance and other parameters control independent of other outputs.

3. Parameter Control Registers

3.1. Single Ended Control Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OP_IMP[1]	OP_IMP[0]	INV	SLEW[1]	SLEW[0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>7:6</td><td>OP_IMP[1:0]</td><td>Output Impedance Control.
00: High-Z
01: 50 Ω
10: 25 Ω (default)
11: 17 Ω</td></tr>
<tr><td>5</td><td>INV</td><td>Inverts clock output.</td></tr>
<tr><td>4:3</td><td>SLEW[1:0]</td><td>Slew Rate Control.
<table>
<tr><th colspan="2"></th><th>Byte18[7:6] = 11</th><th>Byte18[7:6] = 10</th><th>Byte18[7:6] = 01</th></tr>
<tr><th colspan="2"></th><th>17 Ω</th><th>25 Ω</th><th>50 Ω</th></tr>
<tr><th>Byte18[4:3]</th><th>Setting</th><th>Slew Rate (ns)</th><th>Slew Rate (ns)</th><th>Slew Rate (ns)</th></tr>
<tr><td>00</td><td>Slowest</td><td>0.868</td><td>1.004</td><td>1.531</td></tr>
<tr><td>01</td><td>Slow</td><td>0.775</td><td>0.917</td><td>1.449</td></tr>
<tr><td>10</td><td>Fast</td><td>0.548</td><td>0.667</td><td>1.212</td></tr>
<tr><td>11</td><td>Fastest</td><td>0.475</td><td>0.579</td><td>1.109</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>Reserved</td><td>Note: Do not change these bits while re-writing the register values.</td></tr>
</table>

3.2. Differential Control Registers

Register A

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_IMP[1]		FALL_INC[1]	FALL_INC[0]	RISE_INC[1]	RISE_INC[0]	COARSE_ FINE	SKEW_SEL_- COMP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_IMP[0]				SKEW_INC[2]	SKEW_INC[1]	COARSE_ FINE	SKEW_SEL_ TRUE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th><th>Function</th></tr>
<tr><td>7</td><td>DIFF_IMP</td><td>Configure differential output impedance</td><td>
<table>
<tr><th>Register A Bit 7</th><th>Register B Bit 7</th><th>DIFF_IMP</th></tr>
<tr><td>0</td><td>0</td><td>High-Z</td></tr>
<tr><td>0</td><td>1</td><td>50 Ω (default)</td></tr>
<tr><td>1</td><td>0</td><td>33 Ω</td></tr>
<tr><td>1</td><td>1</td><td>20 Ω</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>Reserved</td><td>Reserved</td><td>
<table>
<tr><th>Register A Bit 6</th><th>Register B Bit 6</th><th></th></tr>
<tr><td>Reserved</td><td>Reserved</td><td>Note: Do not change these bits while re-writing the register values.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th><th>Function</th></tr>
<tr><td>5:4</td><td>FALL_INC[1:0]</td><td>Fall Time Increment</td><td>
<table>
<tr><th>Register A Bit[5:4]</th><th>Fall time (ps) with Register A Bit 1 = 0</th><th>Fall time (ps) with Register A Bit 1 = 1</th></tr>
<tr><td>00</td><td>Nominal [default]</td><td>Nominal</td></tr>
<tr><td>01</td><td>+40 ps</td><td>+80 ps</td></tr>
<tr><td>10</td><td>+50 ps</td><td>+140 ps</td></tr>
<tr><td>11</td><td>+70 ps</td><td>+210 ps</td></tr>
</table>
<table>
<tr><th>Register B Bit[5:4]</th><th></th></tr>
<tr><td>Reserved</td><td>Note: Do not change these bits while re-writing the register values.</td></tr>
</table>
</td></tr>
<tr><td rowspan="2">3:2</td><td>RISE_INC[1:0]</td><td>Rise Time Increment</td><td rowspan="2">
<table>
<tr><th>Register A Bit[3:2]</th><th>Rise time (ps) with Register A Bit 1 = 0</th><th>Rise time (ps) with Register A Bit 1 = 1</th></tr>
<tr><td>00</td><td>Nominal [default]</td><td>Nominal</td></tr>
<tr><td>01</td><td>+40 ps</td><td>+80 ps</td></tr>
<tr><td>10</td><td>+50 ps</td><td>+140 ps</td></tr>
<tr><td>11</td><td>+70 ps</td><td>+210 ps</td></tr>
</table>
<table>
<tr><th>Register B Bit[3:2]</th><th>Skew (ps) with Register B Bit 1 = 0</th><th>Skew (ps) with Register B Bit 1 = 1</th></tr>
<tr><td>00</td><td>Nominal</td><td>+ 355 ps</td></tr>
<tr><td>01</td><td>+ 20 ps</td><td>+ 415 ps</td></tr>
<tr><td>10</td><td>+ 50 ps</td><td>+ 510 ps</td></tr>
<tr><td>11</td><td>+ 70 ps</td><td>+ 575 ps</td></tr>
</table>
</td></tr>
<tr><td>SKEW_INC[1:0]</td><td>Skew Time Increment</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th><th>Function</th></tr>
<tr><td>1</td><td>COARSE_FINE</td><td>Set slew rate setting to be coarse or fine setting</td><td>
<table>
<tr><th>Register A Bit[5:4]</th><th>Slew Rate Setting</th></tr>
<tr><td>0</td><td>Coarse slew rate adjust</td></tr>
<tr><td>1</td><td>Fine slew rate adjust</td></tr>
</table>
<table>
<tr><th>Register B Bit 1</th><th>Skew Rate Setting</th></tr>
<tr><td>0</td><td>Fine skew adjust</td></tr>
<tr><td>1</td><td>Coarse skew adjust</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>SKEW_SEL</td><td>Set skew setting as per Register B[3:2] on True and Complement outputs</td><td>
<table>
<tr><th>Register A Bit 0</th><th>SKEW_SEL_COMP</th></tr>
<tr><td>0</td><td>No skew added on Complement output</td></tr>
<tr><td>1</td><td>Add skew on Complement output as per setting in Register B[3:2]</td></tr>
</table>
<table>
<tr><th>Register B Bit 0</th><th>SKEW_SEL_TRUE</th></tr>
<tr><td>0</td><td>No skew added on True output</td></tr>
<tr><td>1</td><td>Add skew on True output as per setting in Register B[3:2]</td></tr>
</table>
</td></tr>
</table>

4. Procedure to Vary AC Performance through I²C Bus

1. Power on the device and connect the output under test and I²C communication through appropriate software like iPort Commlink.
2. Set the communication address to device address (usually D2'h). Make sure I²C connections are communicating by reading back the registers starting from Register 0 and compare with data sheet defaults.
3. Increase Register count to access beyond register 8 (for block read/write operation) by writing Register 4 to 80H.
4. Write Byte 63 (Byte 3F'h) to 01'h to access AC Performance Control page of the respective outputs through I²C.
5. Select appropriate output or byte number to access from “Output-to-Register mapping” table. Read back the content of selected register/registers. Note that the Single ended outputs have single control register and Differential outputs have two control registers.
6. Modify only the bits for altering the ac performance of the output from Control Registers. Write back the new register value to the same register number without altering the reserved bits in the register.
7. Monitor the change in parameter.
8. Note that power cycling the device in between from steps a to g will reset the parameter to default state and the procedure needs to be started from step 1.
9. Finally, the user must write Byte 63 (Byte 3F'h) to 00'h to return to “Core” segment page of the Control Registers. Otherwise, the addressed location remains in AC Performance Control block and for further updates the changes do not take affect.

5. Output to Register Mapping Tables

5.1. Si52142 Output-to-Register Mapping

Si52143 Pin#	Output Description	Differential Output Control		Single Ended Output Control
		Register A	Register B	
2	REF	—	—	18
13	DIFF0	51	52	—
14	$\overline{\text{DIFF0}}$			—
15	DIFF1	53	54	—
16	$\overline{\text{DIFF1}}$			—

5.2. Si52143 Output-to-Register Mapping

Si52143 Pin#	Output Description	Differential Output Control		Single Ended Output Control
		Register A	Register B	
2	REF	—	—	18
8	DIFF0	43	44	—
9	$\overline{\text{DIFF0}}$			—
10	DIFF1	49	50	—
11	$\overline{\text{DIFF1}}$			—
13	DIFF2	51	52	—
14	$\overline{\text{DIFF2}}$			—
15	DIFF3	53	54	—
16	$\overline{\text{DIFF3}}$			—

5.3. Si52144 & Si53154 Output-to-Register Mapping

Si52144/ Si53154 Pin#	Output Description	Differential Output Control	
		Register A	Register B
8	DIFF0	43	44
9	$\overline{\text{DIFF0}}$		
10	DIFF1	49	50
11	$\overline{\text{DIFF1}}$		
13	$\overline{\text{DIFF2}}$	51	52
14	DIFF2		
15	$\overline{\text{DIFF3}}$	53	54
16	DIFF3		

5.4. Si52146 & Si53156 Output-to-Register Mapping

Si52147/Si53159 Pin#	Output Description	Differential Output Control	
		Register A	Register B
9	DIFF0	37	38
10	$\overline{\text{DIFF0}}$		
11	DIFF1	43	44
12	$\overline{\text{DIFF1}}$		
14	DIFF2	49	50
15	$\overline{\text{DIFF2}}$		
17	$\overline{\text{DIFF3}}$	51	52
18	DIFF3		
19	$\overline{\text{DIFF4}}$	53	54
20	DIFF4		
22	$\overline{\text{DIFF5}}$	59	60
23	DIFF5		

5.5. Si52147 & Si53159 Output-to-Register Mapping

Si52147/Si53159 Pin#	Output Description	Differential Output Control	
		Register A	Register B
14	DIFF0	37	38
15	$\overline{\text{DIFF0}}$		
17	DIFF1	43	44
18	$\overline{\text{DIFF1}}$		
19	DIFF2	45	46
20	$\overline{\text{DIFF2}}$		
21	DIFF3	49	50
22	$\overline{\text{DIFF3}}$		
25	$\overline{\text{DIFF4}}$	51	52
26	DIFF4		
27	$\overline{\text{DIFF5}}$	53	54
28	DIFF5		
30	$\overline{\text{DIFF6}}$	59	60
31	DIFF6		
32	$\overline{\text{DIFF7}}$	61	62
33	DIFF7		
35	$\overline{\text{DIFF8}}$	67	68
36	DIFF8		

NOTES:

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