# Using the Si826x Family of Isolated Gate Drivers

## 1. Introduction

Optocoupled gate drivers (a.k.a. “opto-drivers”) provide both galvanic signal isolation and output level shifting in a single package. Opto-drivers are notorious for long propagation times, poor common-mode transient immunity (CMTI), and performance degradation associated with temperature and device age. Modern isolated gate drivers fabricated in CMOS process technology offer higher performance and reliability with none of the downside found in opto-drivers. The Skyworks Solutions Si826x family of digital isolators (available in peak output currents of 0.6 A or 4.0 A) can directly replace opto-drivers while providing substantial gains in performance and reliability. This application note describes how to correctly apply the Si826x. (For more information about Skyworks Solutions CMOS isolation technology and comparisons with optocouplers, please see Skyworks Solutions' white paper “CMOS Digital Isolators Supersede Optocouplers in Industrial Applications”. For more information on the Si826x isolated gate driver family, see the Si826x product data sheet. Both publications are available for download at https://www.skyworksinc.com/technical%20documents.

## 2. Opto-Driver Overview

The opto-driver shown in Figure 1 consists of an input side LED with a transparent shield to reduce capacitive coupling, an optical receiver, and an output driver. The LED emits light when sufficient current flows from anode to cathode. This light passes through the transparent shield and strikes the optical receiver's photo diode, causing bias current flow from VDD to the gate driver, forcing Vo high. An absence of current through the input side LED causes the gate driver output to transition and remain low.

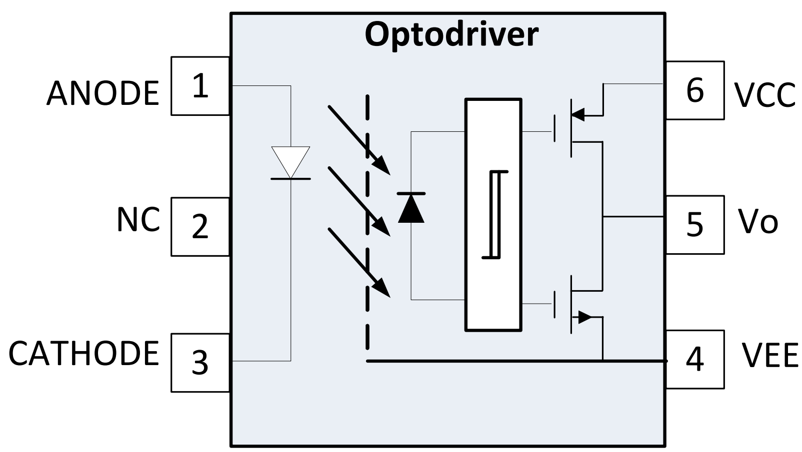


**Figure 1. Opto-Driver Block Diagram**

Opto-driver weaknesses include low reliability, narrow operating temperature ranges, temperature-dependent key timing specifications, and reduced LED device service life and reliability when subjected to excessive temperature, current, and device age. Designers typically allow extra design margin and/or add external components to mitigate these weaknesses.

## 3. Twenty-First Century Isolated Gate Drivers

The input-side diode emulator shown in Figure 2 mimics the behavior of an opto-driver LED to ensure compatibility with existing opto-driver input circuits. The diode emulator enables the high-frequency transmitter when input current IF is at or above its threshold value, sending a high-frequency carrier across the isolation barrier to the receiver. This high-selectivity receiver forces the output driver high when sufficient in-band energy is detected. Input current below the IF threshold disables the transmitter, causing the receiver to force the output driver low.

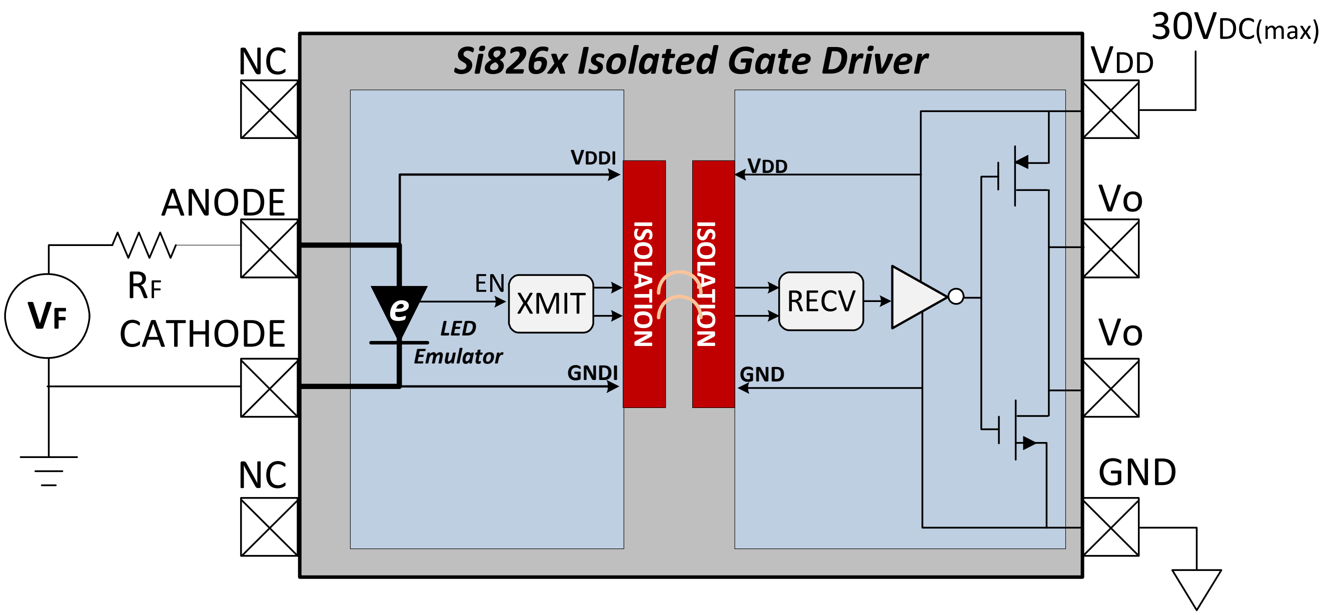


**Figure 2. Si826x Isolated Gate Driver**

Si826x benefits include isolated gate drive and level shifting in a single package, strong rejection of external fields, wider operating temperature range, higher precision current thresholds, faster and more consistent timing performance, lower-power operation, and higher reliability compared to opto-drivers. Furthermore, the lack of opto-driver liabilities allows designers to take full advantage of the extra design margin offered by the Si826x. The Si826x achieves this higher level of performance and reliability, primarily due to its architecture and fabrication methodologies:

- **Fabricated in Mainstream Low-Power CMOS**
  CMOS process technology enables high device integration and speed, low power consumption, high resistance to device temperature and aging effects, stable operation over the –40 to +125 °C temperature range, and exceptionally high reliability. The Si826x isolation barrier lifetime is 10 times higher than that of opto-drivers, and part-to-part matching is 14 times tighter than the Gallium Arsenide (GaAs) process technologies of opto-drivers.
- **High-Frequency Carrier Wave instead of Light**
  The high-frequency carrier brings the benefits of lower device operating power, faster device response, and superior noise rejection. The fully-differential signal path and high receiver selectivity provide CMTI immunity of >50 kV/µs (typ), external RF field immunity as high as 300 V/m, and magnetic field immunity above 1000 A/m for error-free operation.
- **Use of Proprietary Design Techniques to Suppress EMI**
  Devices in this family meet FCC Part B emission standards using automotive J1750 (CISPR) test methods. For more information on CMOS isolator emissions, susceptibility, and reliability compared to optocouplers, please see Skyworks Solutions white paper "CMOS Isolators Supersede Optocouplers in Industrial Applications" available at https://www.skyworksinc.com/technical%20documents.

# 4. Device Application

## 4.1. Si826x Device Transfer Characteristics

Figure 3 illustrates the device transfer characteristics where an anode current of 6 mA is required to achieve rated CMTI of 35 kV/µs (min) and 50 kV/µs (typ). A driver output-high event begins when the anode current crosses the Input Current Threshold, ~3.6 mA. A driver output-low event begins when the input current falls below the ~3.2 mA threshold and continues falling to zero to achieve rated CMTI performance. Note that Si826x devices must have a voltage drop above the Input Forward Voltage (ON), 1.6 to 2.8 V across the input during those periods when the driver output voltage is high.

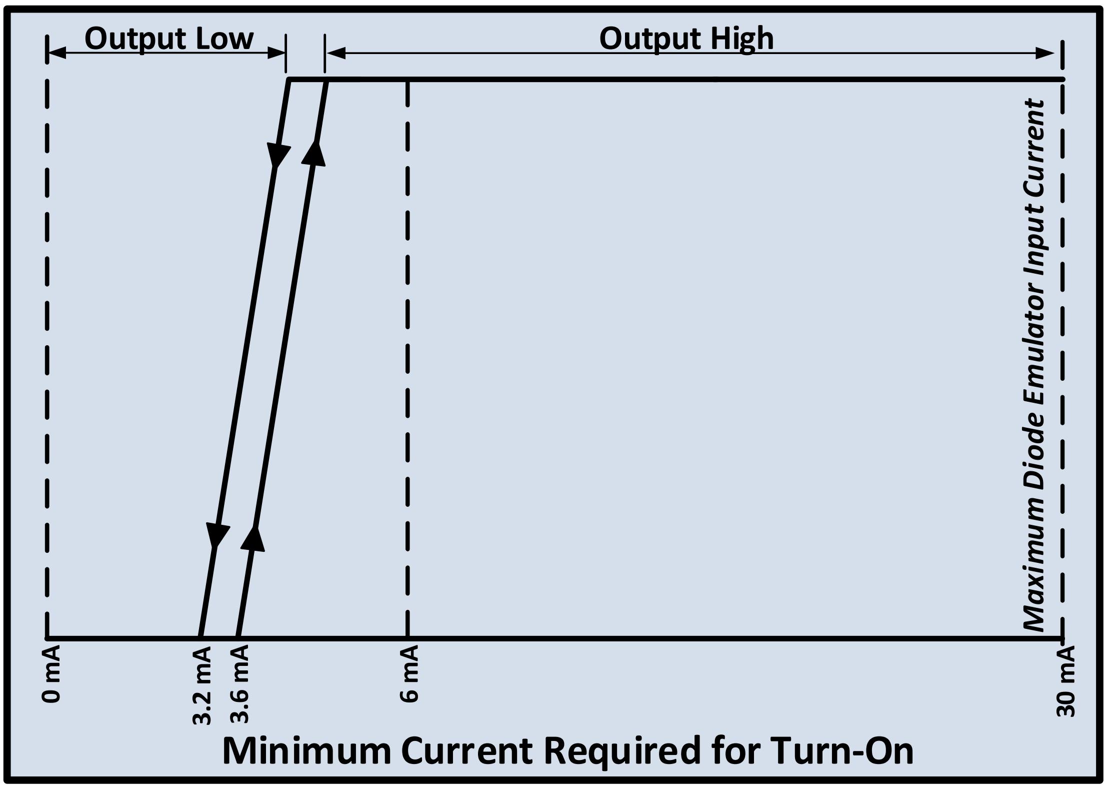


**Figure 3. Si826x Device Transfer Characteristics**

## 4.2. Replacing Legacy Opto-Drivers with the Si826x

The Si826x drops directly into the opto-driver landing site with no changes to the PCB. Opto-drivers sometimes use added external circuitry to enhance noise performance (typical examples include reverse bias and LED shorting switches). These components may be left intact or may be removed depending on the end application. High electrical noise environments should drive the anode input through a low-impedance source for best CMTI performance. The input circuit should not allow the LED emulator to be open-circuited and thereby vulnerable to parasitic coupling that can corrupt data transmission, as shown in Figure 4.

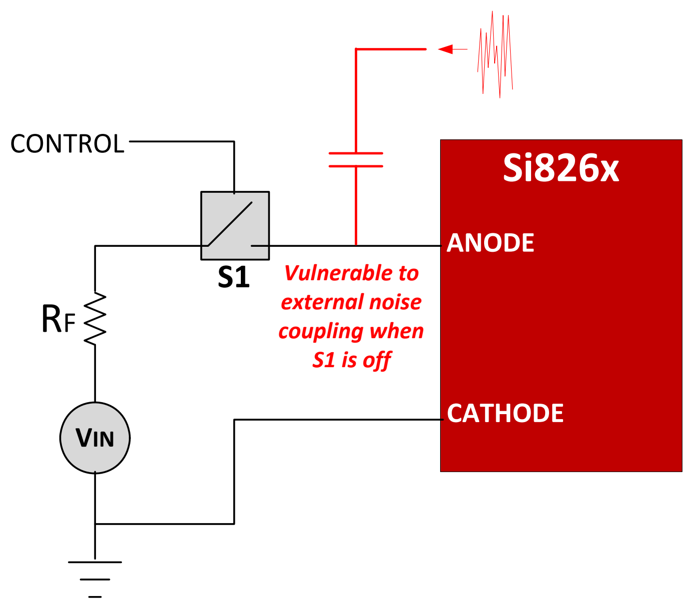


**Figure 4. Poor Input Circuit Design**

The input circuit of Figure 5 shows a simple but effective input circuit using R1 to increase common-mode transient immunity (i.e., the lower the value of R1, the higher the CMTI). Resistor values for R1 can range from 100 Ω to 1,000 Ω; however, these values can be adjusted to meet a designer's needs as long as the device specifications are not violated. The user can optimize the value of RF to achieve the best compromise between power dissipation and CMTI performance. Resistor R1 can also be replaced with a switch to further enhance CMTI performance.

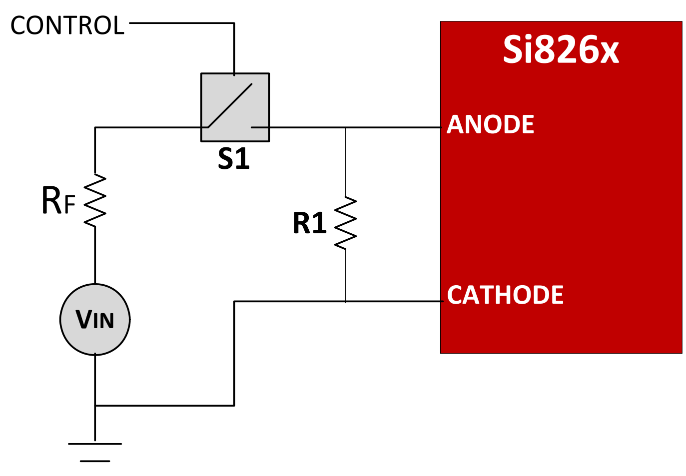


**Figure 5. Cost-Effective, High CMTI Circuit**

The circuit shown in Figure 6 uses a complementary buffer (e.g., MCU port I/O pin, dedicated buffer, discrete circuit, etc.) to drive the anode pin. This circuit offers a balance of low impedance off/on drive and relatively low-power operation by optimizing the value of RF for best CMTI performance.

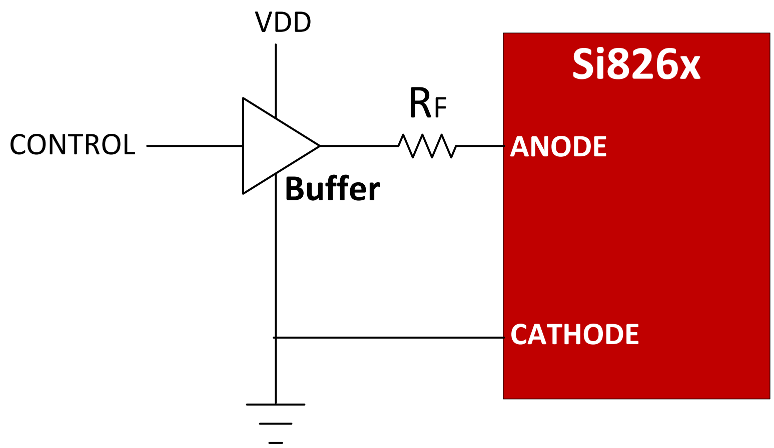


**Figure 6. Complementary Output Buffer Drive**

This section details how to select the $R_F$ resistor value to achieve high CMTI performance and low power operation for a given minimum Input ON Current ($I_{(ON)\_MIN}$) that was chosen by the designer. For this chosen current, the $R_F$ resistor value can be determined by the following equation:

$$I_{(ON)\_MIN} = \frac{VDD - V_{F(ON)\_MAX}}{R_F + R_S}$$

By rearranging the above equation and solving for $R_F$, the $R_F$ formula is given by

$$R_F = \frac{VDD - V_{F(ON)\_MAX}}{I_{(ON)\_MIN}} - R_S$$

The formula for maximum Input ON Current ($I_{(ON)\_MAX}$) is:

$$I_{(ON)\_MAX} = \frac{VDD - V_{F(ON)\_MIN}}{R_F + R_S}$$

Where:

$V_{F(ON)\_MAX}$ is the maximum $V_{F(ON)}$ voltage (2.8 V listed in Si826x data sheet)

$V_{F(ON)\_MIN}$ is the minimum $V_{F(ON)}$ voltage (1.6 V listed in Si826x data sheet)

VDD is the diver supply voltage

Rs is the drive source impedance

The following examples illustrate how to calculate a typical $R_F$ resistor value with the following given:

With VDD = 5.0 V, Rs = 50 Ω and $I_{(ON)\_MIN}$ = 6.0 mA, then:

$$R_F = \frac{5.0V - 2.8V}{6.0mA} - 50\Omega = 367\Omega$$

Using standard resistor series value, $R_F$ is set to 360 Ω from which $I_{(ON)MAX}$ is calculated to be:

$$I_{(ON)\_MAX} = \frac{5.0V - 1.6V}{350\Omega + 50\Omega} = 8.5mA$$

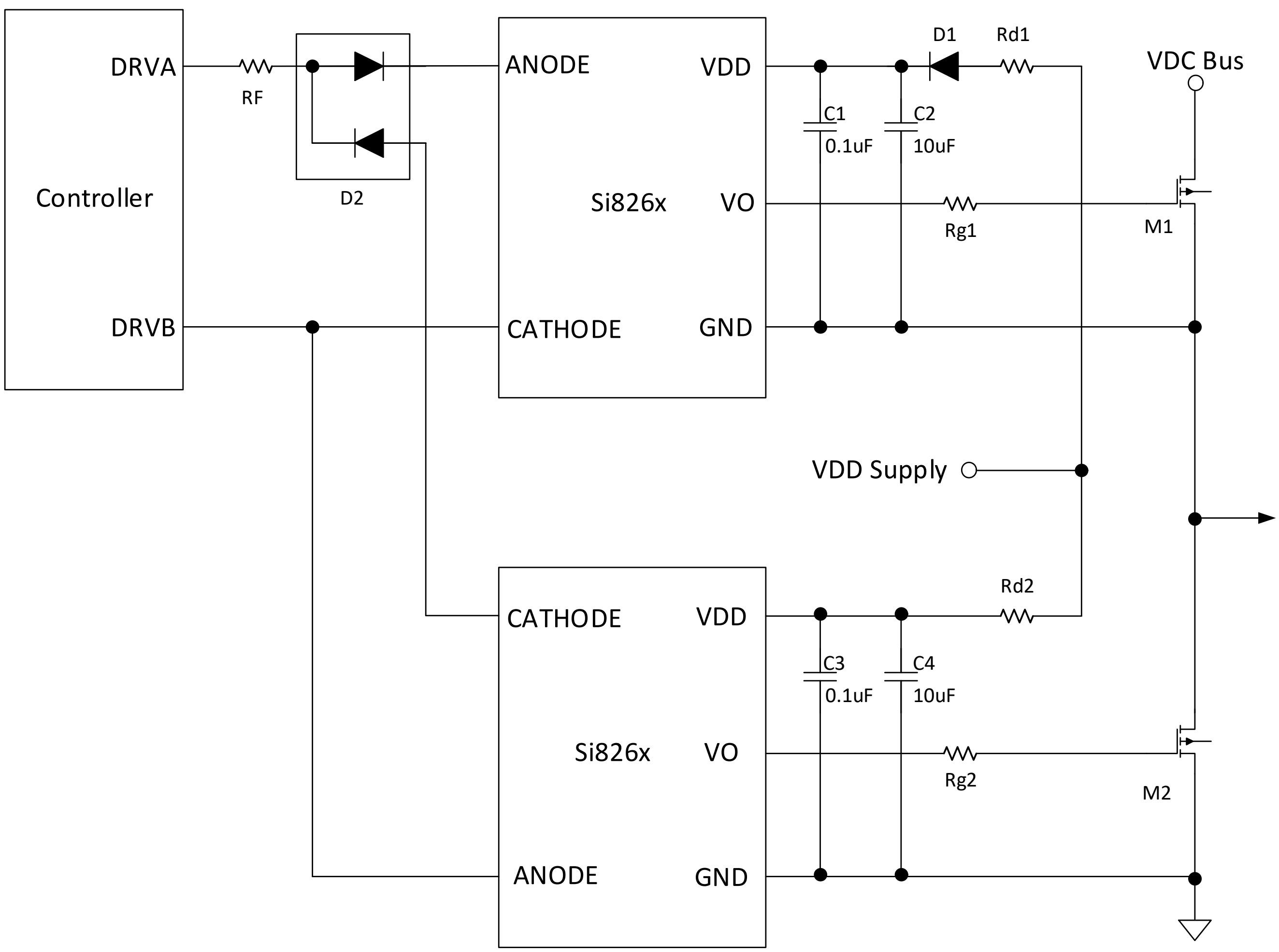


**Figure 7. Opto-Driver Replacement in Legacy High-side/Low-Side Application**

In legacy high-side/Low-side Opto-driver applications, the two inputs of the high-side Opto-driver and low-side Opto-driver are reversely connected for noise immunity and dead time control. The input of an Opto-driver has a true LED diode inside, therefore the Reverse Input Voltage can stand up to 5 V. As shown in Figure 7, the input circuit of the Opto-driver doesn’t need the D2 diode. However, the input of Si826x device has a CMOS circuit (LED Emulator) to simulate the Opto-driver input LED diode and can only be reversed biased to 0.3V. Therefore, for these types of applications that use the Si826x, the circuit shown in Figure 7 uses a two-diode packaged D2 component (SOT-23 package) to block the reverse voltage applied to the Si826x inputs and protect the Si826x’s input ESD diode. Thus, the circuit with D2 can be used in legacy high-side/low-side application for Opto-driver replacement.

# 5. Layout Recommendations

## 5.1. Bypass Capacitors

The output bypass capacitors consist of a parallel combination of a 0.1 µF high-frequency bypass and a 10 µF bulk capacitor connected between VDD and GND and placed as close as possible to the package. Ceramic capacitors should be used for VDD bypass because of their low impedance, high ripple current characteristics, small physical size, and cost-effectiveness.

## 5.2. Layout Guidelines

Ensure that no traces are routed through the creepage/clearance areas of the isolator. It is recommended that the NC pins on the Si826x input side be connected to the input side ground plane since this increases CMTI performance by reducing coupling to the input pins. Minimize the trace lengths between isolators and connecting Si826x circuitry. To enhance the robustness of a design in excessively noisy systems, it is further recommended that the user also include a resistor in series with the input and a capacitor in parallel with the input to form a low-pass filter for noise suppression, place the VDD bypass capacitors close to the VDD pin.

## 6. Summary

The Si826x is the ideal upgrade for legacy opto-drivers in both existing and new isolated gate driver designs. These devices outperform their opto-driver counterparts, adding significant gains in device performance and reliability. Si826x family members can directly replace any one of a number of opto-drivers from numerous suppliers.

# REVISION HISTORY

## Revision 0.5

August, 2019

- Updated "4.1. Si826x Device Transfer Characteristics" on page 3.
- Updated "4.2. Replacing Legacy Opto-Drivers with the Si826x" on page 4.
- Updated "5.2. Layout Guidelines" on page 7.

## Revision 0.4

April, 2013

- Extensive rewrite of document.

## Revision 0.3

August, 2012

- Updated Figure 3 on page 3.
- Added "3.2.1. Si826x Input Circuit Configurations to Maximize CMT Performance" on page 4.
- Rewrote "3.3. Determining Peak Gate Drive Current" on page 6.
- Rewrote "3.4. Output-Side VDD Bypass Capacitor" on page 7.

## Revision 0.2

April, 2012

- Updated "2. Opto-Driver Overview" on page 1.
- Updated Figure 2 on page 2.
- Updated "3.2. External Input Circuits" on page 4.
- Updated Figure 4 on page 4.
- Updated "4. Summary" on page 11.

## Revision 0.1

April, 2012

- Initial release.

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