

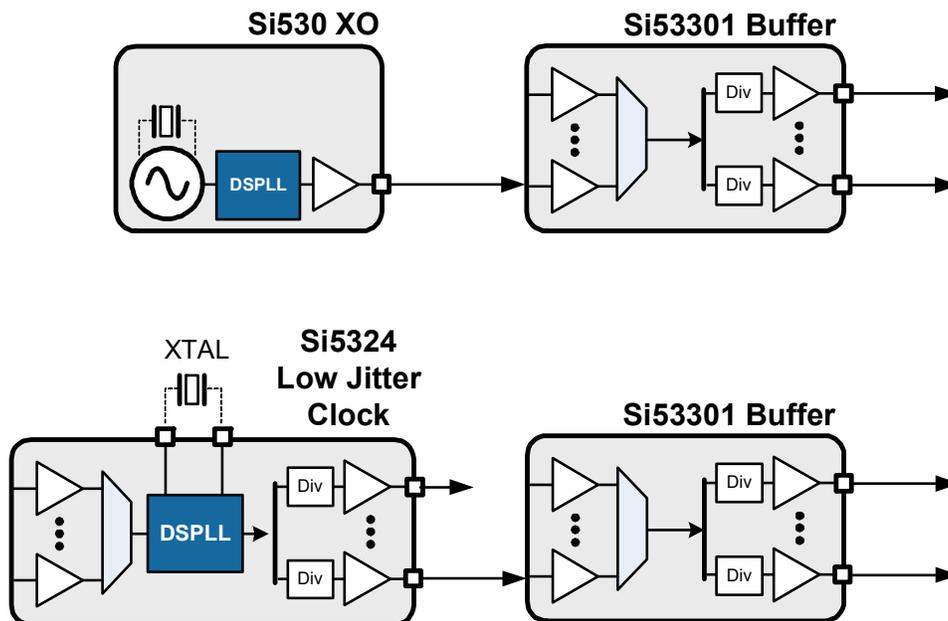
## ESTIMATING CLOCK TREE JITTER

### 1. Introduction

High speed, high performance timing applications often require a combination of XO/VCXOs, clock generators, clock buffers and jitter cleaning clocks to satisfy system timing requirements. Each component in the clock tree adds phase jitter to the starting reference clock. Care must be taken during the timing component selection process to select devices that meet system price/performance goals while providing the lowest jitter and highest system noise margin possible. The next question that arises is how to estimate the total clock jitter through the clock tree to ensure there is adequate system-level margin to reliably meet the application jitter requirements. If this jitter threshold is exceeded in high-speed SerDes applications, for example, it could have a detrimental impact on the Bit-Error Rate (BER) of the associated high-speed communications link. By ensuring jitter design targets are properly met, system timing related problems can be avoided. The application note discusses three common approaches to estimate total clock tree jitter with the focus on additive jitter when using the Si5330x clock buffer.

### 2. Jitter Generation vs. Additive Jitter

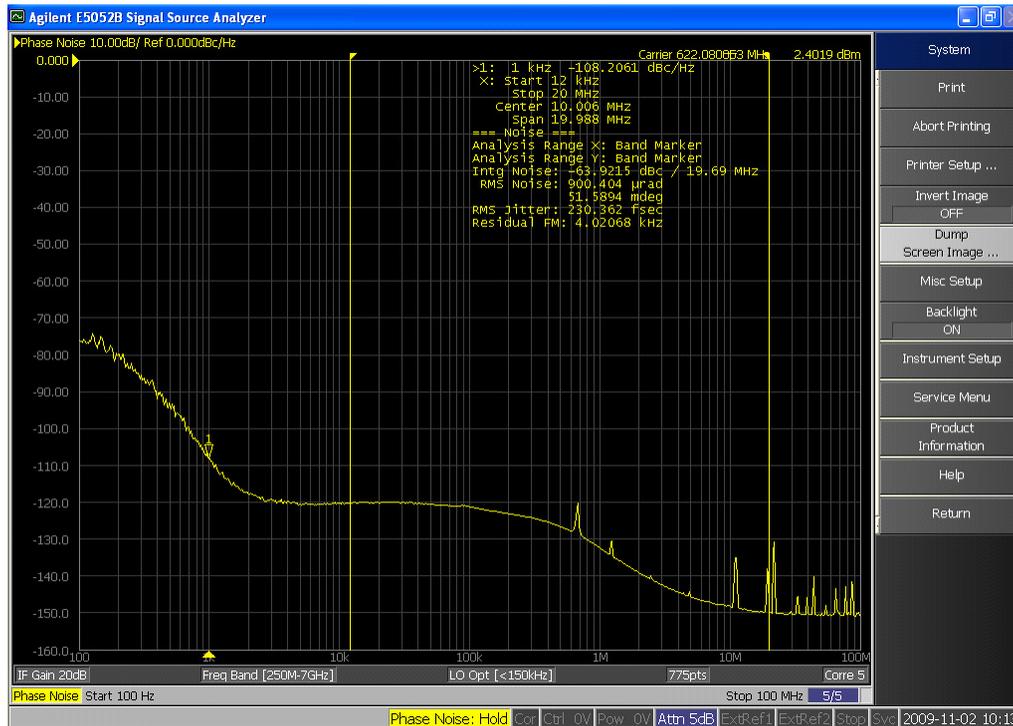
Figure 1 lists two clock tree examples. In the first case, the reference clock is generated by a low phase jitter XO (Si530). In applications where multiple copies of this frequency are required, a low jitter clock buffer (Si53301) is used to fan-out the reference clock. In the second case, a low jitter PLL-based clock generator/jitter cleaner (Si5324) is used to generate multiple output frequencies from a single reference input. If additional copies of a particular frequency are required, a low jitter clock buffer (Si53301) can be used to fan-out one frequency to multiple components with low additive jitter.



**Figure 1. Example Clock Trees: XO + Clock Buffer and Clock Generator + Clock Buffer**

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High performance XO/VCXOs and clock generators usually specify jitter in terms of phase jitter. Since this jitter is strictly a function of jitter derived from internal sources, it is called **jitter generation**. Jitter due to jitter generation can be calculated by integrating the device output clock single sideband phase noise over a predetermined offset (from carrier) frequency range. The offset frequency range, also known as integration bandwidth, is application-dependent. For example, a commonly specified integration bandwidth for many communications applications is 12 kHz to 20 MHz. Phase noise measurements are usually done using a spectrum analyzer with phase noise measurement capability or an instrument such as an Agilent E5052B Signal Source Analyzer. Figure 2 below is an example phase noise plot from an Agilent E5052B.



**Figure 2. Clock Phase Noise Plot Showing RMS Phase Jitter**

The phase noise plot in Figure 2 was taken from a clock generator providing a clock at 622.08 MHz. Note in the plot the integration bandwidth is specified at 12 kHz to 20 MHz and the calculated RMS jitter over this band is 230 fsec. The RMS jitter was calculated based on integrating the area under the phase noise curve over the 12 kHz to 20 MHz range. For details on measuring and calculating phase jitter from phase noise, please refer to *AN256 - Integrated Phase Noise*.

Low jitter clock buffers specify jitter in terms of **additive jitter**, not jitter generation. Why the difference in specification in comparison to XO/VCXOs and clock generators? Measuring phase jitter at the output of XO/VCXOs or clock generators includes the phase jitter of the clock *source* (i.e. oscillator, PLL, clock generator, etc.). For clock fan-out buffers, the clock source is the input signal which the buffer cannot control or predict. Therefore, it is not reasonable to include source, or input jitter, to the buffer's performance measurement. Additive jitter refers to the amount of phase jitter contributed by the clock buffer *only*, independent of its reference input. This means jitter specifications for clock buffers are **additive** jitter specifications and additional calculation is required to arrive at a final jitter specification for any clock tree using clock buffers. But beware, simply adding up jitter numbers from data sheets of jitter generation devices (XOs/VCXOs/clock generators/etc.) to additive jitter devices (buffers) will nearly always give erroneous and/or misleading results.

In practice there are several additional factors that must be considered when analyzing the additive jitter of a clock buffer device. These factors are summarized below:

- **Typical versus maximum additive jitter.** Buffer “typical” jitter specifications do not guarantee device performance over all conditions, including process, voltage, temperature, and frequency variation. Max additive jitter provides a more comprehensive specification inclusive of these additional factors.
- **Additive jitter specification test conditions.** The additive clock jitter of a buffer will vary depending on several variables including operating frequency, input signal amplitude, input slew rate and input rise/fall time. In general, larger signal amplitude, faster slew rates and faster input rise/fall times will enable the clock buffer IC to achieve lower additive jitter. Look for devices that fully specify additive jitter inclusive of these variables since they guarantee operation over a wider operating range.

## 3. Estimating Clock Tree Jitter Using RSS (Method 1)

One of the simplest methods for estimating total clock tree jitter of cascaded devices is to use the Root Sum Squares (RSS) method. This calculation can be performed using data sheet jitter specifications. The total jitter at the output of a cascade of clock devices can be estimated using the following equation:

$$T_j(\text{RMS}) = \sqrt{J_1^2 + J_2^2 + \dots + J_n^2}$$

Where  $T_j$  = Total RMS jitter,  $J_n$  = individual device RMS jitter.

In the following examples,  $J_{1\dots n}$  = XO or clock generator RMS phase jitter and  $J_{2\dots n}$  = clock buffer RMS additive jitter.

From Skyworks Solutions device data sheets, the maximum RMS phase jitter is as follows:

**Table 1. Data Sheet Max RMS Phase Jitter**

Device	Max RMS Phase Jitter	Jitter Type
Si530	420 fs	Jitter Generation
Si5324	410 fs	Jitter Generation
Si5330	200 fs	Additive Jitter

Using the data sheet information from Table 1 and applying the equation above, we can estimate the maximum total RMS jitter for the example Si530 + Si53301 and Si5324 + Si53301 clock trees.

For Si530 + Si53301:

$$T_j(\text{RMS}) = \sqrt{420^2 + 200^2}$$

$$T_j(\text{RMS}) = 465.2 \text{ fs}$$

For Si5324 + Si53301:

$$T_j(\text{RMS}) = \sqrt{410^2 + 200^2}$$

$$T_j(\text{RMS}) = 456.2 \text{ fs}$$

As can be seen, the resulting total RMS jitter estimates are much less than the simple sum of data sheet jitter specifications. The RSS method is recommended when a first-order, conservative approximation of clock tree jitter is required.

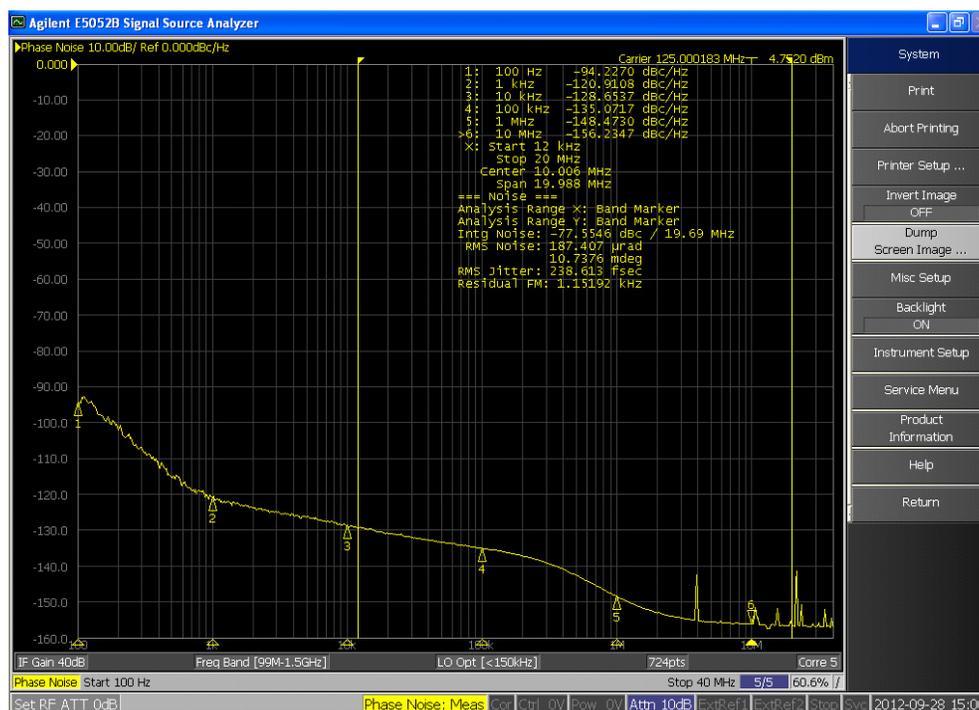
## 4. Estimating Clock Tree Jitter Using Phase Noise (Method 2)

A second more precise approach to estimating clock tree jitter through two or more timing ICs is to use device phase noise measurements for jitter generating devices in conjunction with data sheet specs for the fan-out buffer. This is a useful method when a phase noise plot of the XO/Clock Generator, typically the dominant contributor to overall clock jitter, is available. One important point to keep in mind when using phase noise plots taken at a frequency different than desired application frequency is phase noise scales with frequency. Multiplying the frequency of a clock by a factor of N increases the phase noise by  $20\log(N)$  dB. Similarly, dividing a clock frequency by N reduces phase noise by  $20\log(N)$  dB. Use this method to scale the clock phase noise measurements to match the application's target frequency. Then, integrate the phase noise over the desired integration band to calculate the RMS phase jitter of each device. Lastly, combine the RMS phase jitter of the two devices using the RSS method described above.

Example: Phase noise plot of Si530 and Si53301 data sheet spec.

Below is a phase noise plot of Si530 output at 125 MHz. Note markers are set up starting at 100 Hz and moving up in frequency decade by decade to 10 MHz. The phase noise levels at each of these frequencies can be used to calculate an estimated RMS phase jitter for this plot. This estimate can easily be done using the phase noise to jitter conversion utility found at:

<http://www.silabs.com/support/Pages/phase-noise-jitter-calculator.aspx>.



**Figure 3. Phase Noise Plot of Si530 with 125 MHz Output Clock**

Let's assume the application frequency of interest is 644.53 MHz, a common 10GbE frequency. The phase noise curve above at 125 MHz must be scaled to account for the frequency difference between the measurement's carrier frequency (125 MHz) and the desired application's frequency of 644.53 MHz. The scaling (in dB) can be calculated by the following:

$$\text{dB}(\text{corr}) = 20\log_{10} \times \frac{F_a}{F_b}$$

$$\text{dB(corr)} = 20\log_{10} \times \frac{644.53}{125}$$

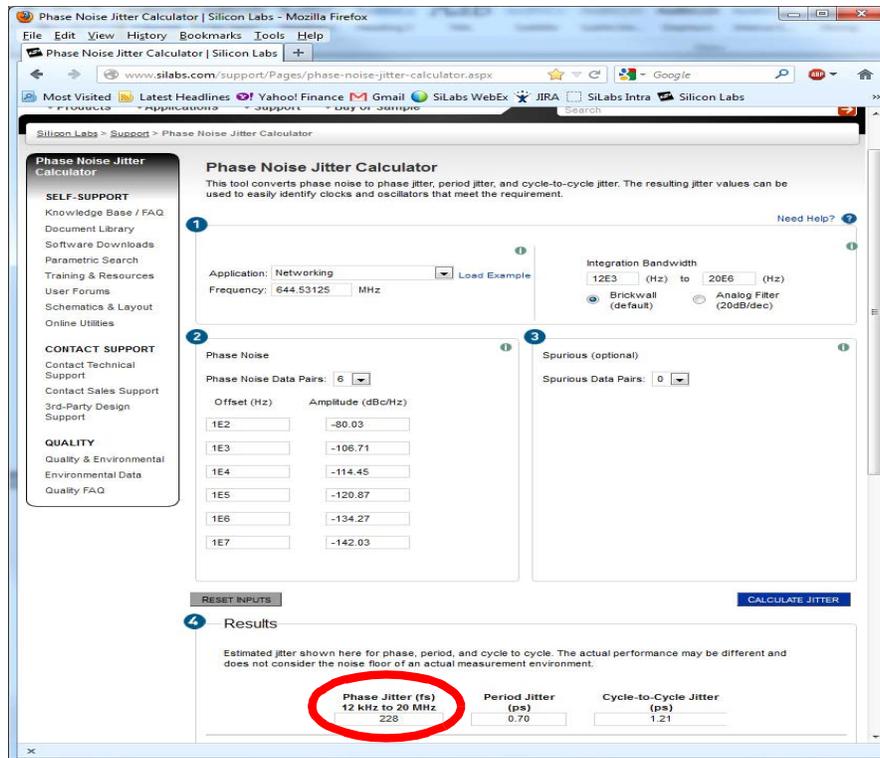
$$\text{dB(corr)} = 14.2 \text{ dB}$$

This gives new frequency adjusted phase noise points as shown in Table 2:

**Table 2. Frequency Adjusted Phase Noise of Si530 Phase Noise Plot**

Offset Frequency (Hz)	125 MHz Phase Noise (dB/Hz)	Calculated 644.53 MHz Phase Noise (dB/Hz)
100	-94.23	-80.3
1000	-120.91	-106.71
10000	-128.65	-114.45
100000	-135.07	-120.87
1000000	-148.47	-134.27
10000000	-156.23	-142.03

Use the phase noise to jitter conversion utility to convert the calculated frequency-adjusted phase noise to phase jitter, as shown in Figure 4.



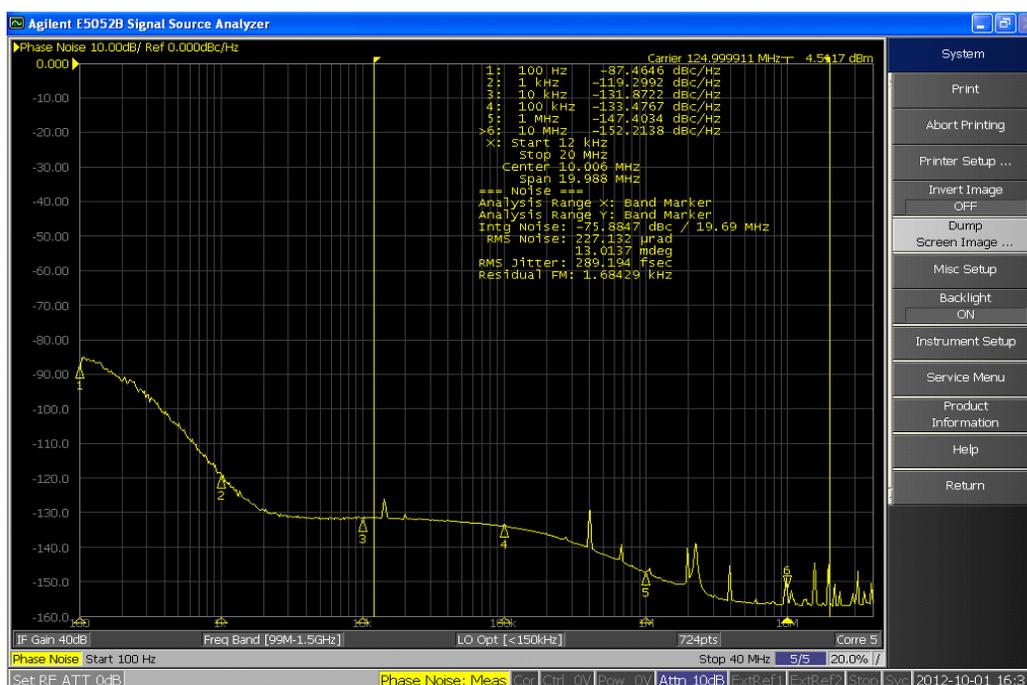
**Figure 4. Screen Capture of Phase Noise Jitter Conversion Utility**

We can now combine the Si530 XO's calculated phase jitter (288 fs) and the Si53301's data sheet additive phase jitter (200 fs) using the RSS approach:

$$T_j(\text{RMS}) = \sqrt{228^2 + 200^2}$$

$$T_j(\text{RMS}) = 303.3 \text{ fs}$$

Similarly, this same measurement, and calculation, can be done for other clock trees such as Si5324 + Si53301. Shown below is a Si5324 phase noise plot at 125 MHz and table of calculated phase noise for 644.53 MHz. The scaling factor is the same as for the previous example, 14.2 dB.

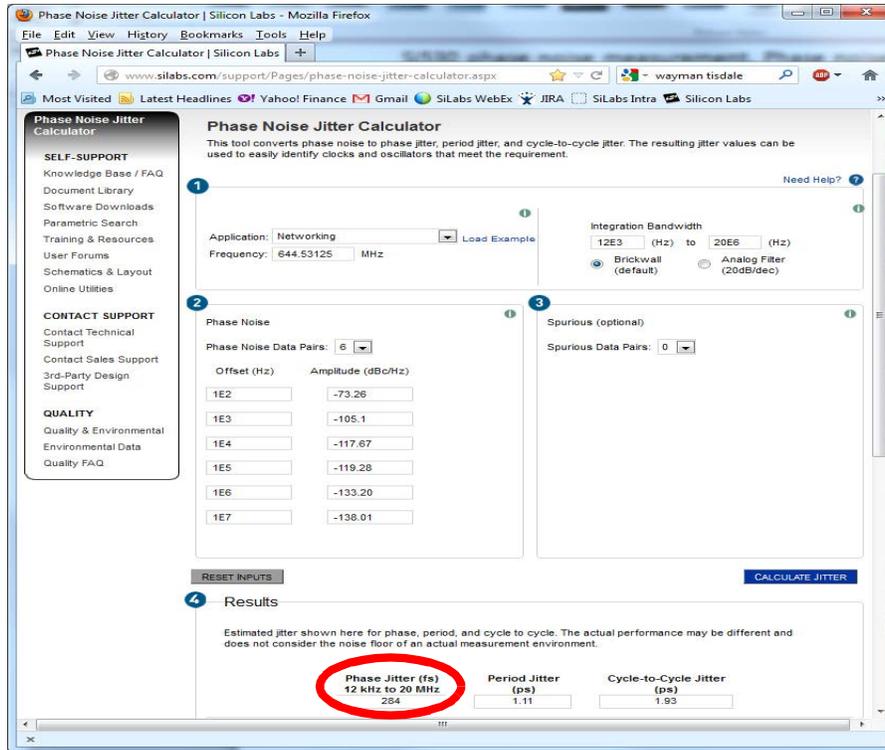


**Figure 5. Phase Noise Plot of Si5324 with 125 MHz Output Clock**

**Table 3. Frequency Adjusted Phase Noise of Si5324 Phase Noise Plot**

Offset Frequency (Hz)	125 MHz Phase Noise (dB/Hz)	Calculated 644.53 MHz Phase Noise (dB/Hz)
100	-87.46	-73.26
1000	-119.30	-105.10
10000	-131.87	-117.67
100000	-133.48	-119.28
1000000	-147.40	-133.20
10000000	-152.21	-138.01

Use the Phase Noise to Jitter Conversion Utility to convert the calculated frequency-adjusted phase noise to phase jitter.



**Figure 6. Screen Capture of Phase Noise Jitter Conversion Utility**

We can now combine the Si5324 Clock Generator’s calculated phase jitter (284 fs) and the Si53301’s data sheet additive phase jitter (200 fs) using the RSS approach:

$$T_j(\text{RMS}) = \sqrt{284^2 + 200^2}$$

$$T_j(\text{RMS}) = 347.4 \text{ fs}$$

Method 2 jitter estimates are more precise than Method 1 estimates because Method 2 estimates are based on actual Si530 and Si5324 phase noise measurements. Phase noise measurements provide an accurate representation of typical device performance for a given frequency, whereas a data sheet’s maximum jitter specification is a statistical maximum based on a larger number of variables. The phase noise method (Method 2) is recommended when a more precise clock tree jitter estimate is required.

## 5. Direct Clock Tree Jitter Measurement Using Device Evaluation Boards (Method 3)

A third approach is to directly measure the clock tree jitter using evaluation board (EVB) measurements. Using this approach, SMA cables can be used to connect the output from the XO/clock generator EVB to the input of the clock buffer EVB. This measurement can be performed using time domain test equipment (e.g. oscilloscope) or frequency domain test equipment (e.g., spectrum analyzer). Modern oscilloscopes include FFT processing to provide frequency domain information that can be integrated over the target frequency band to calculate a RMS jitter value. However, the noise floor of these solutions is not sufficiently low enough to yield accurate results for ultra-low jitter clock trees (<0.5 ps RMS).

For the most accurate results, the total device jitter at the output of the clock buffer EVB should be measured using a spectrum analyzer with a very low phase noise floor, such as the Agilent E5052B.

Figure 7 shows the measured phase noise of the Si530+Si53301 and Figure 8 shows the measured phase noise of the Si5324+Si53301 using this direct measurement technique. This method provides the most precise estimate for clock tree jitter.

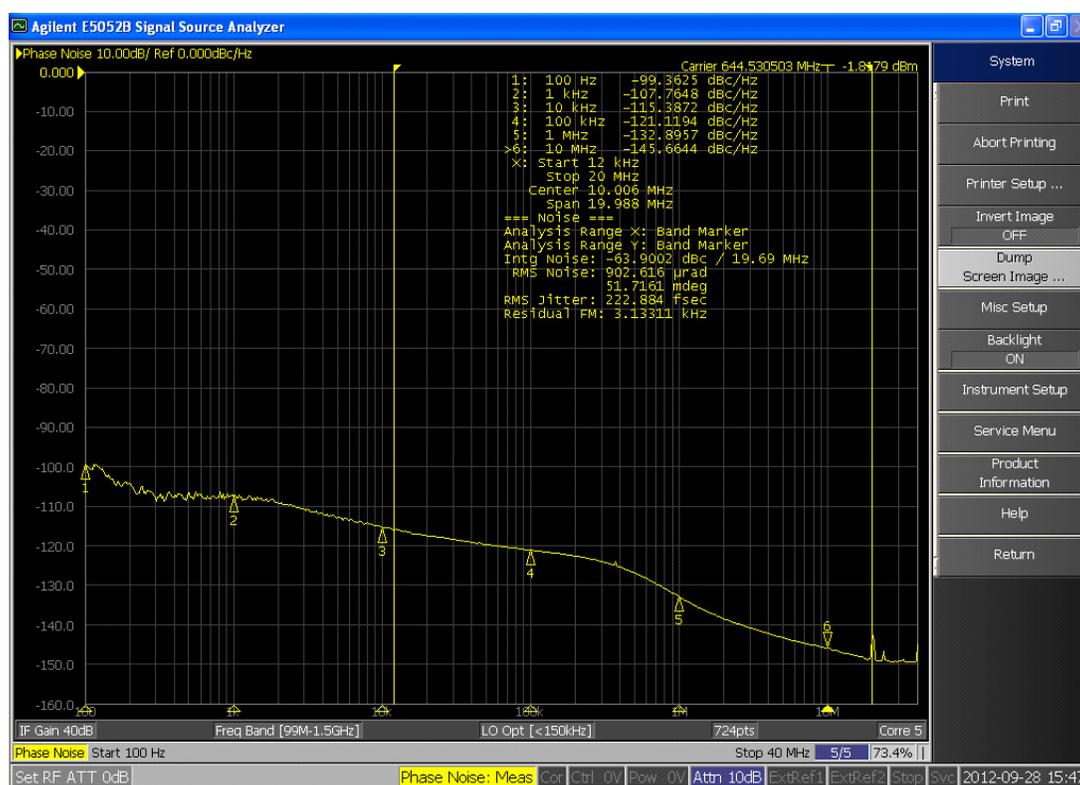


Figure 7. Direct Phase Noise Measurement of Si530 + Si53301 with 644.53 MHz Output Clock

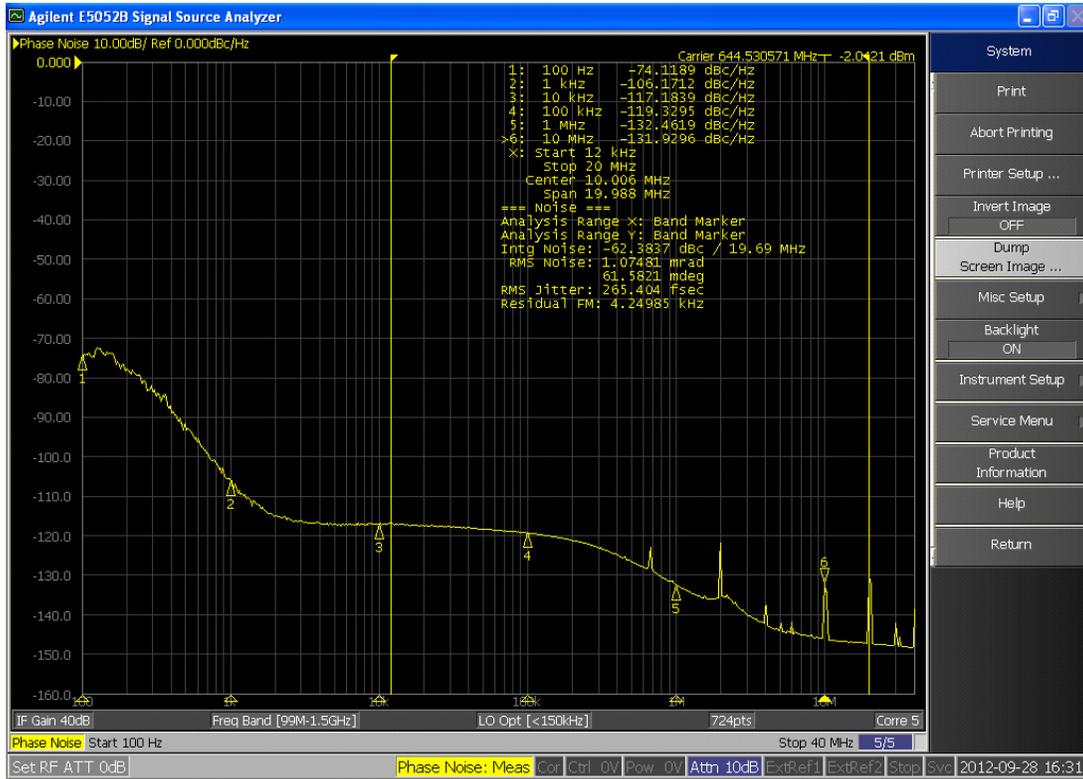


Figure 8. Direct Phase Noise Measurement of Si5324 + Si53301 with 644.53 MHz Output Clock

## 6. Summary

Three different techniques are available to estimate the total clock jitter through two common clock tree topologies: XO + clock buffer and clock generator + clock buffer. The results are summarized in the tables below.

**Table 4. Summary Results of XO + Clock Buffer for all 3 Jitter Estimation Methods**

Method	XO + Clock Buffer (Si5324 + Si53301)	RMS Phase Jitter (12 kHz to 20 MHz)
1	Jitter RSS estimate	465.2 fs
2	Phase noise plot estimate	303.3 fs
3	Direct EVB measurement	222.9 fs

**Table 5. Summary Results of Clock Generator + Clock Buffer for all 3 Jitter Estimation Methods**

Method	Clock Generator + Clock Buffer (Si5324 + Si53301)	RMS Phase Jitter (12 kHz to 20 MHz)
1	Jitter RSS estimate	456.2 fs
2	Phase noise plot estimate	347.4 fs
3	Direct EVB measurement	265.4 fs

As expected, Method 1 provides the most conservative jitter estimate by using specified data sheet maximum RMS jitter values combined using the RSS technique. Method 2 is useful when phase noise plots or phase noise data is available, but is specified at a different frequency than the application in question requires. Method 3 gives direct and more precise application-specific jitter estimation.

## DOCUMENT CHANGE LIST

### Revision 0.9 to Revision 0.91

- Corrected Table 5 typographical error.



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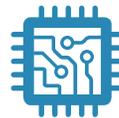
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