AN970: Design Guide for PLC Digital Input Modules Using the Si838x

This application note serves as a design guide for selecting an input resistor network for the Si838x that is robust in regards to part and resistor tolerances. Also discussed are methods of selecting input resistor values to adhere to off, on, and transition region requirements, such as those in IEC 61131-2. The input network serves to map the input thresholds of the Si838x to the system-level current and voltage thresholds (e.g. 24 V dc signals).

The Si838x product family is a set of eight-channel isolators that utilize LED emulator inputs to drive the isolation channel. Depending on the product, the inputs of the Si838x can be read as either parallel digital output signals or as serial data on an SPI bus. SPI products also support daisy-chaining multiple units for quicker access. More information is available in the ordering guide of the Si838x data sheet.

In order to comply with the IEC 61131-2 standard for Programmable Logic Controller (PLC) Digital Input Modules, the Si838x LED emulator inputs are combined with a two-resistor input network and an LED indicator light. This application note provides a system of equations and guidance for selecting the bill of materials to meet system requirements, such as those defined in IEC 61131-2.

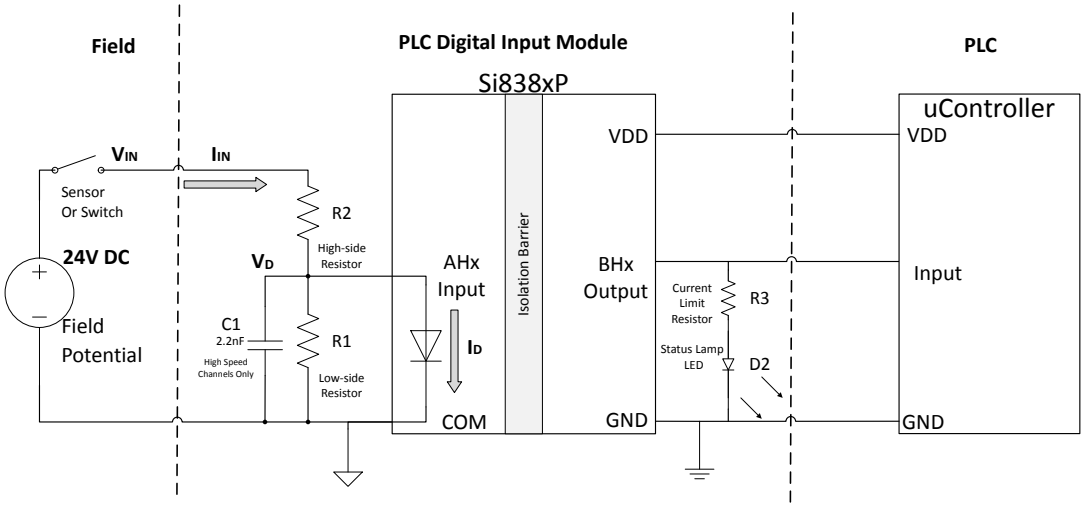
Note that the inputs of the Si838x are bipolar and can be used as either sinking or sourcing inputs. This design guide focuses on the sinking configuration; however, the same practices apply to sourcing configurations.

The figure below illustrates a single high-speed channel in an Si838xP PLC digital input module in a 24 V system. C1 improves Common-Mode Transient Immunity (CMTI) performance on high-speed channels and does not affect the selection of R1, R2, or R3.

Shown below is a single Si838xP channel configured as PLC input module in a 24 V dc system:

KEY POINTS

- Si838x Input Networks
- Input Hysteresis
- System Transition Values
- Example Design
- Resistor Tolerance
- IEC 61131-2 Recommendations



1. Complete Si838xP System Schematic

Each channel on the Si838x requires its own input network and indicator LED as shown in the example schematic below.

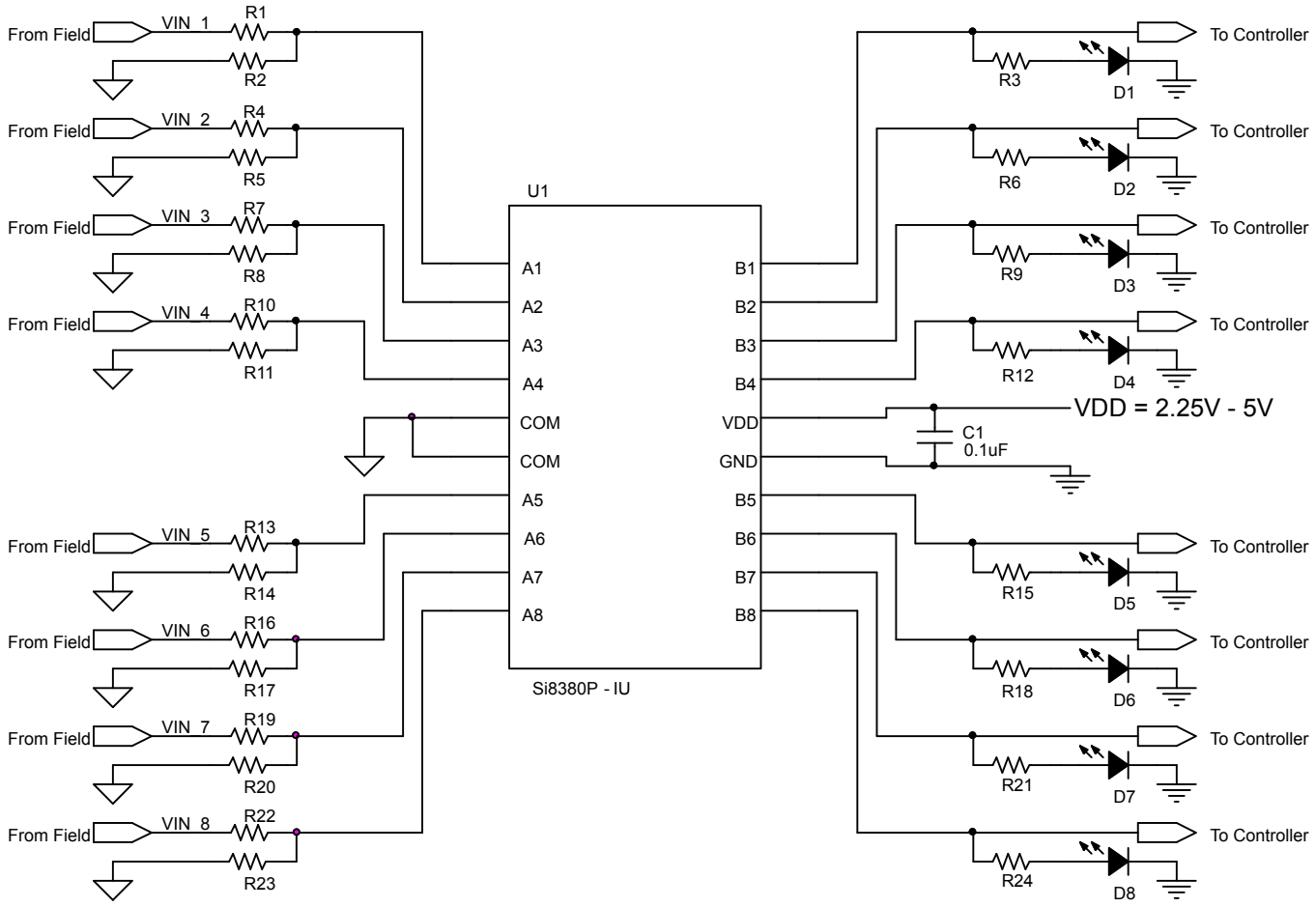


Figure 1.1. Si8380P Configured as a PLC Digital Input Module

2. Si838x Transitions and Thresholds

2.1 Understanding Si838x Transitions

The Si838x detects a HIGH condition when both the input current and input voltage are above their respective thresholds per the Si838x data sheet. Further, the Si838x has built-in hysteresis around its input threshold, meaning that the point on the input I-V curve at which the output will transition from LOW to HIGH is different from the point on the input I-V curve at which the output transitions from HIGH to LOW. The figure below illustrates this point.

The input threshold values for the Si838x are given in Table 4.2 of the data sheet.

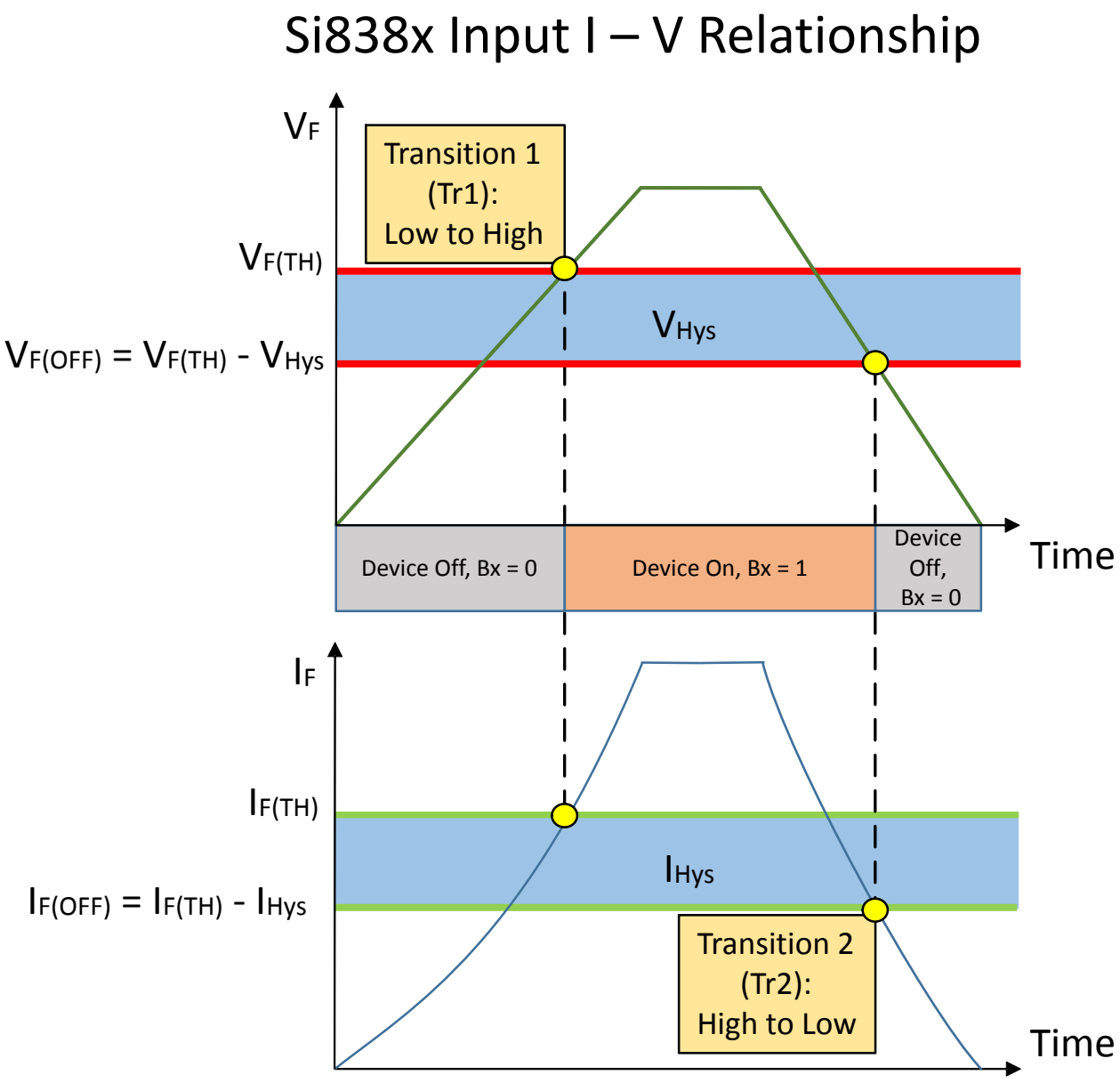


Figure 2.1. Illustration of Input Hysteresis for the Si838x and the Definitions $I_{F(OFF)}$ and $V_{F(OFF)}$

2.2 Input Threshold Tolerance

The Si838x LED emulator inputs are tuned according to a target load-line, and, for that reason, the worst-case tolerances for both current and voltage thresholds will not occur simultaneously. Thus, transition threshold tolerances are bounded by lines parallel to the target load-line at the chip-level input I-V space. These lines will be referred to as the low-side and high-side tolerance load lines. Moreover, the input threshold minima and maxima from the Si838x data sheet can be superimposed atop the I-V space as a box. Since the tolerance load lines more tightly restrict the input I-V space, some corners of the box represent invalid threshold pairs. This additional restriction at the inputs of the Si838x is important because, as is discussed later, it translates to a larger design region for the input resistor network.

The following table describes the load lines where $I_{F(TH)}$ (the input current threshold) is the dependent variable and $V_{F(TH)}$ (the input voltage threshold) is the independent variable.

Table 2.1. Load Line Equations

Load Line	Equation
Low-Side Tolerance	$I_{F(TH)}(mA) = -3.6 \times V_{F(TH)} + 5.0$
Target	$I_{F(TH)}(mA) = -3.6 \times V_{F(TH)} + 5.6$
High-Side Tolerance	$I_{F(TH)}(mA) = -3.6 \times V_{F(TH)} + 6.1$

The figure below illustrates the lines above and their intersection with the bounding box, providing two maxima and two minima to be considered when designing the input network later in this application note.

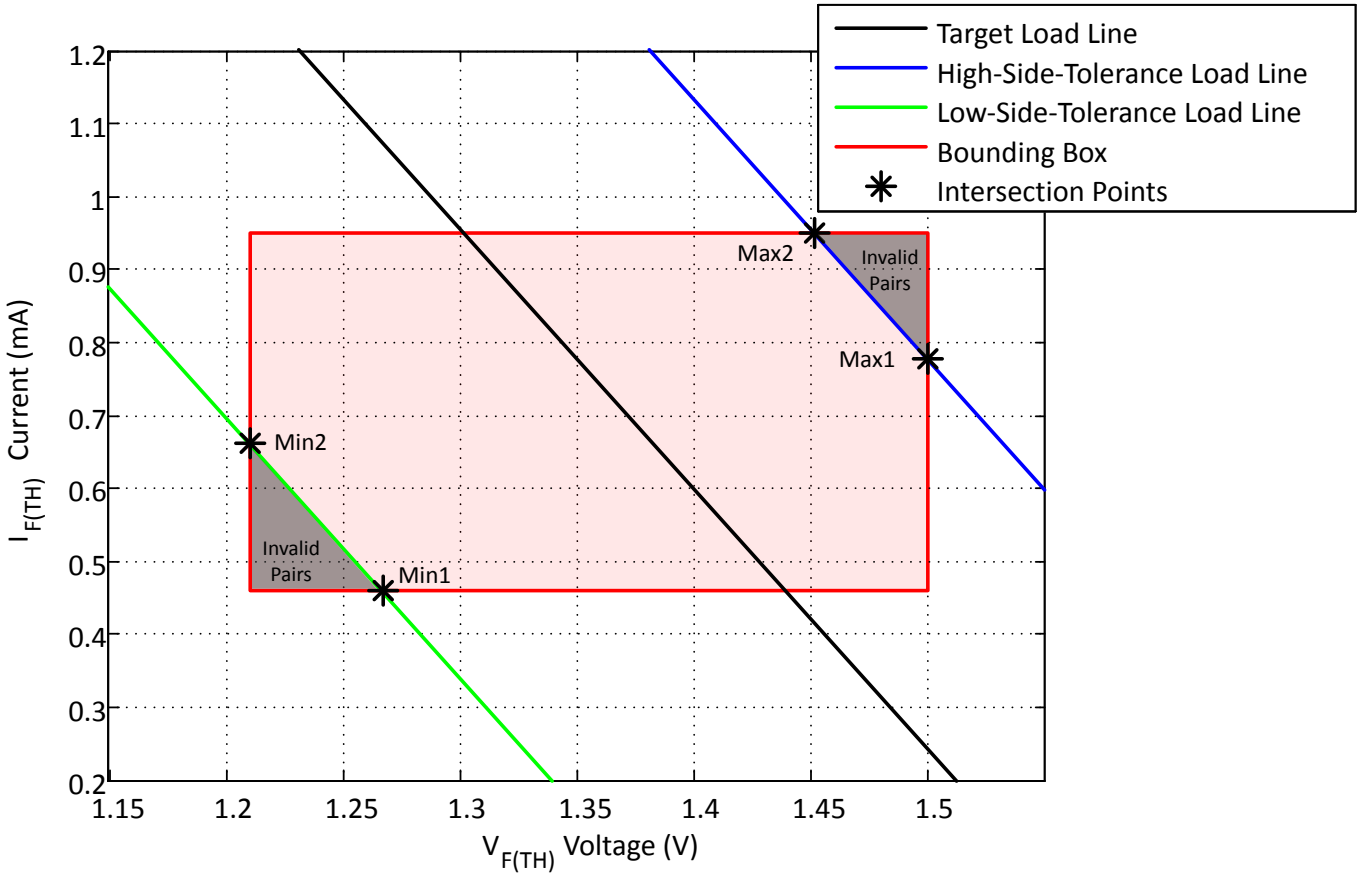


Figure 2.2. Threshold Tolerance Load Lines and Bounding Box from Si838x Data Sheet Values

The intersection for the tolerance load lines with the bounding box provides the following minima and maxima:

Table 2.2. Maxima and Minima Threshold Value Pairs

Point Name	$V_{F(TH)}$ (V)	$I_{F(TH)}$ (mA)
Min1	1.27	0.46
Min2	1.21	0.66
Max1	1.5	0.77
Max2	1.45	0.95

3. Governing Equations for System Transitions

The purpose of the input network is to map the Si838x's transitions (Tr1 and Tr2 in Figure 2.1 Illustration of Input Hysteresis for the Si838x and the Definitions $I_{F(OFF)}$ and $V_{F(OFF)}$ on page 3) to the system's requirements on a per-channel basis. The front page figure provides an example of a correctly configured input network. This system is modeled by the following equations, put in terms of data sheet specifications and resistances:

$$I_{IN} = I_F + I_{R_1} = I_F + \frac{V_F}{R_1}$$

Equation 1.

$$V_{IN} = V_F + V_{R_2} = V_F + I_{IN} \times R_2 = V_F + R_2 \times (I_F + \frac{V_F}{R_1})$$

Equation 2.

The Si838x should not be modeled by a traditional diode equation; however, we can use its transition points to provide the following constraints:

$$\text{At Tr1: } V_F = V_{F(TH)}, I_F = I_{F(TH)}$$

Equation 3.

$$\text{At Tr2: } V_F = V_{F(OFF)}, I_F = I_{F(OFF)}$$

Where, recalling Figure 2.1 Illustration of Input Hysteresis for the Si838x and the Definitions $I_{F(OFF)}$ and $V_{F(OFF)}$ on page 3:

$$V_{F(OFF)} = V_{F(TH)} - V_{HYS}, I_{F(OFF)} = I_{F(TH)} - I_{HYS}$$

Equation 4.

Let the points in the system-level I-V space (I_{IN}, V_{IN}) corresponding to the Si838x's Tr1 and Tr2, be addressed as TR1 and TR2, respectively. The following figure shows a linear approximation of the system curve leading to and from the transition points.

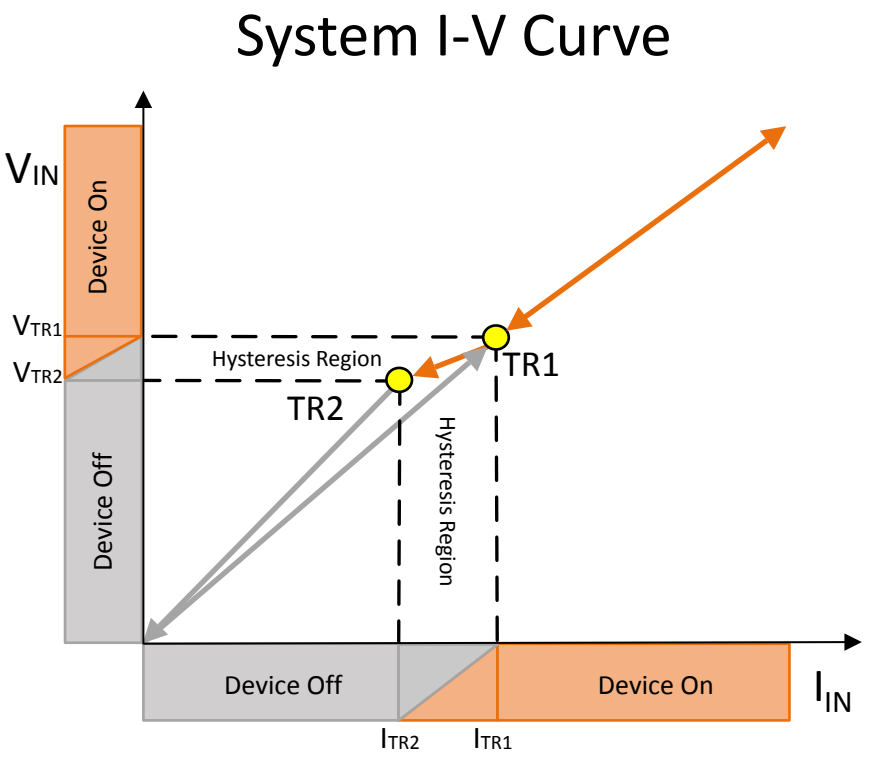


Figure 3.1. System-Level Transition Points and the Hysteresis Region

Then, using Equation 1 and Equation 2 in conjunction with Equation 3 and Equation 4, system-level transitions become defined by:

$$\text{a. } I_{TR1} = I_{F(TH)} + \frac{V_{F(TH)}}{R_1} = \frac{V_{TR1} - V_{F(TH)}}{R_2}$$

$$\text{b. } V_{TR1} = V_{F(TH)} + R_2 \times I_{TR1} = V_{F(TH)} + R_2 \times (I_{F(TH)} + \frac{V_{F(TH)}}{R_1})$$

Equation 5. TR1

$$\text{a. } I_{TR2} = I_{F(OFF)} + \frac{V_{F(OFF)}}{R_1} = \frac{V_{TR2} - V_{F(OFF)}}{R_2}$$

$$\text{b. } V_{TR2} = V_{F(OFF)} + R_2 \times I_{TR2} = V_{F(OFF)} + R_2 \times (I_{F(OFF)} + \frac{V_{F(OFF)}}{R_1})$$

Equation 6. TR2

Finally, through Equations 4, 5, and 6, TR1 and TR2 can be related with the following equations:

$$\text{a. } I_{TR2} = I_{TR1} - (I_{HYS} + \frac{V_{HYS}}{R_1})$$

$$\text{b. } V_{TR2} = V_{TR1} - (V_{HYS} + R_2 \times (I_{HYS} + \frac{V_{HYS}}{R_1}))$$

Equation 7. Relating TR1 and TR2

4. Design Equations and Operational Regions

Designing a network from scratch requires defining the system's transition and logical regions. The transition region is the region in which the module is allowed to transition from an output LOW to an output HIGH and vice-versa. The HIGH and LOW regions are those regions in which the output is guaranteed to be HIGH or LOW, respectively.

The system's design equations derive most of their constraints from the boundaries of the transition region. Remaining constraints for IEC 61131-2 systems come as a mandate to operate within one of the three defined regions at all times. A rearrangement of Equations 5 and 6, such that they are bounded by these regions, provides a set of design equations for the system.

4.1 Transition and Logical Regions

A transition region can be reduced to a rectangle in the system-level I-V space (I_{IN}, V_{IN}) whose bounds are a given by a minimum and maximum I_{IN} and V_{IN}. The following table enumerates one such example transition region.

Table 4.1. Example of Transitional Regional Boundaries

	Transition Region Boundaries			
	V_{IN} (V)		I_{IN}(mA)	
	Symbol	Value	Symbol	Value
Max	V_{TR_MAX}	15	I_{TR_MAX}	15
Min	V_{TR_MIN}	5	I_{TR_MIN}	0.5

Moreover, per the specification, the module should unambiguously output either a LOW or HIGH outside the transition area. This further defines the system level I-V space (I_{IN}, V_{IN}) such that a LOW region and HIGH region become clear as illustrated in the following table and figure.

Table 4.2. Example of Completely-Defined Regional Boundaries

	LOW (Off) Region				Transition Region				HIGH (On) Region			
	$V_{IN\ (V)}$		$I_{IN\ (mA)}$		$V_{IN\ (V)}$		$I_{IN\ (mA)}$		$V_{IN\ (V)}$		$I_{IN\ (mA)}$	
	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
Max	V_{LOW_MAX}	15, 5	I_{LOW_MAX}	15	V_{TR_MAX}	15	I_{TR_MAX}	15	V_{HIGH_MAX}	30	I_{HIGH_MAX}	15
Min	V_{LOW_MIN}	0	I_{LOW_MIN}	0	V_{TR_MIN}	5	I_{TR_MIN}	0.5	V_{HIGH_MIN}	15	I_{HIGH_MIN}	2

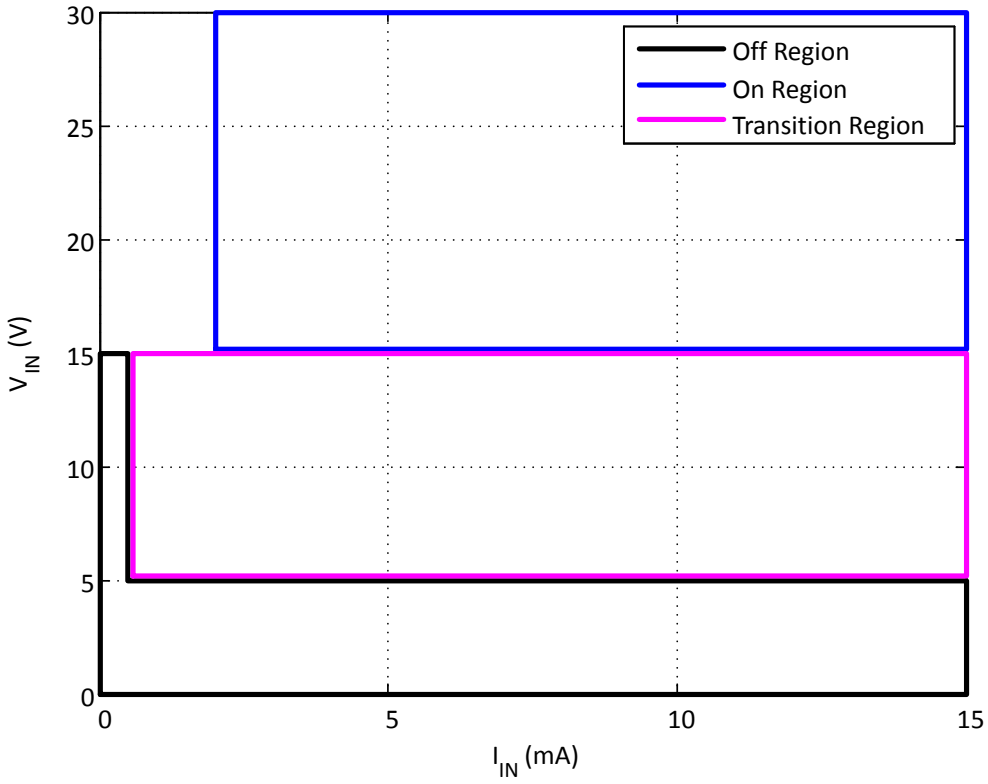


Figure 4.1. Regional Boundary Data Drawn over System-Level I-V Space

4.2 Resistor Equations

The first step towards refactoring Equations 5 and 6 is to relate them to the values in Table 4.1 Example of Transitional Regional Boundaries on page 8, which produces the following equations (where $I_{TR2} \leq I_{TR1}$ and $V_{TR2} \leq V_{TR1}$):

From Equation 5, we have:

$$\text{a. } I_{TR\_MAX} \geq I_{TR1} = I_{F(TH)} + \frac{V_{F(TH)}}{R_1}$$

$$\text{b. } V_{TR\_MAX} \geq V_{TR1} = V_{F(TH)} + R_2 \times (I_{F(TH)} + \frac{V_{F(TH)}}{R_1})$$

Equation 8. Maxima

From Equations 6 and 7, we have:

$$\text{a. } I_{TR\_MIN} \leq I_{TR2} = I_{F(OFF)} + \frac{V_{F(OFF)}}{R_1}$$

$$\text{b. } V_{TR\_MIN} \leq V_{TR2} = V_{F(OFF)} + R_2 \times (I_{F(OFF)} + \frac{V_{F(OFF)}}{R_1})$$

Equation 9. Minima

Solving in terms of R2 and R1 produces:

$$\text{a. } (\frac{V_{F(TH)}}{I_{TR\_MAX} - I_{F(TH)}}) \leq R_1 \leq (\frac{V_{F(OFF)}}{I_{TR\_MIN} - I_{F(OFF)}}), I_{F(OFF)} < I_{TR\_MIN} \text{ and } I_{F(TH)} < I_{TR\_MAX}$$

$$\text{b. } (\frac{V_{TR\_MIN} - V_{F(OFF)}}{I_{F(OFF)} + \frac{V_{F(OFF)}}{R_1}}) \leq R_2 \leq (\frac{V_{TR\_MAX} - V_{F(TH)}}{I_{F(TH)} + \frac{V_{F(TH)}}{R_1}}), \text{ for a given R1}$$

Alternatively, if R2 is set by other constraints, (b) can be arranged as:

$$\text{c. } (\frac{R_2 \times V_{F(TH)}}{V_{TR\_MAX} - V_{F(TH)} - R_2 \times I_{F(TH)}}) \leq R_1 \leq (\frac{R_2 \times V_{F(OFF)}}{V_{TR\_MIN} - V_{F(OFF)} - R_2 \times I_{F(OFF)}}), \text{ for a given R2 and positive denominator}$$

Equation 10. Resistance Boundaries

R1 and R2 should be selected to meet system power requirements, with the general guideline to minimize power and thus maximize the value of R1 and minimize the value of R2, which is discussed later in this section.

4.3 Regions of Inoperability and the Ideal Diode Model

To comply with the IEC 61131-2 specification, the input network must be designed such that the system never operates outside of the three defined regions. To make this guarantee, consider an ideal diode model in which the input voltage is constant once it is above the threshold and the input current is allowed to vary. This model underestimates the input current for a given system voltage and enables a linear approximation for the system level transition curve above TR1, as depicted in Figure 5.1 Example Design I-V Space with Transition Points TR1 and TR2 Displayed per Design Corner on page 14.

$$I_{IN} \geq \frac{V_{IN} - V_{F(TH)}}{R_2} \geq I_{HIGH\_MIN}$$

Equation 11. Input Current Constraints on Ideal Diode Model

From Equations 10 and 11 and Table 4.2 Example of Completely-Defined Regional Boundaries on page 8, R2 becomes constrained according to the lowest corner of the HIGH region:

$$(\frac{V_{TR\_MIN} - V_{F(OFF)}}{I_{F(OFF)} + \frac{V_{F(OFF)}}{R_1}}) \leq R_2 \leq \min((\frac{V_{TR\_MAX} - V_{F(TH)}}{I_{F(TH)} + \frac{V_{F(TH)}}{R_1}}), \frac{V_{HIGH\_MIN} - V_{F(TH)}}{I_{HIGH\_MIN}}), \text{ for a given R1}$$

Equation 12. Final R2 Boundaries

4.4 Power Considerations

After calculating the boundaries for R1 and R2, there can be multiple value pairs, in a given resistor series, that provide a solution. That set of solutions can be further reduced by selecting R1 and R2 values such that power is optimized.

Where the system power is described in the following by substituting Equation 1:

$$P_{IN} = V_{IN} \times I_{IN} = (V_F + R_2 \times (I_F + \frac{V_F}{R_1})) \times (I_F + \frac{V_F}{R_1}) = V_F \times (I_F + \frac{V_F}{R_1}) + R_2 \times (I_F + \frac{V_F}{R_1})^2$$

Equation 13.

It is clear from the equation bove that power is proportional to R2 and inversely proportional to R1. Thus, an input network that maximizes R1 and minimizes R2 in the set of solution pairs will be power-optimized across all operational regions.

5. Design Example—Working with Tolerances

This section provides guidance for designing an input network which is robust to resistor mismatch and Si838x input tolerances by incorporating those conditions into the process. Consider the design requirements listed in the following table.

Table 5.1. Example Design Requirements

Requirement Number	Description	Value
1	Input Signal Magnitude	24 V dc (30 V dc max)
2	Input LOW voltage	$V_{IN} \leq 5$ V
3	Input HIGH voltage	$V_{IN} \geq 19$ V
4	Resistors Series	E24 – 5% tolerance
5	Input HIGH current	$I_{IN} \geq 3$ mA

5.1 Transition Region and Requirements

Turning the above requirements into on/off/transitions regions can be done simply by applying the boundaries in Table 4.2 Example of Completely-Defined Regional Boundaries on page 8 to the requirements above. Examining the minima and maxima in the respective tables shows this to be a conservative design choice. Further, the mismatch scenarios created by Requirement 4 in the table above and combined with the Si838x input tolerances provide the fringe conditions in which the network must operate.

5.2 Resistor Calculations

Table 5.2. Si838x Data Sheet Specifications Relevant to Transition Points and Input Network Design

Si838x Data Sheet Specifications				
	Min	Typ	Max	Units
$V_{F(TH)}$	1.21	1.38	1.5	(V)
V_{HYS}	0.03	0.073	0.13	(V)
$I_{F(TH)}$	0.46	0.606	0.95	(mA)
I_{HYS}	0.03	0.076	0.2	(mA)

The design corners to be considered are shown in the following table:

Table 5.3. Design Corners Definition

Design Corners						
Corner Symbol (TR1–TR2)	Point	Data Sheet Value				Corner Definition
		$V_{F(ON)}$	V_{HYS}	$I_{F(TH)}$	I_{HYS}	
Min–Min	Min1	Min	Max	Min	Max	Minimizes TR2 via $V_{F(OFF)}$ and $I_{F(OFF)}$
	Min2					
T–T	Typical	Typical	Typical	Typical	Typical	Typical Behavior
Max–Max	Max1	Max	Min	Max	Min	Maximizes TR1 via $V_{F(TH)}$ and $I_{F(TH)}$
	Max2					

Designing an input network to accommodate these design corners will ensure a robust design against all other possibilities.

Applying Equation 4 to Table 5.2 Si838x Data Sheet Specifications Relevant to Transition Points and Input Network Design on page 12 produces the $V_{F(OFF)}$ and $I_{F(OFF)}$ values listed in the following table, describing transition point Tr2 for each corner.

Table 5.4. Calculated Tr2 Values for Specified Design Corners

Corner	Point	$V_{F(OFF)}$ (V) $V_{F(OFF)} = V_{F(TH)} - V_{HYS}$	$I_{F(OFF)}$ (mA) $I_{F(OFF)} = I_{F(TH)} - I_{HYS}$
Min–Min	Min1	1.14	0.26
	Min2	1.08	0.46
T–T	Typical	1.307	0.53
Max–Max	Max1	1.47	0.74
	Max2	1.42	0.92

Solving Equation 10a for R1 produces the following table. The design range for R1 is defined as the range between the largest minimum-R1 value and the smallest maximum-R1 value.

Table 5.5. R1 Boundaries and Design Range Rounded to the Nearest Integer

Corner Symbol	Point	R1 (Ω)	
		Minimum	Maximum
Min–Min	Min1	88	4750
	Min2	85	27000
T–T	Typical	96	—
Max–Max	Max1	106	—
	Max2	104	—
R1 Design Range		106	4750

Based on the design range in the preceding table and the approach to power optimization in 4.4 Power Considerations, it should follow that an R1 with a value of 4300 Ω would fit the design, as worst case resistor tolerances are still within the design range. However, solving Equation 12 with R1 = 1.05 x 4300 provides no solution for R2 in the E24 series. Iteratively reducing the R1 value and applying Equation 12 provides R1 = 2700 as the largest value for which an R2 can be selected from the E24 series. Applying that analysis to the Design Corners produces the following table. Note that evaluating R1 x 0.95 is not shown because it is not the minimum value in Equation 12. Again, the design range for R2 is defined as the range between the largest minimum-R2 value and the smallest maximum-R2 value.

Table 5.6. R2 Boundaries and Design Range Rounded to the Nearest Integer

Corner Symbol	Point	R2 (Ω) – When R1 = 2700 Ω	
		Minimum (Using 1.05 x R1)	Maximum
Min–Min	Min1	5830	6865
	Min2	4662	6895
T–T	Typical	3727	6810
Max–Max	Max1	2805	6750
	Max2	2520	6775
R2 Design Range		5830	6750

The obvious candidate is R2 = 6200 Ω. This checks out since 5% variation from 6800 Ω is within design range for R2, and the preceding table already incorporates the worst-case R1 tolerances. Thus, the most energy-efficient solution (per 4.4 Power Considerations) that satisfies the design requirements listed in Table 5.1 Example Design Requirements on page 12 is R1 = 2700 Ω and R2 = 6200 Ω.

5.3 Design Check

Applying Equations 5 and 6 to the previously calculated E24 values of R1 and R2 produces the nominal transition values for TR1 and TR2 for each design corner, as shown in the table below. Since worst case resistor tolerances were used to constrain R1 and R2, the values below encompass those found in all resistor mismatch scenarios. All values are within the transition region, confirming that the R1, R2 network meets the requirements.

Table 5.7. Nominal Transition Values for the Example Design with Si838x Tolerances

Transition Values (R1 = 2700 Ω, R2 = 6200 Ω)					
Corner Symbol	Point	I_{TR1} (mA)	V_{TR1} (V)	I_{TR2} (mA)	V_{TR2} (V)
Min–Min	Min1	0.93	7.04	0.68	5.37
	Min2	1.11	8.08	0.86	6.41
T–T	Typical	1.12	8.31	1.01	7.59
Max–Max	Max1	1.33	9.72	1.28	9.43
	Max2	1.49	10.67	1.45	10.38

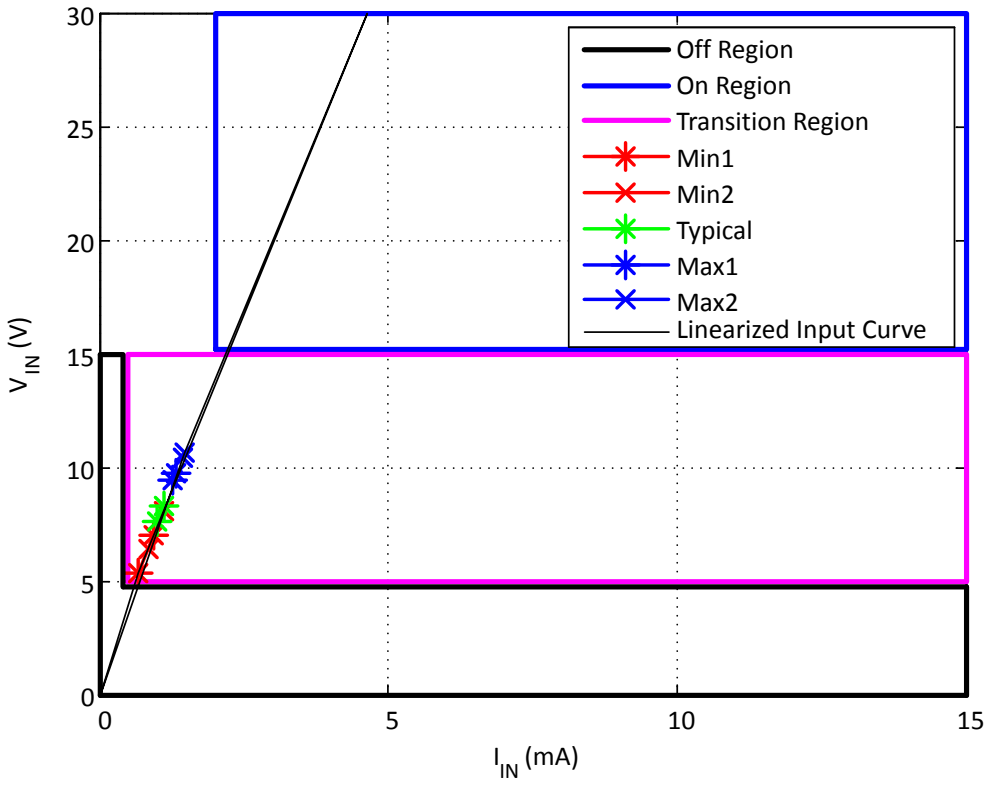


Figure 5.1. Example Design I-V Space with Transition Points TR1 and TR2 Displayed per Design Corner

6. Indicator LEDs

Finally, IEC61131-2 compliant PLC digital input modules require a lamp that indicates when the input signal is in the ON region. Si838xP parts can either have the indication LEDs in parallel with the input network, as seen in Figure 6.1 Parallel Output System Configuration for IEC61131-2 Adherence on page 15, or on the output channels in parallel with the controller inputs, as shown in the front page figure. Conversely, Si838xS parts have SPI outputs and thus can only support indicator LEDs in parallel with the input network, as seen in Figure 6.1 Parallel Output System Configuration for IEC61131-2 Adherence on page 15.

6.1 Parallel Output LEDs (Si838xP)

The Si838xP output channels are capable of driving an LED and resistor directly, per the datasheet values. Given the wide operational voltage of VDD on the output side, 2.5 V to 5.0 V, it is recommended to choose LEDs with lower threshold voltages than the VDD rail. Following from the front page figure, R3 should be sized according to the Si838xP limitations and the desired luminosity for a given LED according to the following equation:

$$I_{F\_D2} = \frac{V_{OUT\_HIGH} - V_{F\_D2}}{R_3}$$

Equation 14. Output Indicator LED Equation

6.2 Parallel Input LEDs (Si838xS or Si838xP)

Placing a LED in parallel with the input network on a per channel basis is the recommended solution for serial output parts or in systems requiring large amounts of LED current for luminosity purposes. It should also be noted that the additional current drawn by the LED at a given V_{IN} moves the system input I-V curve further along the current axis. This means an input network designed for IEC61131-2 will remain within the specifications after an LED and corresponding resistor are placed in parallel with the input network. The design requirement in this configuration is to size R3 and R4 such that the LED turns on inside of the transition region of the input I-V space (I_{IN}, V_{IN}):

$$V_{TR\_MIN} \leq V_{F\_D2} \times (1 + \frac{R_3}{R_4}) \leq V_{TR\_MAX}$$

Equation 15. Input Indicator LED Equation

Where forward current is controlled according to luminosity and input power requirements. Part tolerances must also be considered when designing for robustness.

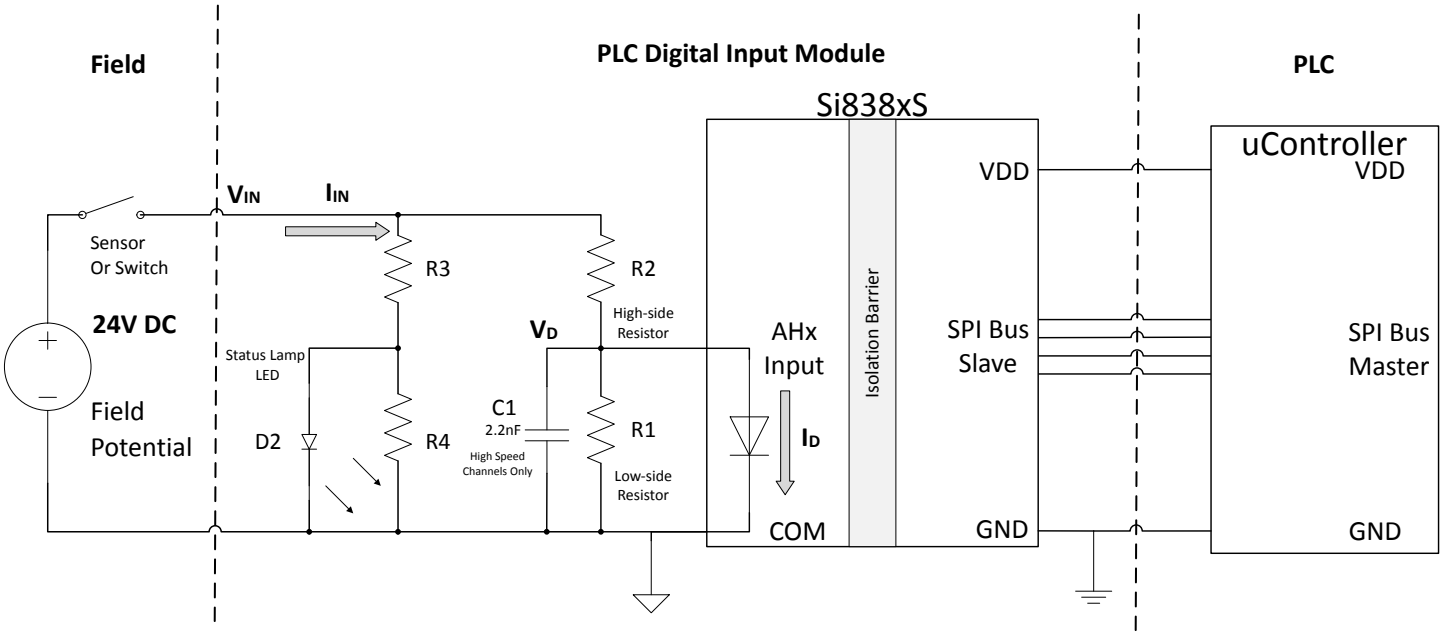


Figure 6.1. Parallel Output System Configuration for IEC61131-2 Adherence

7. IEC 61131-2 Recommended Bill of Materials (24 VDC)

The Si838x data sheet provides a recommended bill of materials for systems compliant with IEC61131-2 Type 1, 2, and 3 digital inputs. The following table restates the recommended input networks.

Table 7.1. Bill of Materials Recommendations for IEC Standard PLC Input Type

IEC Standard PLC Digital Input Type	R1 (Ω)	R2 (Ω)	Series
Type 1	2400	6200	E24
Type 2	390	1500	E24
Type 3	750	2700	E24

The following table provides the relevant data for TR1 and TR2 per recommendation.

Table 7.2. Transition Points TR1 and TR2 for the Recommended Input Networks Based on IEC 61131-2 Standards

Transition Values - Type 1 (R1 = 2400 Ω, R2 = 6200 Ω)					
Corner Symbol	**Point**	**I_{TR1} (mA)**	**V_{TR1} (V)**	**I_{TR2} (mA)**	**V_{TR2} (V)**
Min–Min	Min1	0.99	7.40	0.74	5.70
	Min2	1.16	8.43	0.91	6.72
T–T	Typical	1.18	8.70	1.07	7.97
Max–Max	Max1	1.40	10.15	1.35	9.86
	Max2	1.55	11.09	1.51	10.79
Transition Values - Type 2 (R1 = 390 Ω, R2 = 1500 Ω)					
Corner Symbol	**Point**	**I_{TR1} (mA)**	**V_{TR1} (V)**	**I_{TR2} (mA)**	**V_{TR2} (V)**
Min–Min	Min1	3.72	6.84	3.18	5.91
	Min2	3.76	6.85	3.23	5.92
T–T	Typical	4.14	7.60	3.88	7.13
Max–Max	Max1	4.62	8.42	4.51	8.23
	Max2	4.67	8.45	4.56	8.26
Transition Values - Type 3 (R1 = 750 Ω, R2 = 2700 Ω)					
Corner Symbol	**Point**	**I_{TR1} (mA)**	**V_{TR1} (V)**	**I_{TR2} (mA)**	**V_{TR2} (V)**
Min–Min	Min1	2.15	7.08	1.78	5.95
	Min2	2.27	7.35	1.90	6.21
T–T	Typical	2.45	7.98	2.27	7.44
Max–Max	Max1	2.77	8.98	2.70	8.76
	Max2	2.88	9.24	2.81	9.02

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