AN1155: Differences between Si5342-47 and Si5392-97

This document highlights the key differences between the high performance Si534x family of products and the ultra-high performance Si539x products. The key products discussed are shown below:

- Si5342 vs Si5392
- Si5344 vs Si5394
- Si5345 vs Si5395
- Si5346 vs Si5396
- Si5347 vs Si5397

In summary, the Si5392-97 (revision A) are next generation versions of the Si5342-47 (revision D) devices with the following improvements:

- Better phase jitter performance
- Enhanced hitless switching performance
- More outputs for the Si5395

KEY FEATURES

- NEW P-grade (Precision Calibrated) for 56G/112G PAM-4 SerDes
- Improved jitter for standard A/B/C/D grades
- Improved clock switching
- Additional output clocks

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1. When to Consider Using the Si539x Versus the Si534x

The Si539x devices are Skyworks' newest family of ultra-high performance jitter attenuator clocks. Based upon the popular Si534x's DSPLL technology, the Si539x offers enhancements to meet the needs of the latest communications equipment designs. Customers who use the Si534x but need lower jitter, improved hitless reference switching, or need more output clocks should consider future-proofing their design with the Si539x clocks. For example, the latest high-speed data interconnects use 56G SerDes and require lower jitter. In this case, the Si539x P-grade devices offer a guaranteed maximum jitter specification of less than 90 fs-RMS (12kHz - 20 MHz) giving more design margin than the Si534x. However, those who are happy with the performance of the Si534x can continue to do so. Skyworks will support the Si534x revision D products for many years to come.

For those who have already decided to use the Si539x devices, please see Section 3. Migration from Si534x to the Si539x to see how to seamlessly move your Si534x project to the Si539x.

2. New Features and Capabilities

The Si539x offers options for improved jitter performance, reduced phase transients during input reference switching, and has added two more output clocks. This section provides details on the improvements on the Si539x jitter attenuating clock family.

2.1 Improved Jitter

The Si534x family of products offers a standard integer mode or a fractional mode with low-jitter performance, as shown in the table below.

Table 2.1. RMS Phase Jitter for the Si5342-45

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RMS Phase Jitter	J_{GEN}	Integer Mode 12 kHz to 20 MHz		90	145	fs rms
		Fractional Mode 12 kHz to 20 MHz		120	170	fs rms

Similar to the Si5345/4/2, the Si5395/94/92 has an integer and fractional mode but the jitter performance of these is even lower. Some customer specific 56G PAM-4 SerDes plans requiring 156.25MHz and 312.5MHz can be created with the precision calibrated P-grade option to deliver MAXIMUM jitter of 90fs.

Table 2.2. RMS Phase Jitter for the Si5392-95

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
RMS Phase Jitter (Grade P)	J_{GEN}	$f_{in} = f_{out}$ = 312.5 MHz		—	75	100	fs
		f_{in} = 25 MHz	f_{out} = 156.25 MHz	—	69	90	fs
			f_{out} = 312.5 MHz	—	69	95	fs
			f_{out} = 100 MHz	—	150	200	fs
			f_{out} = 50/25 MHz	—	200	300	fs
RMS Phase Jitter (Grade A/B/C/D)	J_{GEN}	Output divider Integer Mode		—	85	125	fs
		Output divider Fractional Mode		—	100	170	fs

The jitter performance of the Si5397/96 are the same as the previous generation products Si5347/46.

Table 2.3. Phase Jitter for the Si5397/96 and Si5347/46

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RMS Phase Jitter	J_{GEN}	12 kHz to 20 MHz		95	140	fs

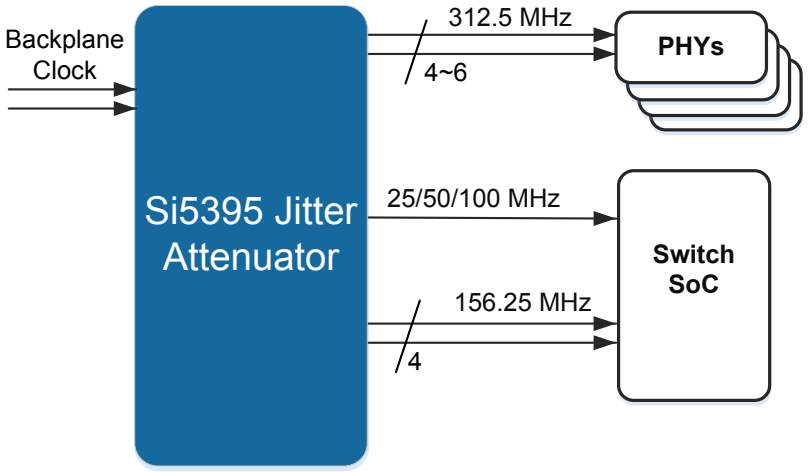

Figure 2.1. Si5395 56G SeDes

The current 28G SerDes reference designs from customers like BRCM have designed in the Si534x. The next generation applications from Broadcom should use the Si539x devices.

2.2 Additional Output Clocks

The Si5395 jitter attenuator features 12 output clocks versus the Si5345's 10-outputs. These additional outputs (OUT0A and OUT9A) can be set to be integer multiples of OUT0 and OUT9 respectively and must be powered from the same respective power supplies. These additional 2 outputs in combination with proprietary MultiSynth and DSPLL technologies allow users to reduce the number of components used thereby reducing system cost and saving space. An example of this clock tree consolidation is shown in Figure 3.1 below.

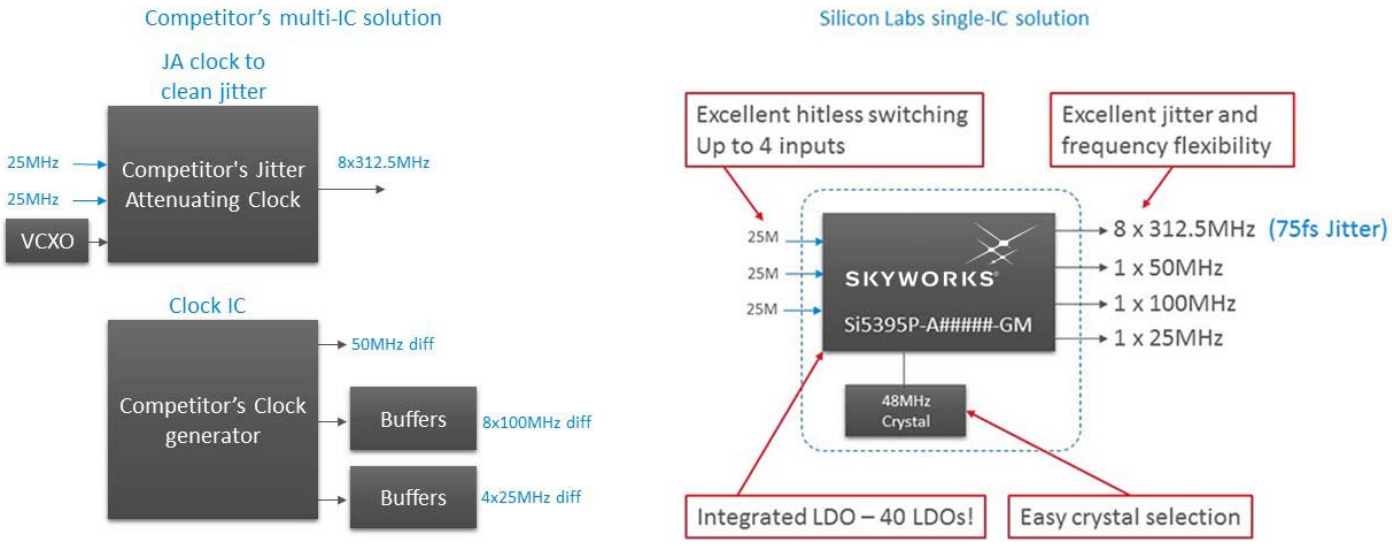

Figure 2.2. Skyworks Advantage Compared to Competing Devices

2.3 Input Clock Switch Improvements

Hitless switching and frequency-ramped switching are requirements found in many communications systems that use clock frequency and phase synchronization reference. Switching between 2 inputs can occur either internal to the Si539x using the internal crosspoint multiplexer or externally via external MUX/FPGA. The Si539x has enhanced hitless switching to deliver the lowest phase and frequency transient for both internal and external switching.

Hitless and frequency-ramped switching behavior for ther Si5392-97 are supported in Skyworks' Clock-Builder™ Pro software version 2.25 or later.

Table 2.4. Input Clock Switching Comparison

Si534x operation	Si539x operation
Si534x features hitless switching, but may exhibit larger phase/frequency transients at low phase detector input frequency typically associated with low input clock frequencies (e.g., 8 kHz).	The Si539x devices feature significantly improved hitless switching at all frequencies, including low-phase detector input frequency typically associated with low-input clock frequencies. This includes both manual and automatic reference switching.
Si534x devices have the option to enable a frequency ramp/phase buildout upon exit from holdover or freerun (startup/reset)	Si539x devices have the option of enabling a more precise phase buildout upon exit from holdover or freerun

Hitless switching performance is dependent on the phase detector input frequency (Fpfd) associated with the frequency plan. The table below shows the performance with both automatic and manual hitless switching with 8 kHz and 2 MHz Fpfd frequencies.

Table 2.5. Hitless Switching Performance

Auto/Manual	Fpfd	DSPLL BW	Output Phase transient	
			Typ	Max
Auto	2 MHz	400 Hz	0.2 ns	0.3 ns
Manual	2 MHz	400 Hz	0.2 ns	0.25 ns
Auto	8 kHz	400 Hz	0.5 ns	1.2 ns
Manual	8 kHz	400 Hz	0.5 ns	1.0 ns

3. Migration from Si534x to the Si539x

Migration from Si534x to Si539x can be done with an import tool built into CBPro. First, ensure that the latest version of CBPro (version 2.25 or later) is installed on your computer and follow the steps shown below.

Step 1 - Click on the *Convert Existing Project/NVM File* button on the main page

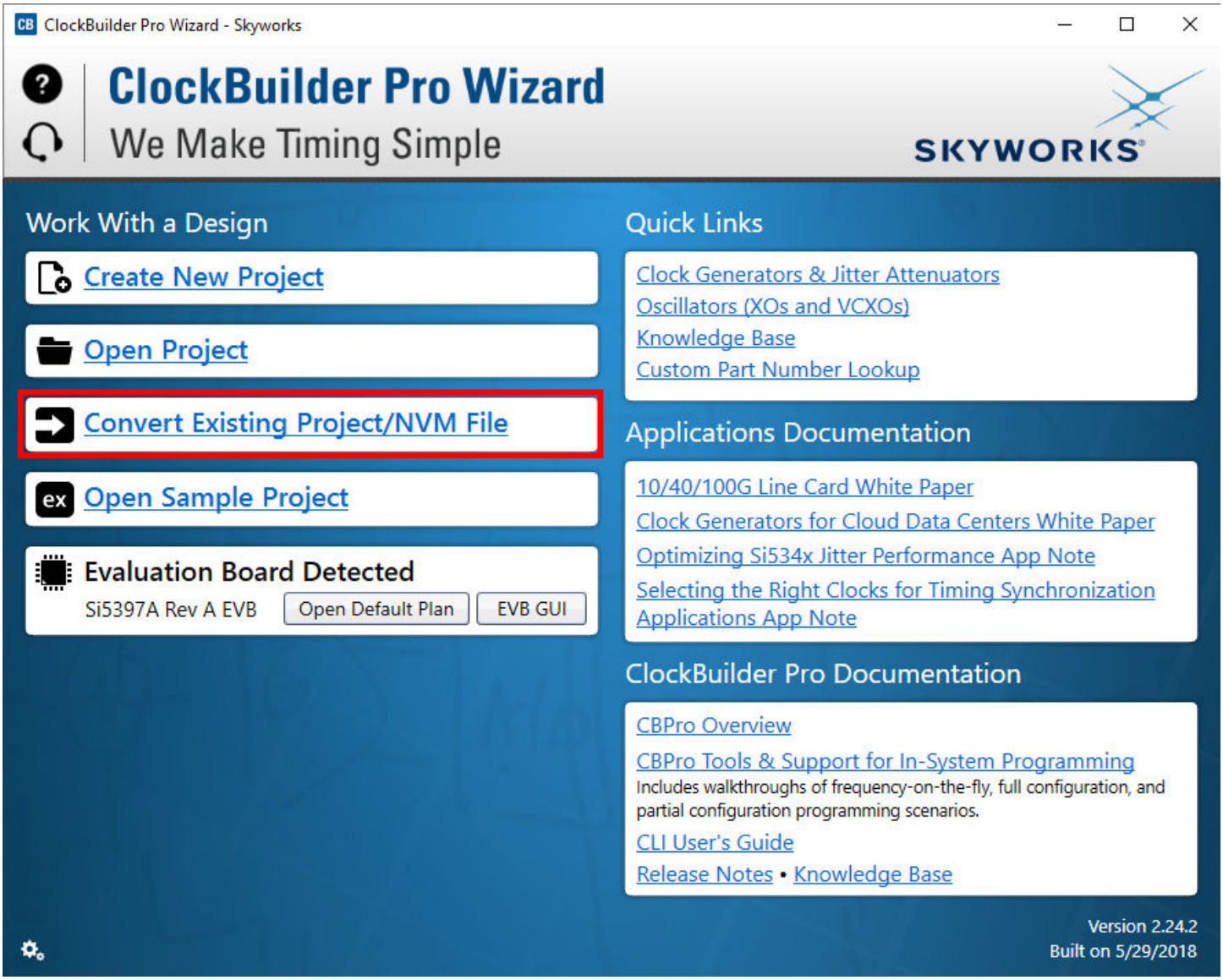

Figure 3.1. Import Design from Si534x Project File

Step 2 - Select the part that you want to convert from and the new part you want to convert to.

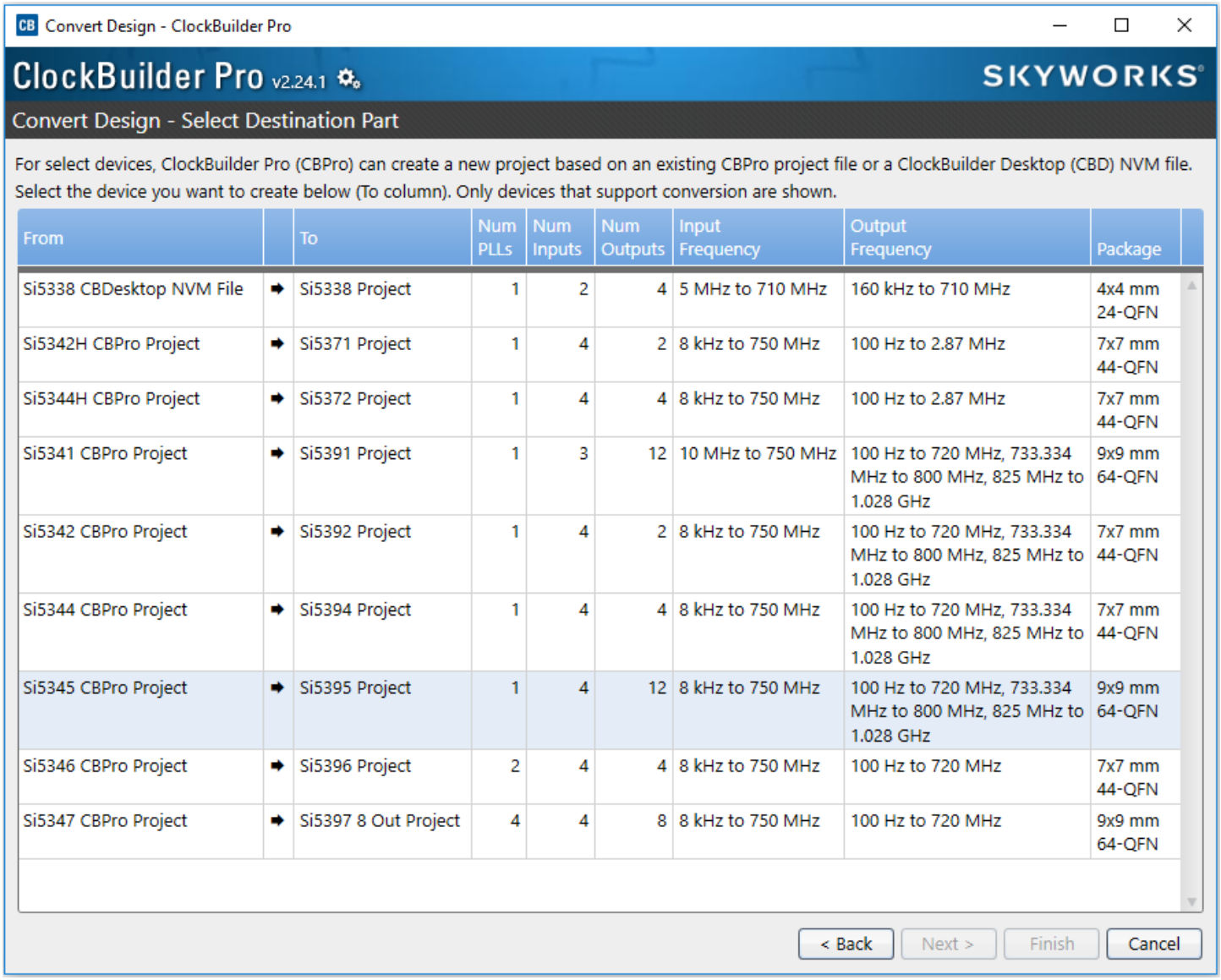

Figure 3.2. Select Part Number to Convert

Step 3 - Select the CBPro project file to be converted.

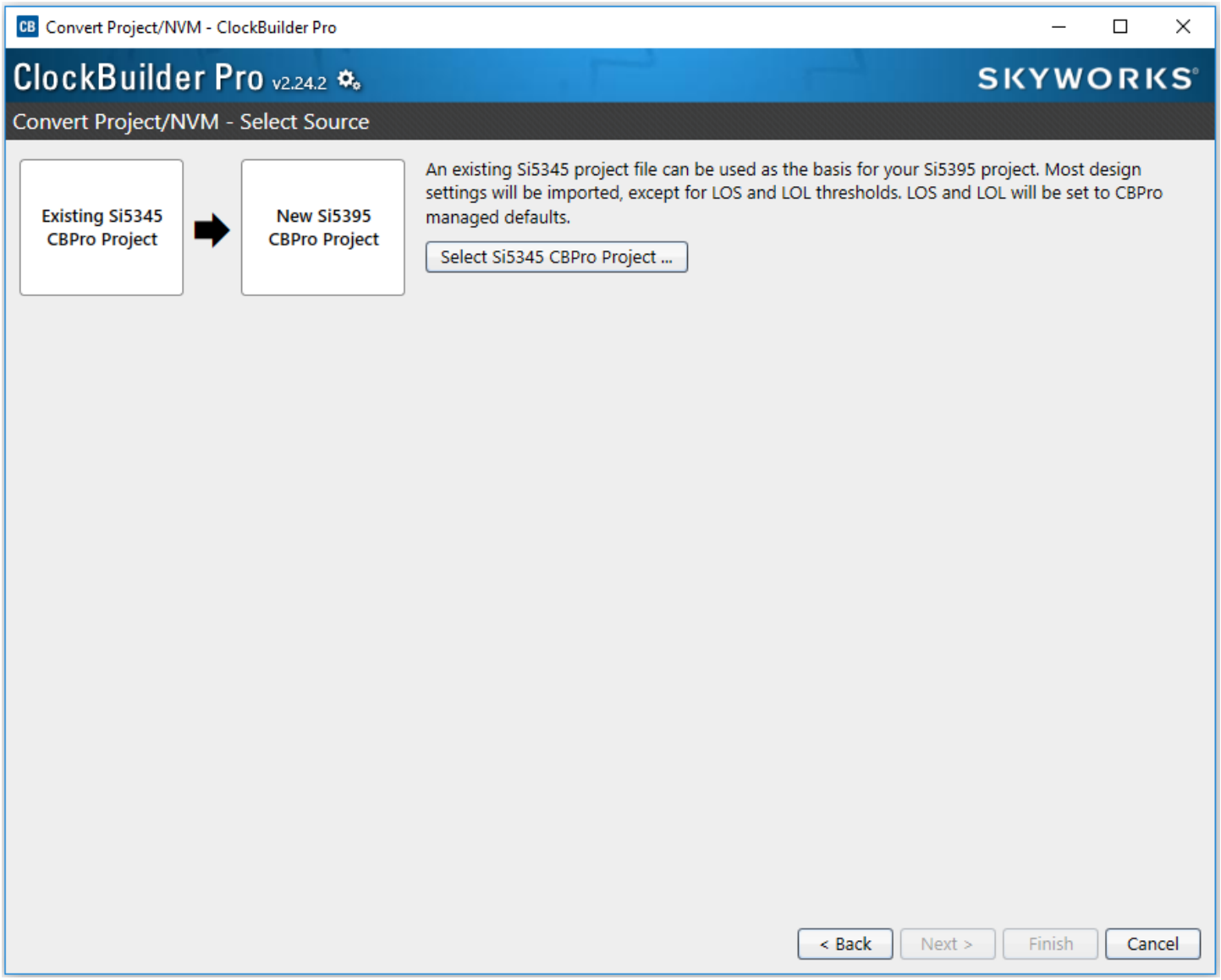

Figure 3.3. Select CBPro Project File to Convert

Once the file is selected, CBPro will convert the project to the new part number. It is important to note that while the majority of the settings will be copied over, the LOS and LOL settings will be overridden by the new Si5395 default settings. It is important to review all converted Si539x plans to ensure that settings are accurate.

While the register map between the Si534x and Si539x look similar, there are new registers in the Si539x to support the enhanced feature set. These additional registers are only configured and enabled after this conversion is made using CBPro. Therefore, loading a Si534x register programming file (aka "register script") into a Si539x in-system is not supported and could result in the device not functioning as expected.

3.1 Device Ordering and Identification

The revision letter, which is the 9th digit of the ordering part number, indicates "A" for product revision A, for example, Si5395C-A-GM or Si5395C-Axxxxx-GM (where xxxxx is the custom OPN ID). See the ordering guide in the datasheet for details on the ordering part number.

4. Register Changes

To preserve backward compatibility, all of the setting names in Si534x revision D have been left unchanged in the Si539x. Several new registers have been added to support the new features described above.

Writing a Si534x register file to a Si539x device is not supported. The project file must first be converted into the Si539x project using CBPro conversion tool, and then re-exported to a programming file. This will also ensure new device features are enabled. In the case of the Si5345/Si5395, for example, the additional 2 outputs (OUT0A and OUT9A) will only be available for configuration after conversion from the Si534x project file to a Si5395 project file.

Details about converting old plans to new plans are provided in Section 3. Migration from Si534x to the Si539x and detailed descriptions of the new features can be found in the reference manual for each device.

5. Supporting Documentation

Document / Resource	Description / URL
Si5395/94/92 Data sheet Si5397/96 Data sheet	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5395-94-92-a-datasheet.pdf https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5397-96-a-datasheet.pdf
Si5395/94/92 Family Reference Manual Si5397/96 Family Reference Manual	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si5395-94-92-family.pdf https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5397-96-a-datasheet.pdf
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AN1151: Using the Si539x in 56G SerDes Applications	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/an1151-using-si539x.pdf
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Development Tools	https://www.skyworksinc.com/en/Products/Timing
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