Optimizing Design and Layout for the Si5318/20/21/64 Clock ICs

1. Introduction

The Skyworks Si5318/20/21/64 (Si53xx) family of clock ICs is capable of generating clock signals with extremely low jitter, making these devices well suited for clock cleaning, switching, and distribution in SONET/SDH equipment. This application note discusses design and layout considerations and suggests the best engineering practices for achieving optimal jitter performance when designing with these devices.

The following topics are discussed:

- Recommendations for new designs
- Power supply considerations
- Bandwidth selection
- Input/output interfaces and signal conditioning
- Minimizing electro-magnetic noise coupling

2. Recommendations for New Designs

Figures 1, 2, 3, and 4 show typical application circuits for the Si5318, Si5320, Si5321, and Si5364. These figures illustrate Skyworks recommendations for new designs. All clock I/Os are ac-coupled, and clock input transmission lines are terminated externally.

If board space is not an issue, it is also recommended that new designs include locations for input clock filter components. Most applications will not need input clock filtering. However, this conservative approach for new designs allows for maximum flexibility in case the input clock is especially noisy.

See "2.3.3. Input Clock Signals" on page 6 for details about how to choose values for the input clock filter if needed.

2.1. Power Supply Considerations

The Si53xx clock device is powered by applying a 3.3 V system supply to the 3.3 V power supply pins of the device. The internal on-chip regulator produces the 2.5 V level that powers the precision clocking circuitry of the device. The internal regulator must be compensated by an external RC network with a time constant in the range of 15–50 µs. The baseline compensation network (which corresponds to the 3.3 V jitter specifications in the data sheets) is a single 33 µF tantalum capacitor with an effective series resistance (ESR) of 0.8 Ω. This provides an RC time constant of 26.4 µs. An example of a capacitor that meets these specifications in the Venkel part number TA6R3TCR336KBR.

Powering the Si53xx family of clock ICs with the integrated 2.5 V regulator is the preferred way of isolating the precision clocking circuitry of the devices from spurs and random noise on the 3.3 V system supply (provides a minimum of 40 dB of isolation). This allows the devices to deliver good jitter performance despite being powered from a relatively noisy supply. The 2.5 V chip supply output must not be shared with other system components.

When operating an Si53xx device using the internal 2.5 V regulator, use a small 2.5 V power island dedicated to the device's V_{DD25} pins. The 2.5 V power island should ideally be placed between two ground planes to isolate it from any ambient system noise, including noise on other power planes. It is also recommend that the 3.3 V power supply should be decoupled by placing a 0.1 µF, a 2200 pF, and a 22 pF capacitor between the 3.3 V power supply and a ground plane on the board. These capacitors should be placed as close as possible (i.e., within 5 mm of the clock device). Using three or more 0.1 µF capacitors and eliminating the 2200 pF and 22 pF capacitors is also acceptable for decoupling the 3.3 V power supply.

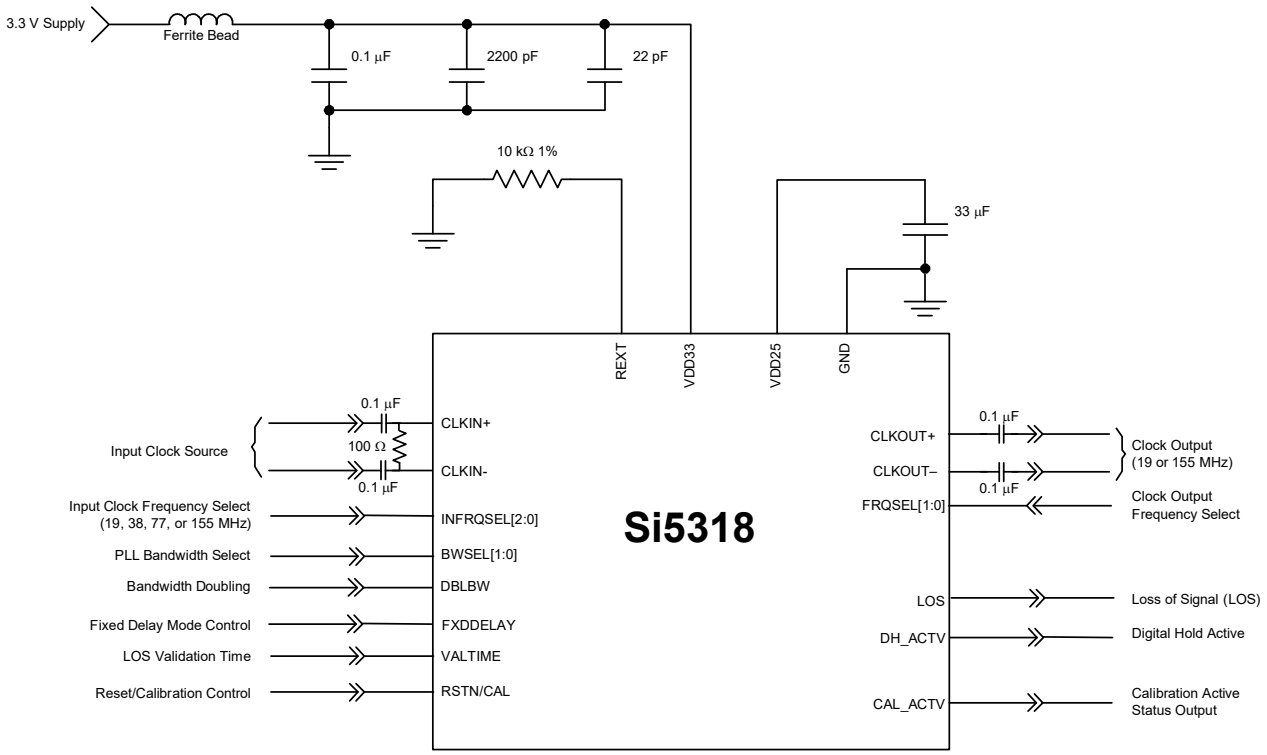

Figure 1. Si5318 Typical Application Circuit

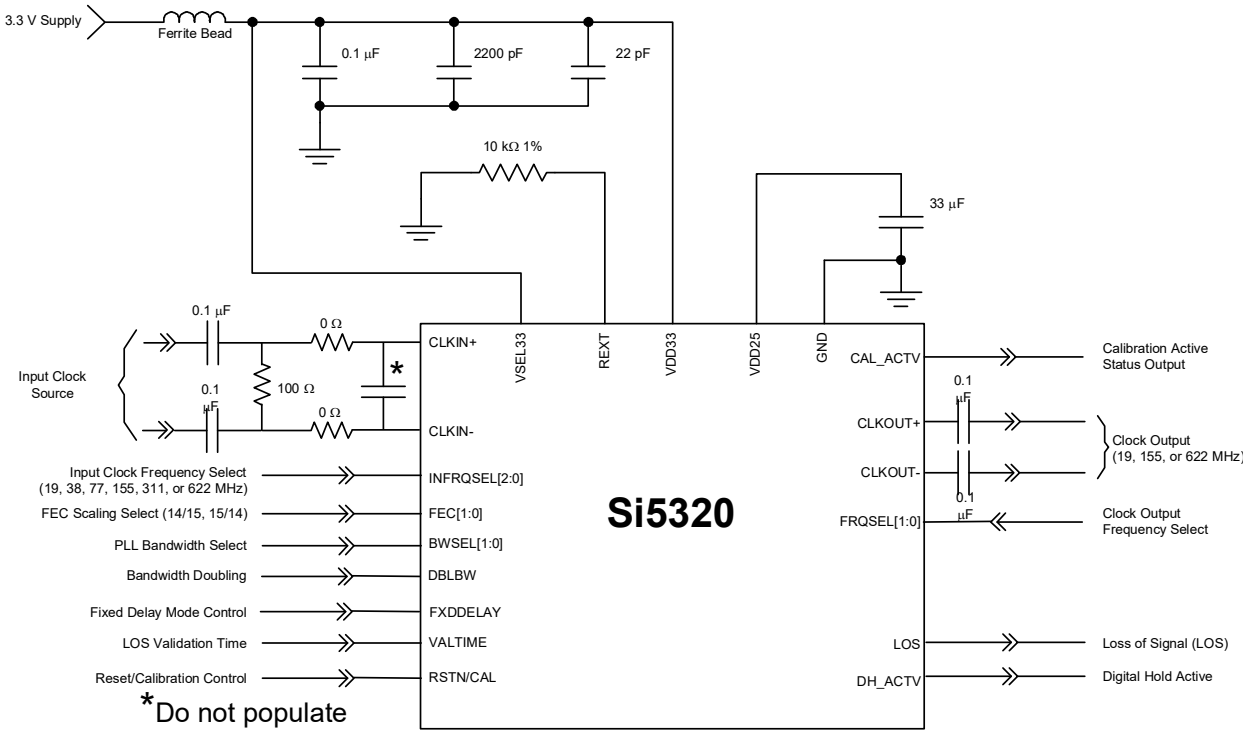

Figure 2. Si5320 Typical Application Circuit

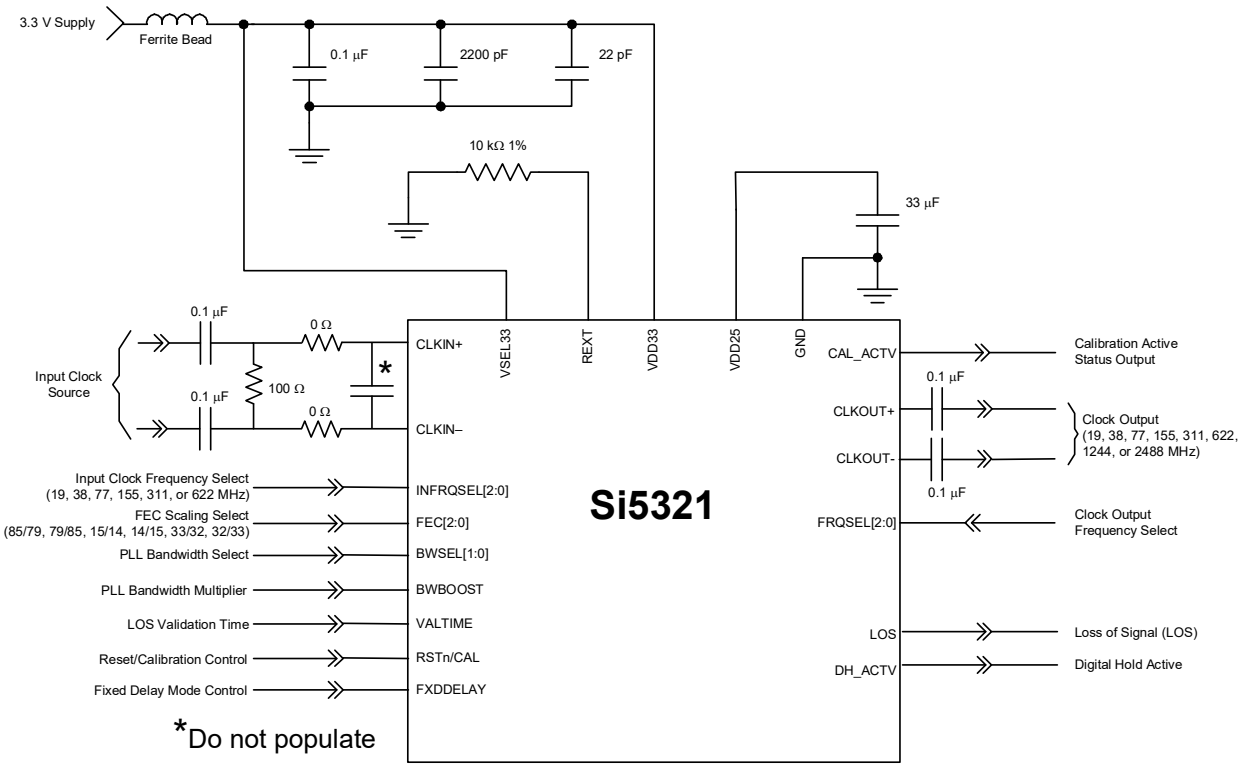

Figure 3. Si5321 Typical Application Circuit

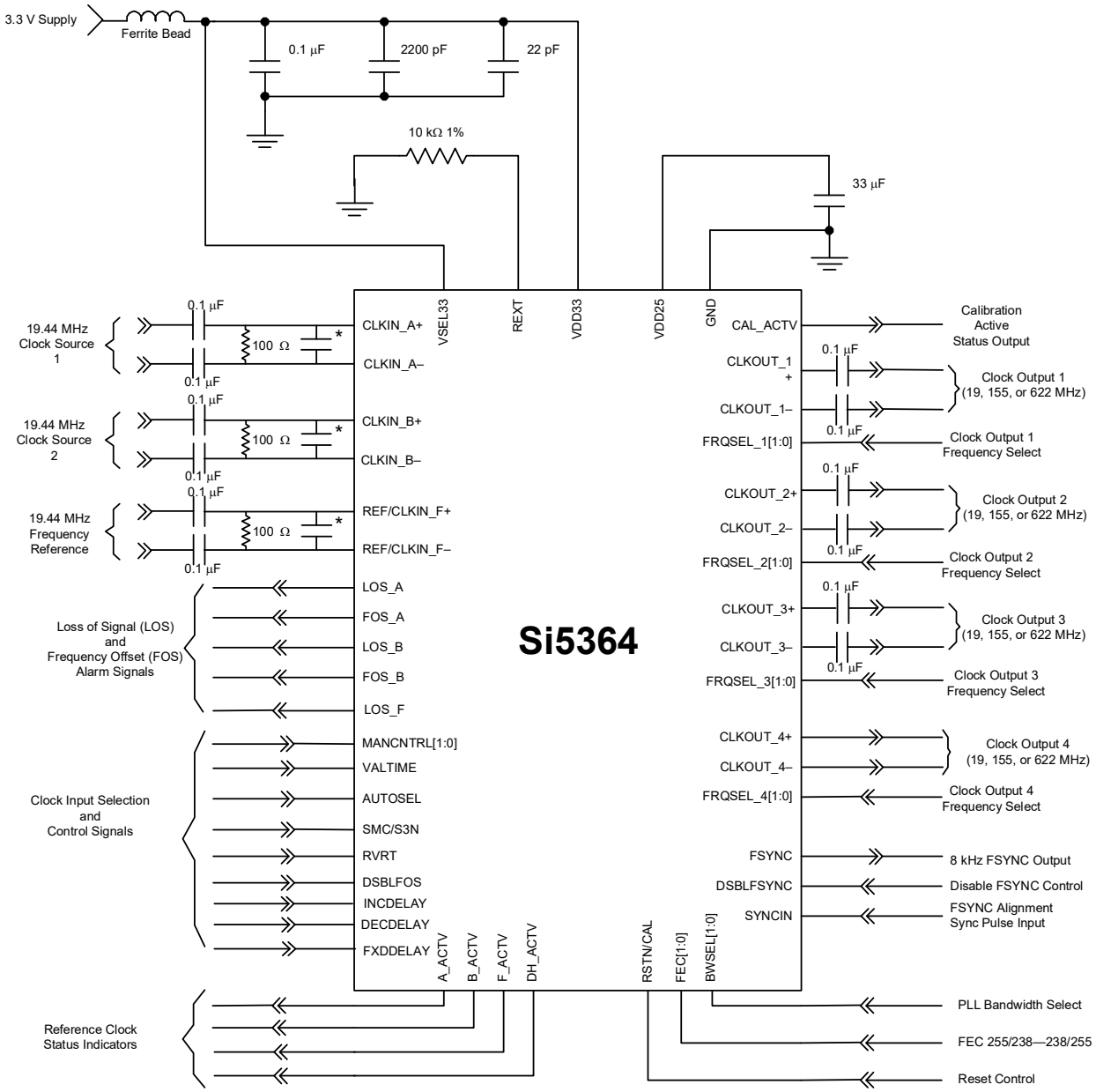

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Figure 4. Si5364 Typical Application Circuit

2.2. Bandwidth Selection

The Si53xx clock ICs provide several phase-locked loop (PLL) bandwidth settings. It is important to understand the trade-offs involved with these settings to select the optimal bandwidth for each application.

2.2.1. Background Information on Generated Noise vs. Bandwidth in PLLs

All PLLs generate some noise that appears as jitter on the output clock. Although this noise is produced by a variety of sources within the PLL itself, all these sources can be roughly grouped into two categories: front-end noise and oscillator noise. Because of the dynamics of the PLL, front-end noise increases with increased PLL bandwidth while oscillator noise decreases. Therefore, for each PLL, there is a bandwidth at which the front-

end noise equals the oscillator noise, resulting in the minimum total generated noise for that PLL.

2.2.2. Selecting the PLL Bandwidth for Minimum Total Output Noise (Jitter)

Although the previous section suggests that the optimal bandwidth setting is always the one that produces the minimum generated output jitter, there is another important issue to consider: input clock noise (jitter). Input clock noise is partially transferred to the output clock (according to the jitter transfer characteristic of the PLL) where it adds to the generated noise on the output clock. Like front-end noise, the amount of input clock noise that is transferred to the output clock increases with PLL bandwidth. Since total output clock noise is most important in a system application, both generated noise and transferred noise must be considered when selecting the best PLL bandwidth for the application.

To predict the amount of input clock noise that transfers to the output clock, it is necessary to know the jitter transfer characteristic of the PLL and the jitter characteristics of the input clock. Predicting the output noise power in each bandwidth setting is then a question of passing the input clock noise through the jitter transfer function for that bandwidth setting and then adding this transferred noise power to the generated noise power for that bandwidth setting. Since Si53xx clock devices use DSPLL technology to deliver stable predictable transfer characteristics, this task is simplified compared to other PLL-based clock devices whose transfer characteristics change with temperature, supply, and aging.

2.2.3. Considerations for Using the Bandwidth Boosting Modes

Some Si53xx clock devices offer bandwidth boosting modes that provide further improved output jitter generation performance. When operating in these modes, the devices operate in the same way as they do when operated in the non-boosted modes except that the input jitter tolerance is reduced. Also, FEC scaling and hitless recovery are not available in the bandwidth boost mode. Refer to the applicable data sheet for specific input jitter tolerance and output jitter generation specifications.

2.3. Input/Output Interfacing and Signal Conditioning

Si53xx signal interfaces may be divided into two broad categories, clock signals and LVTTL signals, each of which are treated somewhat differently. The Si53xx clock interfaces are differential but designed so that clocks may be implemented in either single-ended or differential mode. Regardless of their fundamental frequency, they should be considered high-speed signals, routed as transmission lines, and terminated for proper signal integrity. In contrast, LVTTL signals are single-ended and quasi-static and generally need not be terminated.

This section discusses differential clock interfaces from a specification point-of-view and some implementation detail. Afterward, LVTTL I/O considerations are also briefly discussed. In addition to the information presented here, IBIS models for the Si53xx clock chip I/Os are also available from Skyworks if needed.

2.3.1. Si53xx Differential Clock Interfacing: A General approach

The following is a general approach to use when considering the interface between the Si53xx clock differential I/Os and common differential signaling types, such as CML, LVPECL, LVDS, etc. The emphasis is on reviewing the relevant specifications and interfacing with passive devices only (resistors and capacitors) as opposed to situations requiring amplifiers, interface translation ICs, etc.

First, a note about ac versus dc coupling: The Si53xx family of ICs is specifically designed for ac coupling on the clock I/O. Therefore, it is strongly recommend that ac coupling be used for all applications. Even where dc coupling may appear feasible from a CM (common mode) voltage specification perspective, the driver output impedance may adversely impact the receiver input common mode voltage, which may cause the input sensitivity to degrade significantly. In addition, ac coupling has some other advantages:

- It eliminates the need for level shifting.
- It allows the driver and receiver to operate from different power supply voltages if necessary.

For dc coupling, consider the compatibility of the driver common mode output voltage or VOCM with the receiver common mode input voltage or VICM range. By employing ac coupling, the consideration for the CM voltage specifications is omitted in the following steps.

In the following discussion, the Si53xx may be either the driver or the receiver, and the application may be differential or single-ended.

1. Review Driver Specs
   - Driver differential output voltage swing or VOD Typically, LVPECL driver outputs have a VOD of ~700–800 mV or more while LVDS outputs typically have a VOD of ~350 mV. CML drivers are more vendor-specific, and their VOD may range from ~400 mV up to ~1000 mV. Unless otherwise noted, assume typical large swing CML drivers.
   - Driver output termination
2. Review Receiver Specs

- Receiver differential input voltage swing or VID
- Receiver input impedance

3. Compare the specs for electrical compatibility
   - Is the driver VOD compatible with the receiver VID?
   - Will the driver see its intended load?
4. Review and revise interface circuit for compatibility or performance

Revise the circuit as necessary to properly terminate the differential clock transmission lines. Whenever the Si53xx IC is being used as a receiver, external termination is required. Transmission line termination must be done at the board level since the Si53xx input impedance RIN (CLKIN+, CLKIN–) is ~80 kΩ. This is much higher than typical transmission line impedances. Under normal circumstances, these will be 100 Ω differential microstrip or stripline on a PC Board.

Finally, while level shifting does not apply, the interface circuit may be revised further to incorporate one or more additional design aspects listed below.

- Attenuation for reasons of signal compatibility or to reduce EMI
- Filtering to reduce EMI

2.3.2. Si53xx Differential Clock Interfacing: An example application

Apply the general approach described above to the use of company X's differential LVDS transceiver driving into the Si5321's differential clock inputs.

1. Review Driver Specs

The relevant driver specs are from company X's data sheet.

- Driver differential output voltage for VCC = 3.3 V |VOD| = 247 mV – 454 mV (350 mV typical).
- Driver output termination
- All the specs above assume RL = 100 Ω

2. Review Receiver Specs

In this example, the receiver is the differential clock input of an Si5321 and the relevant specs are as follows:

- Receiver differential input voltage swing
  VID = 200 mV – 500 mV_{PP}
- Receiver input impedance
  RIN (CLKIN+, CLKIN-) = 80 kΩ
  (As the data sheet notes, transmission line termination must be provided separately.)

3. Compare the specs for electrical compatibility
   - Is the driver VOD compatible with the receiver VID?
     Yes, the driver's |VOD| ranges from 247–454 mV which falls within the Si5321's VID range of 200–500 mV_{PP}.
   - Will the driver see its intended load?
     Yes, if we add an external termination equivalent to 100 Ω.
4. Revise interface circuit for compatibility or performance

As stated earlier, termination is required in this example since the Si5321 is the receiver. The basic circuit shown in Figure 6 on page 8 applies.

Additional candidate features:

- **Attenuation**—Unnecessary but permissible down to the guaranteed 200 mV input level
- **Filtering**—While generally not required, a low-pass filter on the clock input is considered good practice.

The next section will review both clock and LVTTL interface implementation in more detail and give several more example schematics.

2.3.3. Input Clock Signals

The Si53xx family of clock ICs use differential clock inputs. Figure 5 shows a simplified clock input circuit.

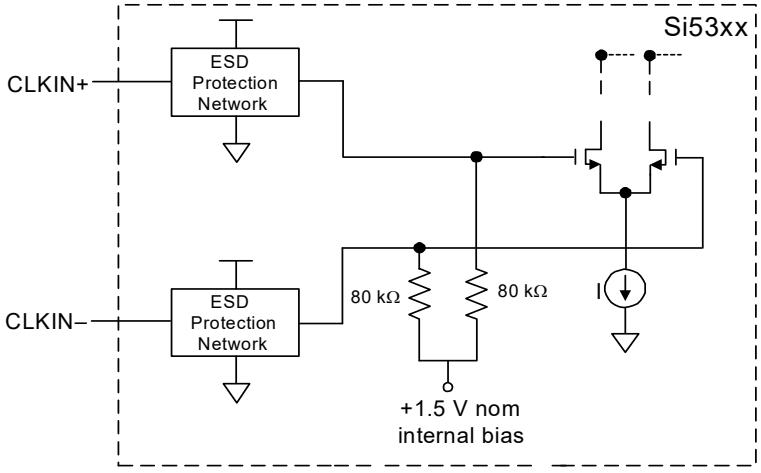


Figure 5. Simplified Clock Input Circuit

The first important feature is that the input impedance is relatively high, which requires that transmission lines be terminated externally. The input impedance is dominated by the 80 kΩ shown and a few hundred ohms of additional series resistance up front due to the ESD protection network.

The second important feature is the presence of an internal dc bias voltage. The VICM or CLKIN Common Mode Input Voltage is nominally 1.5 V. (See the ICs data sheet for specified limits.) No LVPECL style termination to an external dc voltage bias is required. This dc bias is generated from current sources. AC coupling is recommended so that the driver dc bias and impedance are independent of and do not impact VICM.

The Si53xx clock inputs are designed to be driven by either differential or single-ended drivers. See Figures 6 and 7 for illustrations of typical differential and single-ended clock source termination.

Filtering and attenuation (other than for signal compatibility) is normally not needed in Si53xx applications. One possible exception is to minimize the risk of injection lock, a particular form of electromagnetic interference (EMI). Si53xx clock devices will not injection lock unless an extraneous 2.5 GHz source can inject a signal > –62 dBm at an individual pin. If significant interfering energy is present, filtering, attenuation, and good layout can reduce the level of conducted interference on the input clock pins.

The input clocks are the one place where there is most likely to be energy at or near the Si53xx tank frequency and where the amplitude may be sufficient to overdrive the inputs. This is why we recommend at least allowing for the possibility of an input clock filter early on in design. To minimize conducted interference from harmonics on the input clocks, the following suggestions may be implemented:

- Attenuate the clock signal: Use relatively low clock input levels (i.e., 200 to 500 mV_{PP} differential) to minimize the possibility of internally-generated 2.5 GHz harmonics.
- Filter the clock signal: Harmonics can be reduced by the addition of an RC filter to the input clock signals. Setting the pole of the filter near the input clock fundamental frequency is recommended to accomplish both a reduction of the input amplitude of the fundamental and significant roll off of 2.5 GHz harmonic energy.
- Lower the clock frequency (Si5320/21 only): If possible, use lower input clock frequencies. Using a 19.44 MHz or a 155.52 MHz clock input instead of a 622.08 MHz clock input reduces the 2.5 GHz harmonic levels.

The basic circuits shown in Figures 6 and 7 are appropriate for any drivers with on-chip biasing and outputs capable of driving 100 Ω differential or 50 Ω single-ended transmission lines. Typical LVDS and CML drivers, such as another Si53xx clock chip, fall into this category.

Example applications that add filtering to Figures 6 and 7 as suggested in the second bullet item above are illustrated in Figures 8 and 9, respectively. Using the values shown results in corner frequencies near the input clock fundamental.

These filter values should be regarded as suggestions only since there are trade-offs between practical component values, filter frequency response, and the quality of the transmission line termination. For example, in Figure 8, we would generally prefer to use higher value series resistors to minimize the filter's impact on the line termination. However, this is harder to do at higher cutoff frequencies as the table indicates.

An alternate approach is to employ only a single capacitor across the 100 Ω termination resistor. This would be as if the series filter resistors in Figure 8 were shorted using 0 Ω resistors. This approach is useful where the input clock frequency energy is well below the corner frequency necessary to sufficiently filter 2.5 GHz. A good example application is with the Si5364 since it only uses 19.44 Mhz input clocks. Assuming a 100 Ω differential output impedance driver, using a 15 pF capacitor across a 100 Ω transmission line termination results in a corner frequency near 212 MHz, which is still well below 2.5 GHz yet does not significantly impact the input clock or the transmission line termination.

More conservative example applications that may be used are illustrated in Figures 10 and Figure 11 on page 10. In these examples, both attenuation and filtering have been added to Figures 6 and 7, respectively. These would apply if the input clock source contained significant energy at 2.5 GHz and was being driven by a relatively large amplitude swing driver, such as a CML driver. CML drivers typically have a VOD of 700–800 mV or more. LVDS drivers on the other hand typically have a VOD closer to 350 mV, and such attenuation should not be needed or used.

Attenuation would also be required, with or without filtering, for single-ended applications where the clock driver output is LVTTL/LVCMOS. Depending on the part's exact specifications, the output swing might be within a few tenths of a volt of 3.3 V. This far exceeds the Si53xx single-ended input voltage specification of 200–500 mV_{PP} differential.

LVPECL drivers typically require external components to properly terminate their emitter outputs both from a dc and an ac point of view. As always, it is best to double check the vendor's driver termination recommendations. Figure 12 on page 11 shows several possible approaches to using an LVPECL device to drive a differential clock into an Si53xx IC. In all cases, ac coupling is recommended so that there are no CM voltage issues between the driver and the receiver. Remember that the Si53xx device is biased internally and does not require, nor should it be supplied with, a typical LVPECL bias voltage.

The first version, shown in Figure 12(a), is a typical differential LVPECL driver with the outputs terminated individually as complementary single-ended lines. Each side and its termination components should match closely to minimize duty cycle distortion and skew. The resistor values chosen in this example provide a Thevenin equivalent resistance, R_{TH}, of approximately 50 Ω at the receiver end. The Thevenin equivalent voltage, V_{TH}, is about VDD – 2 V = 1.3 V. As mentioned earlier, always confirm the vendor's driver termination recommendations.

The second version, shown in Figure 12(b), uses a true differential termination at the receiver. Here, local termination resistors at the driver are used to provide dc paths for the LVPECL outputs per the manufacturer's recommendations. The value of these resistors is a compromise between dc and ac performance, and the vendor-suggested value may vary anywhere from 75 to about 300 Ω depending on the device. All of these LVPECL input circuits may be revised further to include filtering and/or attenuation if necessary.

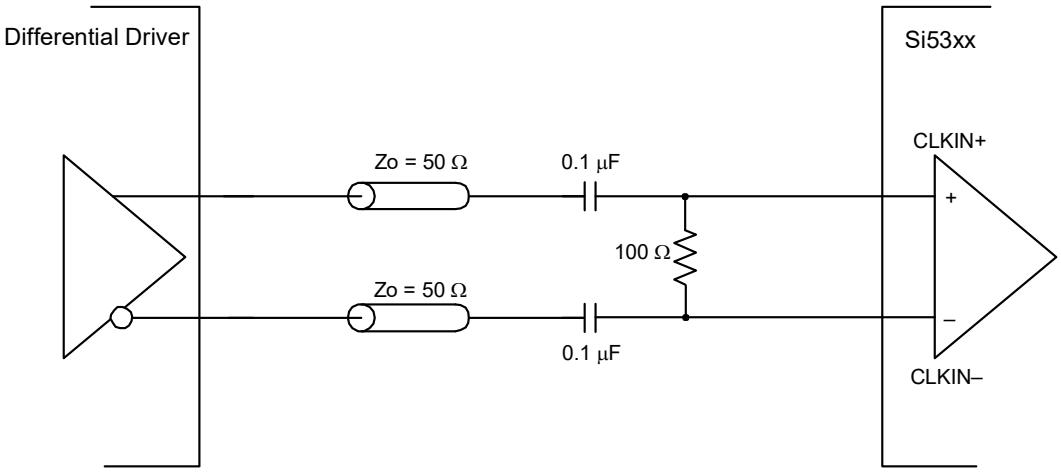


Figure 6. Typical Input Termination for Differential Clock Source

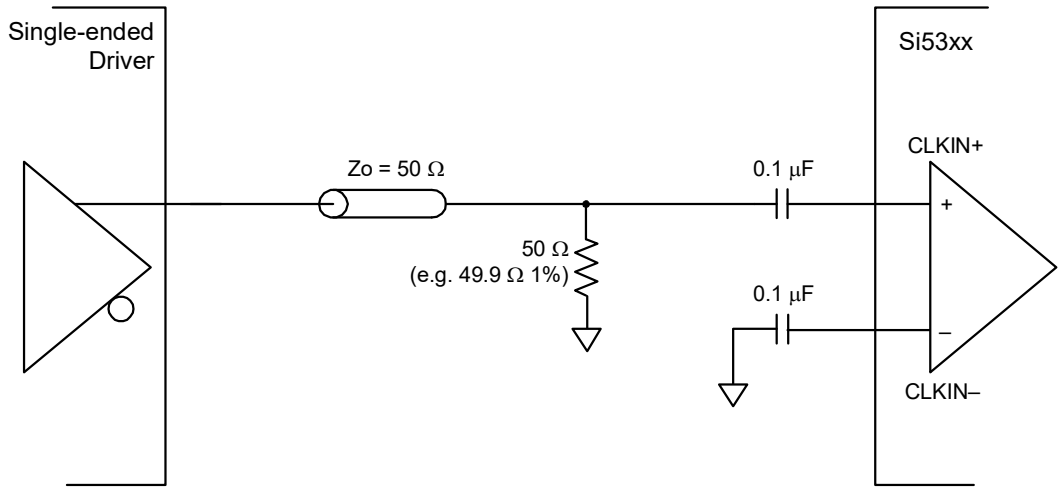
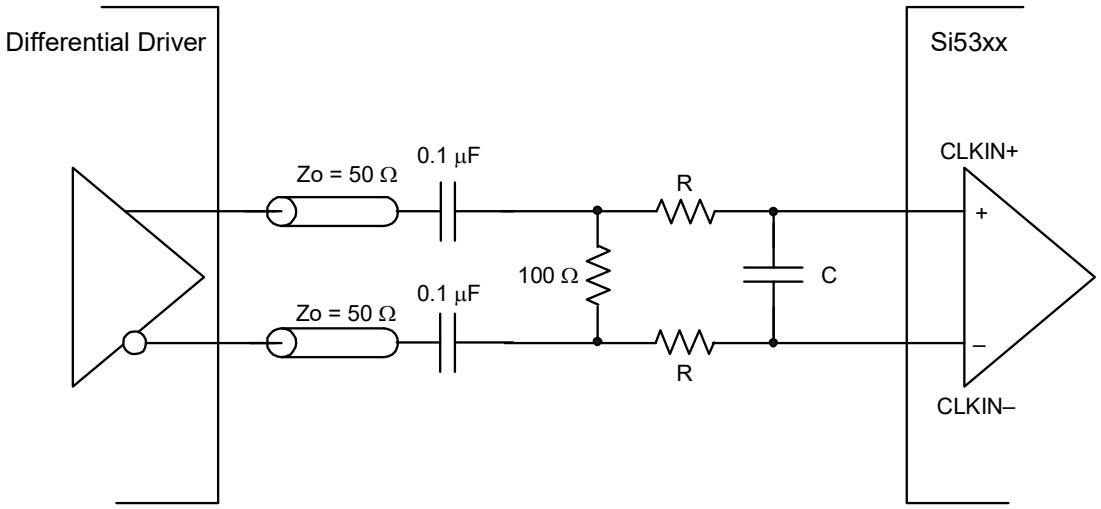
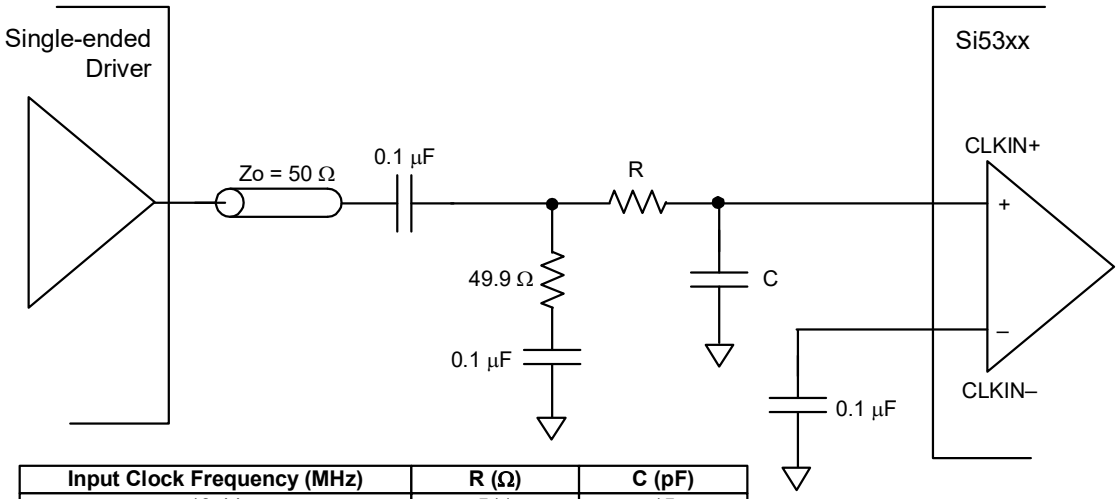


Figure 7. Typical Input Termination for Single-Ended Clock Source



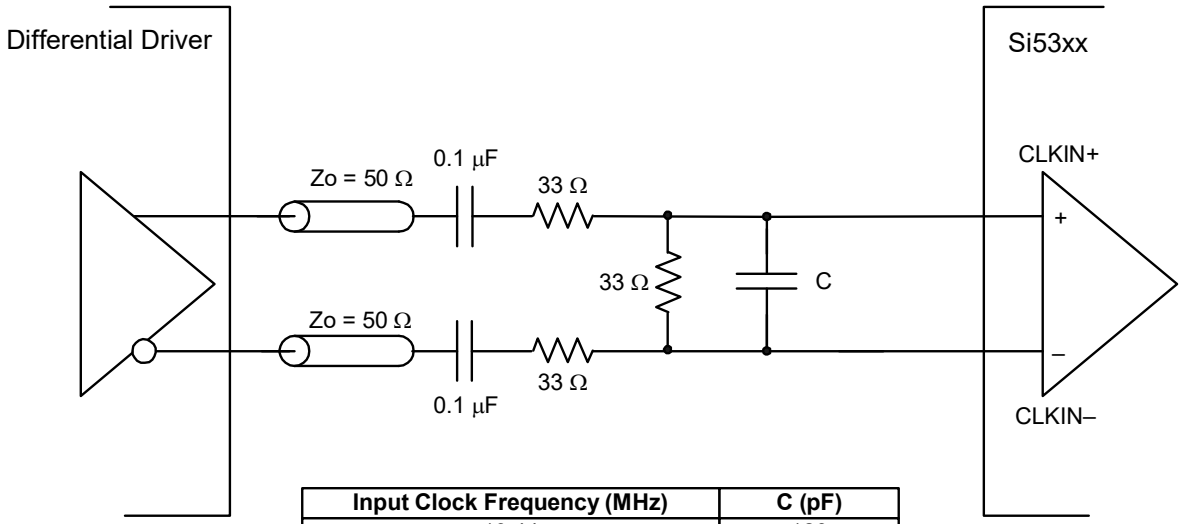
Input Clock Frequency (MHz)	R (Ω)	C (pF)
19.44	511	7.5
38.88	511	3.6
77.76	511	1.8
155.52	453	1.1
311.04	232	1.1
622.08	115	1.1

Figure 8. Example Filtered Input Termination for Differential Clock Source



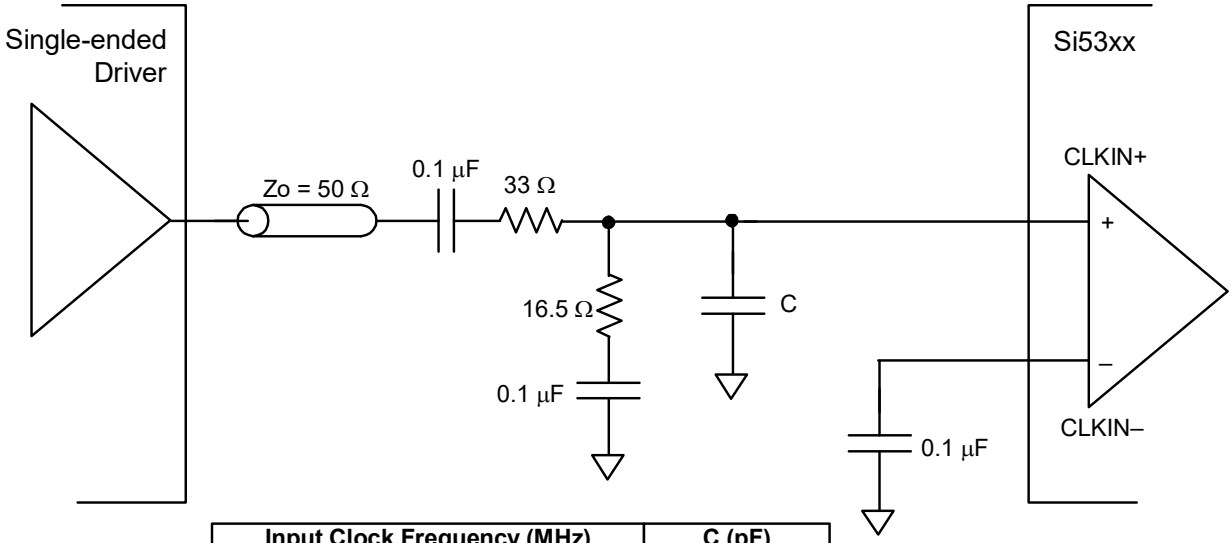
Input Clock Frequency (MHz)	R (Ω)	C (pF)
19.44	511	15
38.88	511	7.5
77.76	511	3.9
155.52	453	2.2
311.04	232	2.2
622.08	115	2.2

Figure 9. Example Filtered Input Termination for Single-Ended Clock Source



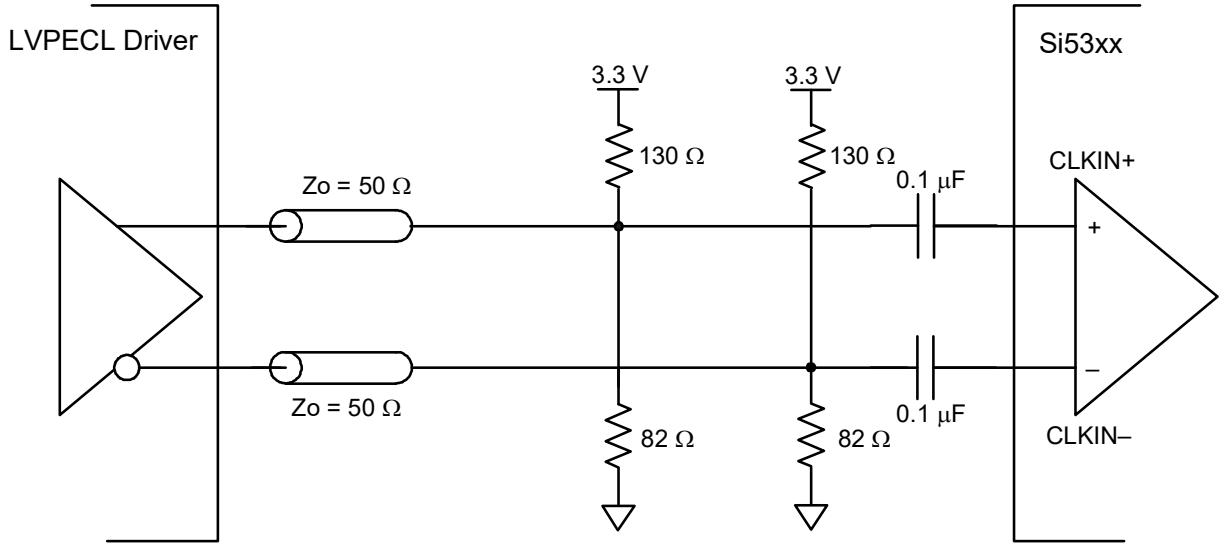
Input Clock Frequency (MHz)	C (pF)
19.44	120
38.88	120
77.76	56
155.52	27
311.04	18
622.08	15

Figure 10. Example Filtered and Attenuated Input Termination for Differential Clock Source

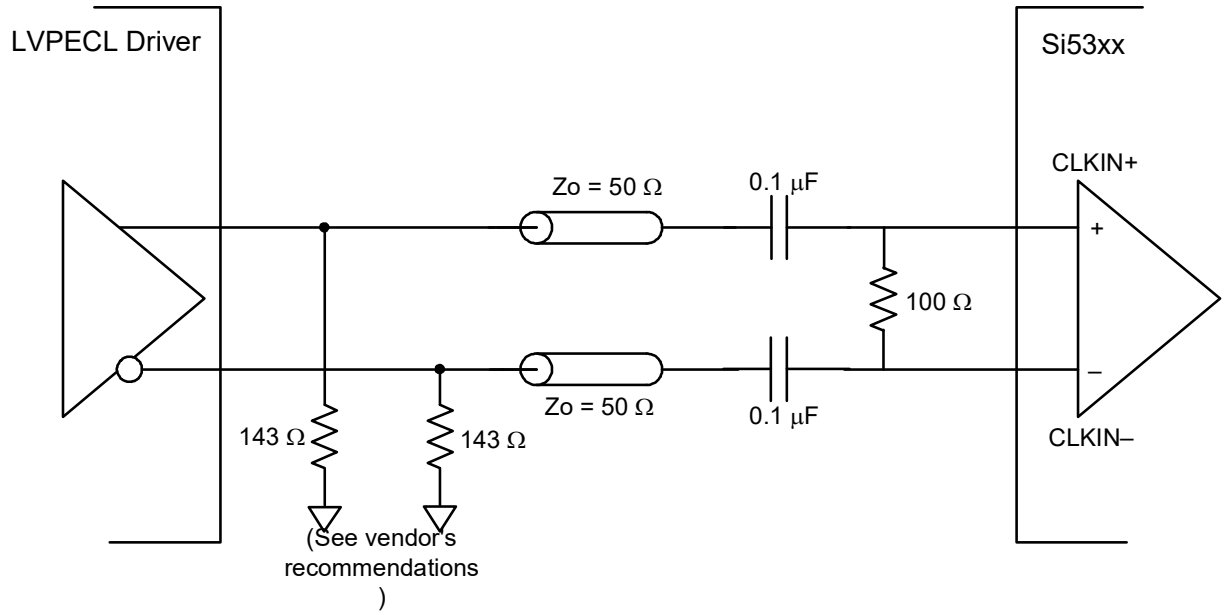


Input Clock Frequency (MHz)	C (pF)
19.44	240
38.88	240
77.76	112
155.52	54
311.04	36
622.08	30

Figure 11. Example Filtered and Attenuated Input Termination for Single-Ended Clock Source



Standard LVPECL DC and AC Termination
(a)



Driver Local DC Termination
(b)

Figure 12. Example Input Terminations for LVPECL Clock Source

2.3.4. Output Clock Signals

The Si53xx family of clock ICs use differential CMOS current mode logic (CML) clock output structures. These are flexible enough to work easily with virtually all common differential signal interfaces. Figure 13 shows a simplified illustration of a CML output buffer.

The output impedance of the buffer is relatively low and designed so that each output clock polarity can operate into a 50 Ω load or differentially into an equivalent 100 Ω load. Si5320/21/64 CLKOUT differential and common mode output voltages, VOD and VOCM, are nominally 906 mV_{PP} and 1.8 V, respectively. Si5318 CLKOUT differential and common mode output voltages, VOD and VOCM, are nominally 938 mV_{PP} and 1.8 V, respectively. Minimum and maximum values are designated on the IC's data sheet.

No LVPECL style termination to an external dc voltage bias is expected or required for the Si53xx devices. AC coupling is recommended so that VOCM is independent of the load's dc bias.

A typical output clock termination is illustrated in Figure 14. This figure applies to typical high-impedance differential receivers (e.g., CML, LVDS, and high-impedance LVPECL-compatible devices that incorporate on-chip biasing). Attenuation may be applied if the Si53xx differential output swing is higher than can be handled by the receiver. However, if the application must interface to a single-ended LVTTL/LVCMOS input, which requires full rail swings, a voltage translation IC must be used.

Figure 15 on page 14 shows a couple of examples for how one might interface to LVPECL receivers that require external dc biasing components. The first example, Figure 15(a) shows the standard LVPECL termination at the receiver with the components configured to provide an equivalent resistance, R_{TH}, of approximately 50 Ω on each side and the standard LVPECL termination voltage, V_{TH} = VDD – 2 V = 1.3 V. Other resistor values may be used which yield R_{TH} = 50 Ohms but a different bias voltage as long as V_{TH} falls within the receiver's specified input common mode range. Always confirm the vendor's receiver termination recommendations.

The alternate example in Figure 15(b) provides a better differential termination but requires the extra 100 Ω resistor and different values for the voltage dividers.

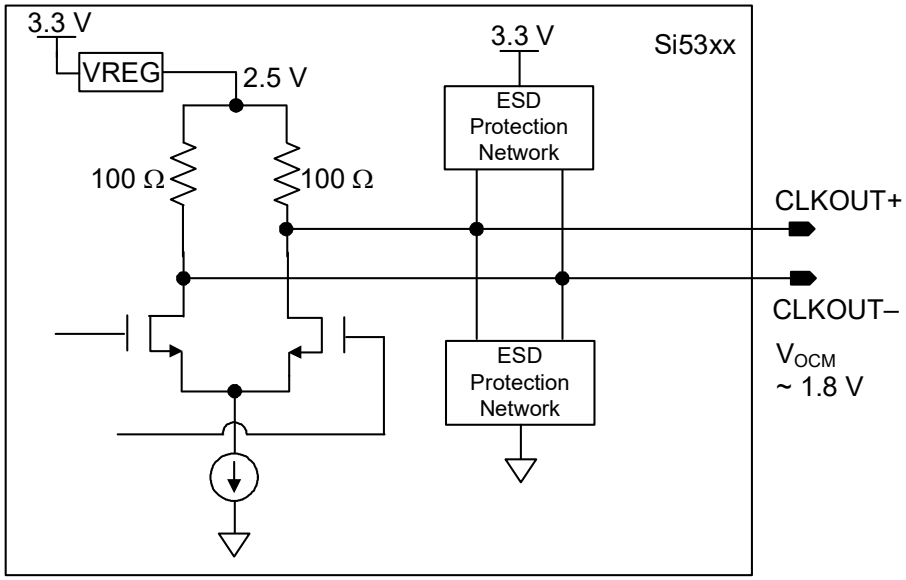


Figure 13. Simplified CML Output Buffer

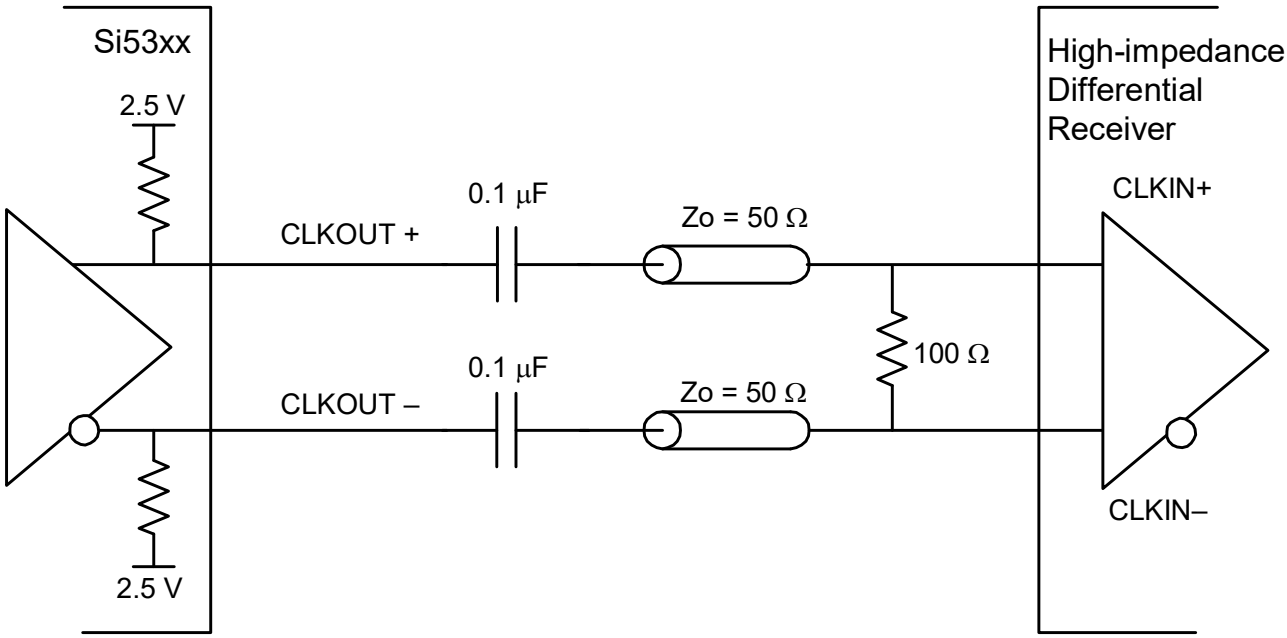
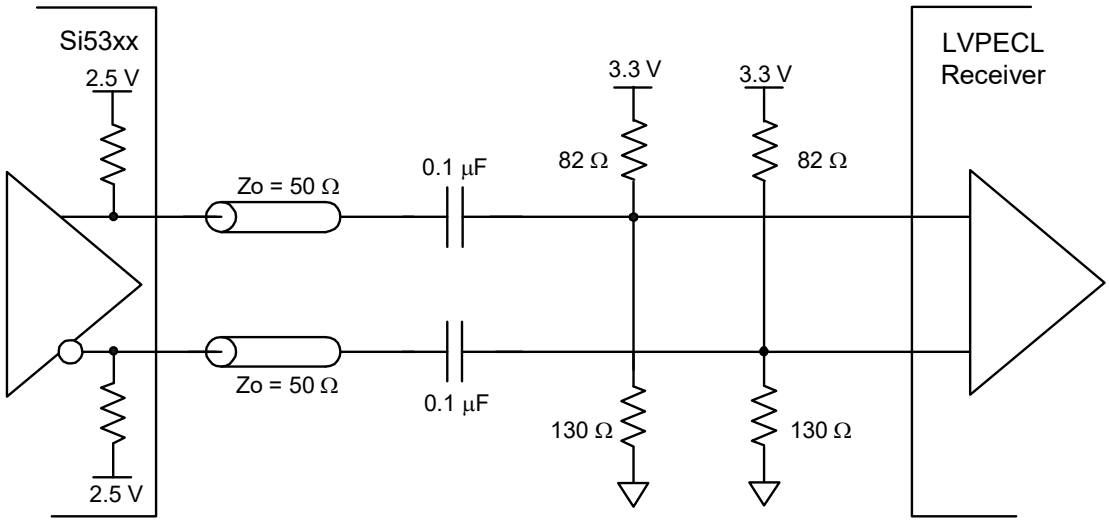
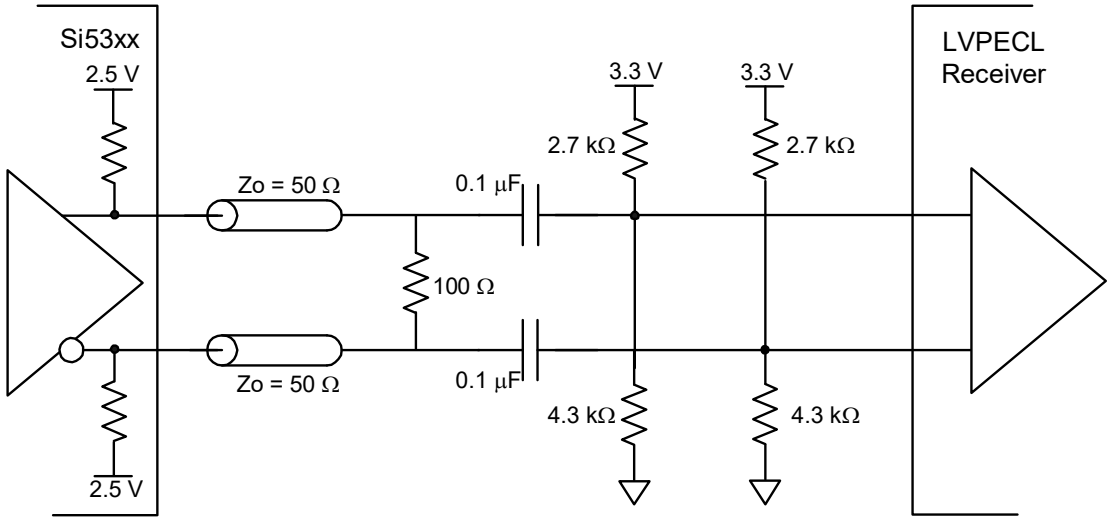


Figure 14. Typical Output Clock Termination



Standard LVPECL Termination
(a)



Modified LVPECL Termination
(b)

Figure 15. Example Output Clock Terminations to an LVPECL Receiver

2.3.5. LVTTL I/O Signals

The Si53xx family of ICs use LVTTL signals for digital control and status or alarm functions. These are single-ended quasi-static signals, which normally do not require filtering or termination. Simplified LVTTL input and output circuit schematics of the ICs are illustrated in Figures 16 and 17, respectively. In these figures, the on-chip current-limiting resistor, R, is hundreds of ohms,(e.g., 238 Ω) and the capacitor, C, is a few picofarads (e.g., 5.5 pF). Additional filtering is normally not required on the LVTTL I/O lines.

The LVTTL inputs on the Si53xx have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source. For LVTTL inputs that need to be tied high and remain unchanged for a given application, the inputs should be connected to the filtered side of the 3.3 V supply as shown in Figure 18.

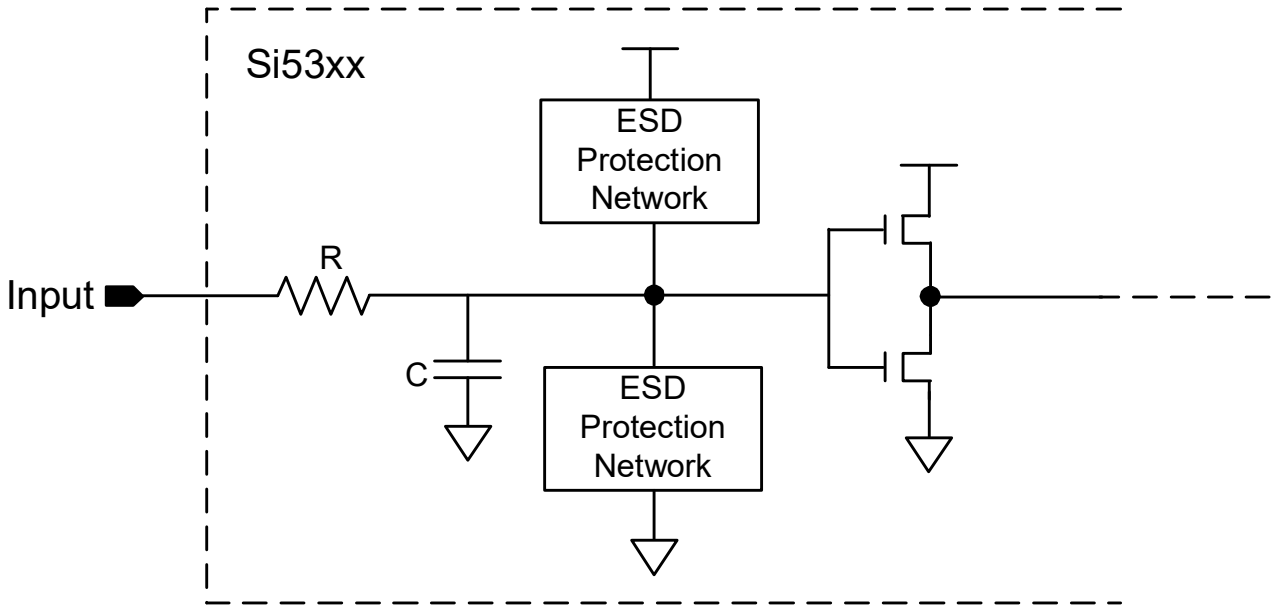


Figure 16. Simplified LVTTL Input Circuit

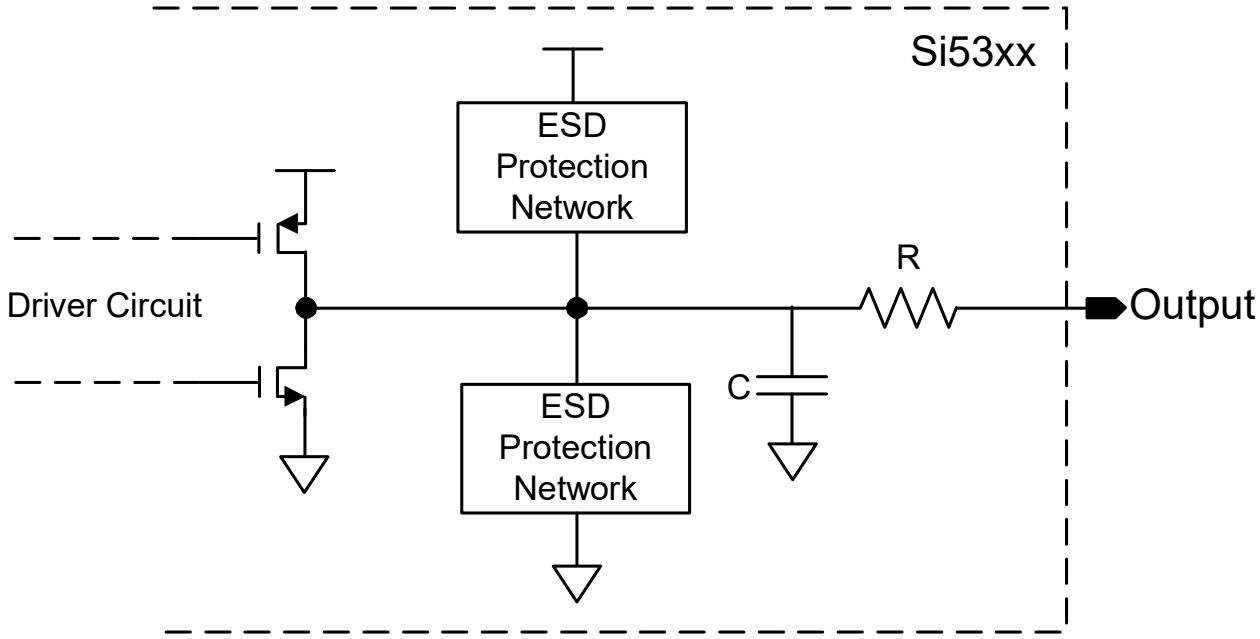


Figure 17. Simplified LVTTL Output Circuit

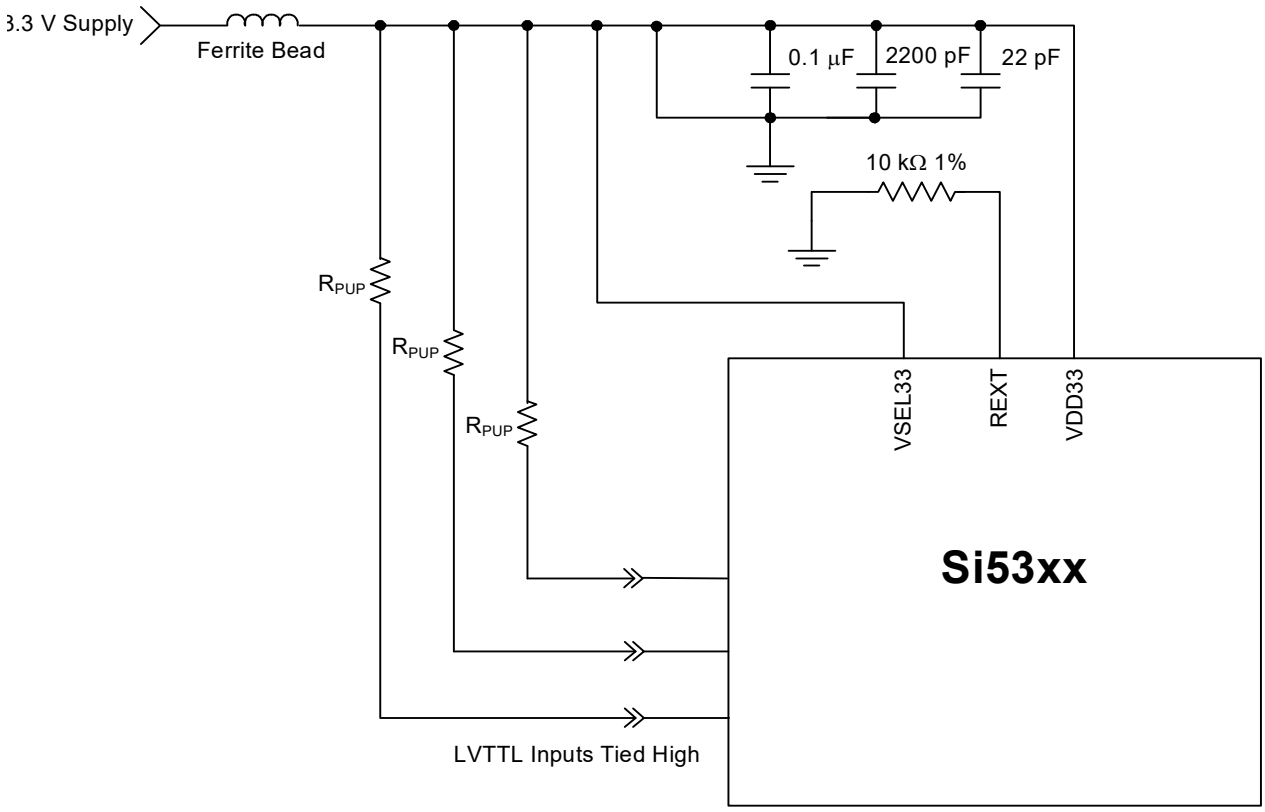


Figure 18. Terminating High State LVTTL Signals

2.4. Minimizing Electromagnetic Noise Coupling

Each Si53xx clock device is built around a high-quality L-C voltage-controlled oscillator (VCO) circuit that provides excellent phase noise performance. Because this LC-VCO is a high-quality, high precision circuit, care must be taken to avoid electromagnetic coupling of external noise sources into this circuit as this can degrade its performance. The LC-VCO inside the clock devices operates in the range of 2487.8 MHz to 2774.8 MHz, depending on the frequency of the input clock(s) and the FEC settings of the device. (See the individual part's data sheet for specified minimum and maximum frequencies of operation.)

The EMI coupling condition that creates the most SONET in-band jitter in OC-48 systems is when a nearby device operates anywhere in the range from f_{BW} to 12 kHz offset from the frequency of the LC-VCO, where f_{BW} is the PLL bandwidth setting of the affected Si53xx device. Likewise, the worst case for OC-192 systems is when a nearby device operates anywhere in the range from f_{BW} to 50 kHz offset from the frequency of the LC-VCO.

The dominant coupling mechanism by far is conducted coupling from the device pins (e.g., the 2.5 V power supply pins, the LVTTL output pins, and the clock input pins) to the LC-VCO. Through proper board layout and signal routing techniques, it is possible to minimize these coupling paths so that their impact on the device's output phase noise becomes negligible relative to the device's inherent phase noise generation. The recommended layout guidelines for minimizing these noise coupling paths are given in the following section, "2.4.1. Layout Guidelines for Minimizing Noise Coupling" .

Skyworks' applications engineering will review your application's schematic and layout free of charge. Please contact us if you would like to take advantage of this service.

2.4.1. Layout Guidelines for Minimizing Noise Coupling

1. Route clock input signal and output signals on a dedicated board layer sandwiched between two ground planes. Do not share this board layer with any other nearby signals that could couple to the clock lines. Route clock inputs and outputs differentially when possible.
2. Use a small 2.5 V power island for connecting the 2.5 V device supply pins. Place this 2.5 V island between two ground planes.
3. Route all LVTTL I/O signals between ground planes so that they cannot couple ambient EMI back into the device.
4. An example 8-layer board stack-up (used in our latest evaluation boards), which has been shown to deliver good performance, is as follows:
   - Ground Plane (Component Side)
   - Differential Clock Inputs and Outputs
   - Ground Plane
   - 2.5 V Island
   - Ground Plane
   - 3.3 V Supply
   - LVTTL I/Os
   - Ground Plane (Solder Side)

Document Change List

Revision 0.3 to Revision 0.4

- Updated “2. Recommendations for New Designs” section.
- Updated “2.3. Input/Output Interfacing and Signal Conditioning” section.
- Updated “2.3.2. Si53xx Differential Clock Interfacing: An example application” section
- Removed “Injection Lock” section.
- Updated “2.3.3. Input Clock Signals” section.
- Updated “2.3.4. Output Clock Signals” section.
- Removed Figure 15 “Example Filtered Output Clock Termination”.
- Updated “2.3.5. LVTTL I/O Signals” section.
- Removed Figure 18. “Example Schematics for LVTTL I/O Filters”.
- Removed Figure 19. “Example Layout for LVTTL I/O Filters”.
- Updated “2.4. Minimizing Electromagnetic Noise Coupling” section.
- Removed “Shield Recommendations for Eliminating Electromagnetic Noise Coupling Directly into the LC-VCO” section
- Removed Table 1 “BMI Shield Part Numbers”.

Revision 0.4 to Revision 1.0

- Added Si5318 typical application circuit.
- Updated “2.3.5. LVTTL I/O Signals” section.

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