THERMAL ANALYSIS OF SKYWORKS SOLUTIONS' TIMING DEVICES

1. Introduction

The junction temperature of semiconductor devices affects reliability and performance of Integrated Circuits (ICs), including timing devices. This application note provides the following:

1. A definition of the thermal problem in ICs.
2. Basics of heat transfer from ICs.
3. IC level Solutions to thermal problems.
4. System level Solutions to thermal problems.
5. System level thermal solutions recommended for different timing ICs in the Skyworks Solutions timing product family.
6. Appendix
   a. Definitions of terms used in this application note.
   b. Standard information pertaining to Skyworks Solutions timing devices.
   c. References

1.1. A Definition of the Thermal Problem in ICs

The temperature of PN junctions in an IC tend to increase due to the self-heating of the IC (the IC dissipates power as heat). The temperature of the PN junction affects reliability (The voltage and/or current stress that a diode can withstand without a junction breakdown) and can lead to breakdown of the junction when the temperature is high enough. The solution to the above problem is that the heat generated by the IC should be transported out of the IC to the environment efficiently. This will keep the junction "cool" and the IC reliable.

1.2. Basics of Heat Transfer from ICs

Heat flows from the junction(s) of an IC into the external environment in two major paths (as shown in Figure 1).

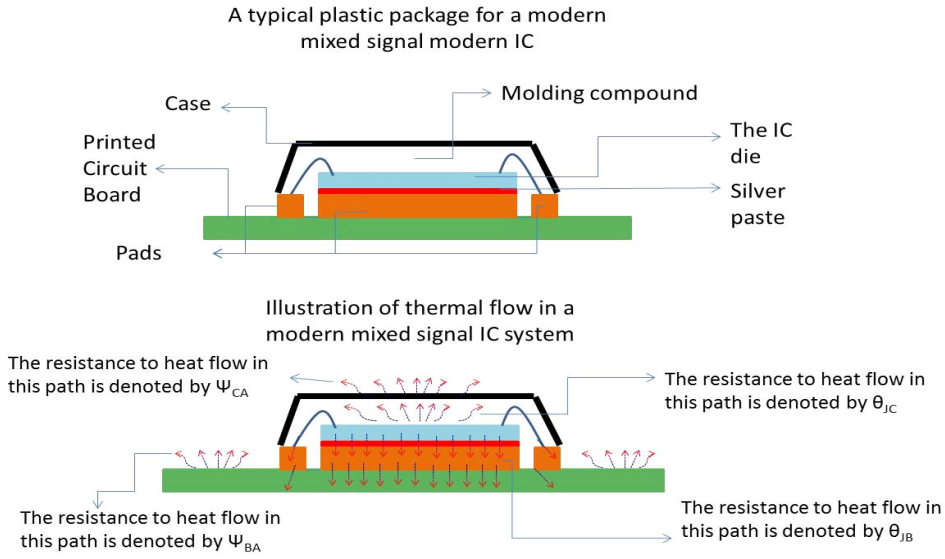

Figure 1. Thermal Flow in a Typical Mixed-Signal IC System

The major paths of heat flow in an IC system are as follows:

- Heat flow from junction to ambient through the top case.
- Heat flow from junction to ambient through the PCB (Printed Circuit Board).

The thermal resistances for the paths of heat flow can be modeled as equivalent electrical resistances and the entire thermal system can be viewed as an analogous electrical system. The advantage of using an electrical model is that it makes the construction of the problem simpler and visualization of the solutions to the problem clearer (especially to electrical engineers).

Table 1. Thermal Parameter and its Electrical Counterpart

Thermal Parameter	Electrical counterpart in Electrical Model
Heat Source	Current Source
Temperature of a point	Voltage at the corresponding node.
Thermal resistance	Electrical resistance

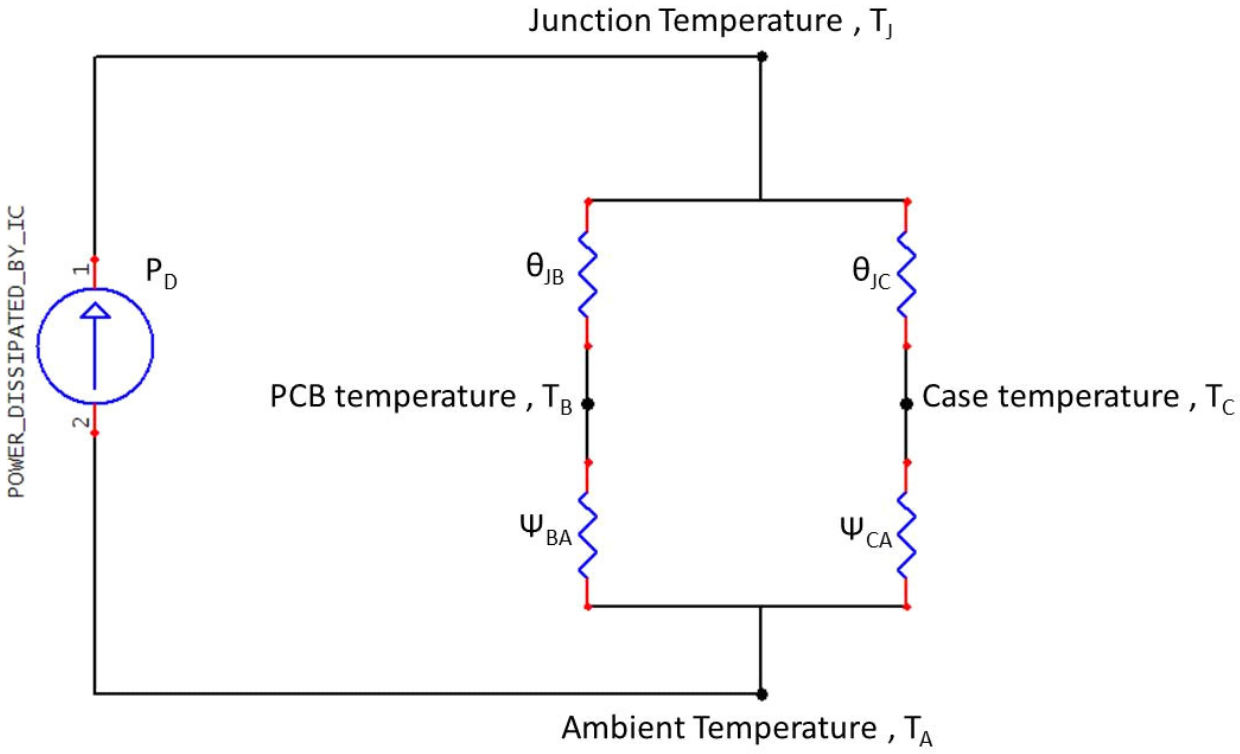

Figure 2. Electrical Model of the Thermal Problem

After applying the transformations from the thermal domain into the electrical domain (as from Table 1 and Figure 2), it becomes quite straight forward for us to calculate T_J.

$T_J = T_A + P_D \times \{(\theta_{JB} + \psi_{BA}) \,||\, (\theta_{JC} + \psi_{CA})\}$*

If we treat TJ as a voltage, it becomes clear that in order to minimize T_J, the total thermal resistance must also be minimized. The next few sections outline the steps taken at IC level to minimize the total thermal resistance and the steps that can be taken at a system level to minimize the total thermal resistance. As a general demarcation, θ's can be taken care of at IC level and ψ's can be taken care of at system level.

***Note:** Distinction between θ's and ψ's:

- Thermal resistance denoted by θ is applicable when all the paths for heat flow between points A and B are known.
- Thermal resistance denoted by ψ is applicable when not all the paths for heat flow between points A and B are known.

1.3. IC level Solutions to Thermal Problems

This section explores the different mechanisms by which θ_{JB} and θ_{JC} can be minimized at IC level.

Controlling θ_{JB}:

At IC level, the following knobs control (or minimize) θ_{JB}:

1. The mechanism by which an IC pad is connected to the package pin (BGA, Flip chip, wire bonding in general plastic packages, etc.). The larger the connecting mechanism, the better the thermal conduction.
2. The size of the IC pads, larger the IC, the better the conduction.
3. The Package pin dimension and material composition.

While the material choice is largely determined by considerations that take higher precedence over thermal performance, the various sizes involved generally shrink over time implying a definite degradation in thermal performance as far as θ_{JB} is concerned.

In order to improve θ_{JB}, modern ICs provide a large thermal relief pad. This provision generally outweighs the other dis-advantages significantly.

Controlling θ_{JC}:

θ_{JC} is a function of the package choice and package choices are largely determined by other factors such as reliability and cost. Therefore, θ_{JC} is not (and cannot be) always optimized.

1.4. System level Solutions to Thermal Problems

This section explores the different mechanisms by which ψ_{BA} and ψ_{CA} can be minimized at system level.

Factors controlling ψ_{BA}:

The main factor that controls ψ_{BA} is the path the heat takes in the PCB. Copper is a better conductor compared to FR4 (the standard dielectric material used in PCBs). Therefore for the best possible ψ_{BA}, the IC will need access a large copper layer. Also, thicker copper layers (70 micron thickness) offer better thermal conductivity. Usually this factor takes lesser precedence over ψ_{BC} in thermal design (which we explore in next section) but with use of E-pads in ICs, it is imperative that ψ_{BA} is also optimally designed to take advantage of the lower θ_{JB} in certain ICs. The use of controlled air flow (i.e., cooling fans) also helps reduce ψ_{BA} significantly.

Factors controlling ψ_{CA}:

The three most important factors that control ψ_{CA} directly are the use of heat sinks, the use of cooling fans and the use of fluids to cool the case in certain ICs. These three tools (especially the first two) are the primary tools available to reduce ψ_{CA} significantly. Generally air flow has the impact of reducing the θ_{JA} by 15–20% in systems as shown in Figure 3:

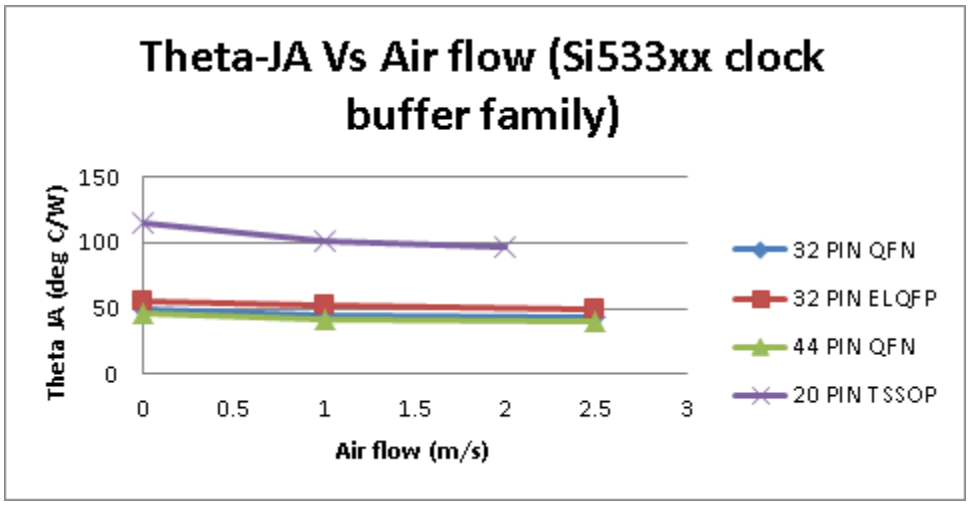

Figure 3. θ_{JA} vs. Air Flow for the Si533xx Devices

1.5. Recommended System Level Thermal Solutions

Skyworks Solutions' timing portfolio covers a wide range of ICs in terms of packaging, power consumption and power density. The power density of Skyworks Solutions' timing devices is shown in Figure 3.

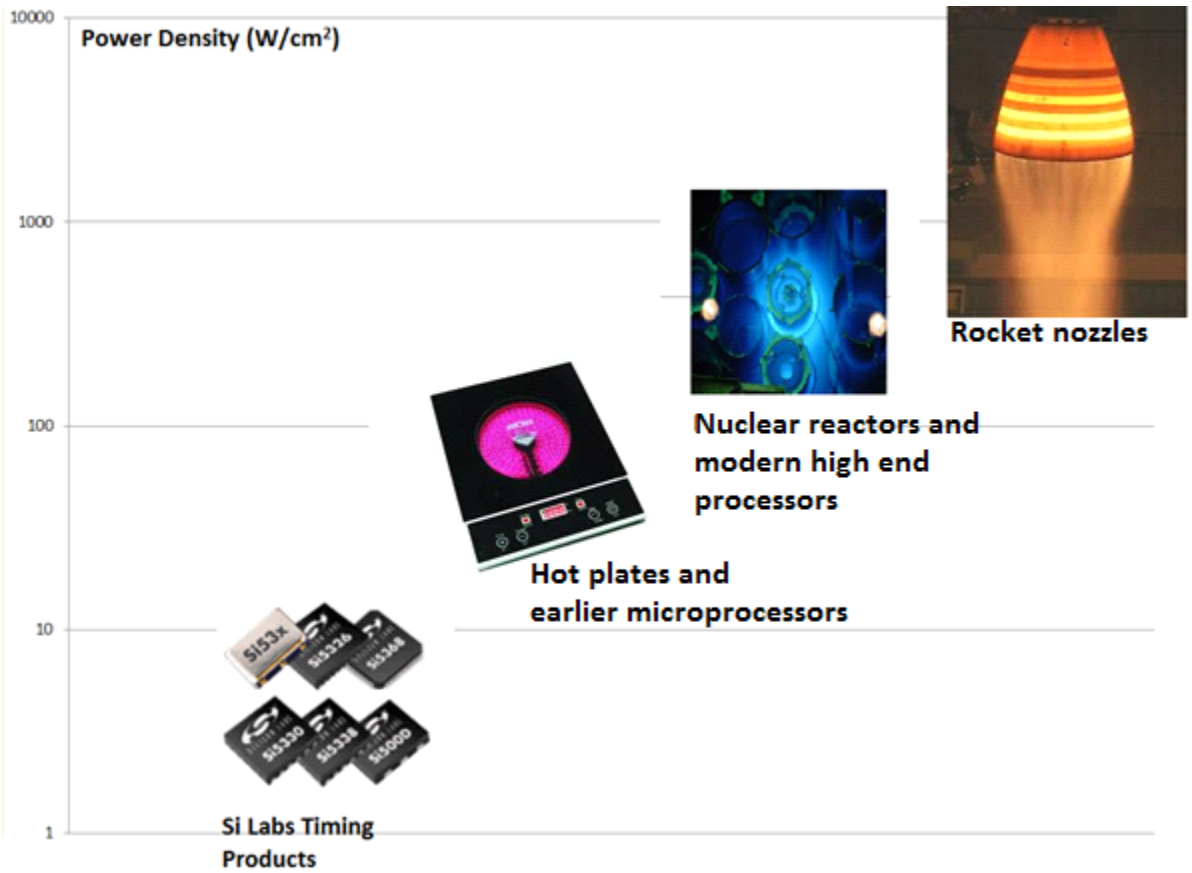

Figure 4. Power Density of Skyworks Solutions Devices vs. Other Common Heat Sources

Skyworks Solutions timing products have thermal density ~10–15 W/cm^2 which is not quite as hot as a hot plate or modern micro-processors Therefore, most of the thermal management problems related Skyworks Solutions timing products can be solved using relatively simpler thermal solutions like board design, air flow, etc. and rarely require additional solutions like heat sinks, liquid cooling, etc.

Table 2. θ_{JB}, θ_{JB}, and $P_{D\text{-}MAX}$ for Skyworks Solutions Timing Devices

Product family	Product (PN)	Package	PCBs used for simulation	Theta-JB	Theta-JC	Theta-JA (Still Air)	Max. Power (mW)
Oscillators	Si510/511	CLCC (5 mm x 7 mm)	4 layers (2S2P), 4” x 4.5	61.2	60.5	110	160
	Si512/513			61.2	60.5		
	Si514			61.2	60.5		
	Si530/531			39.5	38.8		439
	Si532			39.5	38.8		
	Si533			39.5	38.8		
	Si534			39.5	38.8		
	Si570			39.5	38.8		476
	Si590/591			39.5	38.8	84.6	454
	Si598/599			39.5	38.8	84.6	476
Clock Generators	Si5334	24-Pin QFN	4 layers (2S2P), 4” x 4.5	23.4	26	45.4	327
	Si5335	24-Pin QFN					
	Si5338	24-Pin QFN					
	Si5356	24-Pin QFN	4 layers (2S2P), 4” x 4.5	23.4	26	45.4	327

Table 2. θ_{JB}, θ_{JB}, and $P_{D\text{-}MAX}$ for Skyworks Solutions Timing Devices (Continued)

Clock Buffers	Si53301	32-Pin QFN	3” x 4.5”, 2L, 1.6 mm thick	28.6	32.3	49.6	1000
	Si53302	44-Pin QFN		28	27.1	46.2	1000
	Si53303	44-Pin QFN		28	27.1	46.2	1000
	Si53304	32-Pin QFN		28.6	32.3	49.6	1000
	Si53305	44-Pin QFN		28	27.1	46.2	1000
	Si53311	32-Pin QFN		28.6	32.3	49.6	1000
	Si53312	44-Pin QFN		28	27.1	46.2	1000
	Si53313	44-Pin QFN		28	27.1	46.2	1000
	Si53314	32-Pin QFN		28.6	32.3	49.6	1000
	Si53315	44-Pin QFN		28	27.1	46.2	1000
	Si53320	20-Pin TSSOP		62.4	30.6	115.2	500
	Si53321	32-pin QFN		28.6	32.3	49.6	1000
	Si53321	32-Pin-ELQFP		37.2	38	54.9	1000
	Si53325	32-pin QFN		28.6	32.3	49.6	1000
	Si53325	32-Pin-ELQFP		37.2	38	54.9	1000
Jitter Attenuators	Si5317	36-Pin QFN	4L , 3” X 4.5” , 1.6 mm thick	20	14	32	1013
	Si5323	36-Pin QFN			14	32	1013
	Si5326	36-Pin QFN			14	32	1013

Based on the above data, a system engineer can estimate the improvements in systems thermal characteristics needed to maintain a given junction temperature at a given ambient temperature for a given Skyworks Solutions clock IC.

Example 1:

The following example illustrates the calculated ψ_{BA}, ψ_{CA} to keep the junction temperature less than 120 °C of junction temperature at an ambient temperature of 85 °C for Si53302. Furthermore, we assume that the Si53302 is running at maximum power (1000 mW).

For this example, θ_{JA} desired at these conditions is given by the following:

$(\theta_{JA})DESIRED = (T_J - T_A)/PD = (120\text{-}85)/1000\ mW = 15/1\ deg\ C/W = 35\ deg\ C/W$

$(\theta_{JA})DESIRED = (\theta_{JA})STILLAIR \times 0.756$ i.e., we need to reduce the (θ_{JA}) of the Si53302 by ~24% to get the desired thermal performance.

This translates into the following:

$(\theta_{JA})DESIRED = 1/\{(1/\theta_{JB} + \psi_{BA}) + 1/(\theta_{JC} + \psi_{CA}\}$

If we decide to improve thermal resistance primarily via air flow and assume that $\psi_{BA} \approx \psi_{CA} \approx \psi$, we get the following:

$\psi \approx 2 \times (\theta_{JA})DESIRED - \{\theta_{JB} + \theta_{JC}/2\} = 42.5\ °C/W$

For the standard JEDEC test, $\psi \approx 65\ °C/W$

Therefore, we require the system thermal parameters to improve by a factor of 35% to get to the desired θ_{JA}. An important parameter will be the amount of ground plane that is connected to the E-pad underneath the device. The JEDEC thermal PCBs have at least 75% plane coverage below the device and the same metric is recommended to optimize the thermal performance in real applications, i.e. At least 75% of the area underneath the Si53302 device and directly connected to the E-pad of the Si53302 should be a continuous ground plane.

An even more important factor is the air flow and in order achieve (θ_{JA})DESIRED = 35 °C/W, the Si53302 device needs an air flow of ~4.1 m/s. This air flow requirement is calculated for a 2-Layer PCB based on JEDEC standard for thermal calculations. The air flow requirement in an actual application depends on the thermal characteristics of the PCB used.

Example 2:

What is the highest temperature one can operate a system with a Si53302 device at full power?

Refer to Figure 2. If we get $\psi_{BA} \approx \psi_{CA} << \theta_{JB}, \theta_{JC}$ (i.e., the thermal design of the PCB system is such that there is almost zero thermal resistance from the case and board to the ambient.)

In such a case we can get the minimum possible θ_{JA} which is given by the following:

$(\theta_{JA})\text{MINIMUM} = 1/\{(1/\theta_{JB}) + 1/(\theta_{JC})\} \approx 13.78$ °C/W.

The junction temperature TJ is given by the following:

$T_J = T_A + P_D \times (\theta_{JA})\text{MINIMUM}$

Therefore, T_A cannot exceed 106.22 °C to keep T_J less than 120 °C. This means that if we have a system that is near ideal in its thermal characteristics, there will still be an inherent limit on the maximum ambient temperature for ICs. In the case of the Si533xx buffer family, care must be taken when using the ICs for applications that will exceed ambient temperature of 85 degrees (Military applications are an example).

2. Conclusion

This application note introduces the basic thermal parameters and factors important for optimal thermal design in systems. These thermal parameters can be used by the designer to find out the specific cooling needs for a given timing device as illustrated in the two examples above.

3. Appendix

3.1. Term Definitions

θ_{JA} **thermal resistance, junction-to-ambient**: the thermal resistance from the operating portion of a semiconductor device to a natural convection (still-air) environment surrounding the device.

θ_{JC} **thermal resistance, junction-to-case**: the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface; the package interface surface can be on either the top or bottom of the package.

θ_{JB} **thermal resistance, junction-to-board**: the thermal resistance from the operating portion of a semiconductor device to the Printed Circuit Board that houses the device.

ψ_{BA} **thermal characterization parameter**: parameter characterizing the behavior of the package. While the units are °C/W, they are not resistances because the temperature difference is divided by the total power, not the power flowing between the board and the ambient.

ψ_{CA} **thermal characterization parameter**: parameter characterizing the behavior of the package. While the units are °C/W, they are not resistances because the temperature difference is divided by the total power, not the power flowing between the board and the ambient

3.2. Skyworks Solutions Timing Devices Standard information

- Max TJ = 125 °C (unless other noted in the device data sheet).
- Skyworks Solutions typically reports only θ_{JA}, θ_{JB}, θ_{JC} based on thermal simulation.

3.3. References

- http://powerelectronics.com/thermal_management/thermal_management_simulation/803PET21.pdf
- http://www.ece.umn.edu/~sachin/jnl/FnT08.pdf
- http://www.jedec.org/sites/default/files/docs/jesd51-12.pdf
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- http://www.jedec.org/sites/default/files/docs/JESD51-13.pdf

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