AN862: Optimizing Jitter Performance in Next-Generation Internet Infrastructure Systems

To realize 100 fs jitter performance of the Si534x jitter attenuators and clock generators in real-world applications, designers should consider a few simple guidelines to minimize crosstalk and optimize overall jitter performance. These guidelines apply to frequency synthesis of any high-speed clock generator.

Whenever a number of high frequency, fast rise time, large-amplitude signals are close to one another, there will be some amount of crosstalk between them. The jitter of the Si534x family is so low that what used to be relatively minor crosstalk is now a non-trivial portion of the final measured output jitter. The source of some of the crosstalk will be due to the Si534x device and some will be introduced by the PCB. It is difficult to allocate the jitter portions between the two sources because the jitter can only be measured when the Si534x is mounted on a PCB. This application note provides simple guidelines to enable designers to optimize jitter performance.

KEY POINTS

- Select differential output format options
- Order clocks carefully by avoiding placement of clocks beside each other if they are within the integration bandwidth (eg., 12 kHz to 20 MHz)
- Separate clocks with unused outputs
- Avoid using CMOS output formats in jitter-critical applications
- Consider reducing the output swings and I/O voltages
- Use the Clock Placement Wizard in ClockBuilder Pro
- Contact Skyworks if you need more information

APPLIED DEVICES

- Si534x
- Si539x

1. Four Simple Rules for Optimal Jitter Performance

1.1 Select the Differential Output Options (LVDS, LVPECL, HCSL)

Differential outputs produce balanced, complementary output signals designed to yield the best jitter performance. These differential signal formats also inherently produce minimal common mode noise (minimizing EMI), and they generally consume less power than CMOS formats.

1.2 Order the Output Clocks Carefully

One of the easiest ways to reduce crosstalk is to arrange the clock outputs so clocks that are more likely to experience crosstalk between one another are not physically located next to one another. For networking applications, jitter integration bandwidths typically come from the relevant communications standards that are important to the end system. Jitter outside of the integration bands is considered to not be an issue. The details of the integration band will differ from application to application and from standard to standard. The commonly used, default integration band of 12 kHz to 20 MHz comes from SONET OC-48 and is used in the following example:

If two adjacent clock outputs are closer to each other than 20 MHz (the extent of the jitter integration band), then there might be crosstalk issues. Consider the example of a 155.52 MHz clock output next to a 156.25 MHz clock output. Since 156.25 MHz – 155.5222 MHz = 730 kHz, the mixing differences between the two will be well within the 12 kHz to 20 MHz jitter mask band. Therefore, the designer should avoid placing a 155.52 MHz clock next to an 156.25 MHz clock.

Note that this integration bandwidth proximity placement guideline does not apply to clocks that are simple integer multiples of one another. For example, a 125 MHz clock can be located next to a 625 MHz clock because 125 MHz * 5 = 625 MHz. The simple integer relationship means that the edges of one clock will not be moving with respect to the edges of the other clock.

1.3 Separate Clocks with Unused Outputs

Unused clock outputs can be used to physically separate clocks that would otherwise interfere with one another. For example, if there is an unused clock output, it can be placed between a 155.52 MHz and a 156.25 MHz clock to physically separate them. Table 1 shows the benefits of rearranging the used output clocks and strategically placing unused output clocks to improve jitter. In this example, a ten output Si5345 was programmed in two different ways: one ignores the recommendations for rearranging clock outputs and the other takes them into account. The jitter was integrated from 12 kHz to 20 MHz and all of the outputs are LVDS at 2.5 V. Clearly, rearranging the outputs lowers the jitter and results in high performance at all outputs. See Appendix A to view the phase noise plots that generated the data.

Table 1.1. Impacts of Output Clock Ordering on Jitter Performance

	Sub-optimal Clock Ordering		Optimal Clock Ordering	
Output	Frequency (MHz)	Jitter (fsec RMS)	Frequency (MHz)	Jitter (fsec RMS)
0	155.52	269	155.52	101
1	156.25	439	155.52	104
2	155.52	411	622.08	92
3	156.25	186	not used	
4	200	123	156.25	121
5	100	165	156.25	119
6	622.08	92	625	102
7	625	103	not used	
8	not used		200	122
9	not used		100	100

1.4 Avoid Using CMOS Output Formats in Jitter Critical Applications

- Because CMOS output buffers swing rail-to-rail and are not balanced (unlike such output formats as LVPECL, LVDS, CML, and HCSL), CMOS outputs create significant current surges at all of the clock edges and, therefore, are prime crosstalk aggressors. For this reason, CMOS outputs should be avoided whenever possible for jitter sensitive applications.
- When CMOS formats must be used, the CMOS clocks should be “quarantined” and kept away from critical clock outputs that are not the same frequency.
- Select the "complementary" output option (instead of the in-phase option) in ClockBuilder Pro to help balance the output current surges during transitions.
- If one of the output sides of the CMOS pair is unused but actively toggling, do not terminate the load.
- Consider using an external, low-jitter, differential mode to CMOS buffer (seehttps://www.skyworksinc.com/en/Products/Timing-Clock-Buffers). Place the buffer away from the Si534x device on the PCB to avoid coupling.

2. Spurs, Jitter Integration Band, and Harmonics

Jitter performance degrades when nearby clock outputs couple into an output clock. As an example, consider that a 155.52 MHz clock output is located next to a 156.25 MHz clock output. The difference in frequency between the two is 156.25 MHz – 155.52 MHz = 730 kHz. As a result, there is a spur located at 730 kHz off of the 155.52 MHz carrier, corresponding to the first harmonic that is labeled “1st” in Figure 1. As expected with a square wave produced by a CMOS output clock, the second harmonic is significantly smaller, which is located at 2 * 730 kHz = 1.46 MHz off of the carrier and is labeled “2nd”. The third harmonic is larger than the second but not as large as the first. It is located at 3 * 730 kHz = 2.19 MHz and is labeled “3rd”. Because all of these and the other harmonically related spurs are located within the 12 kHz to 20 MHz jitter integration band, they all can contribute to degrading the jitter performance (shown in Table 1) for differential output clocks. The magnitude of this degradation (which can be hundreds of femtoseconds when CMOS clocks couple to other CMOS clocks) is dependent on many factors, among them I/O voltage, signal format, and PCB layout.

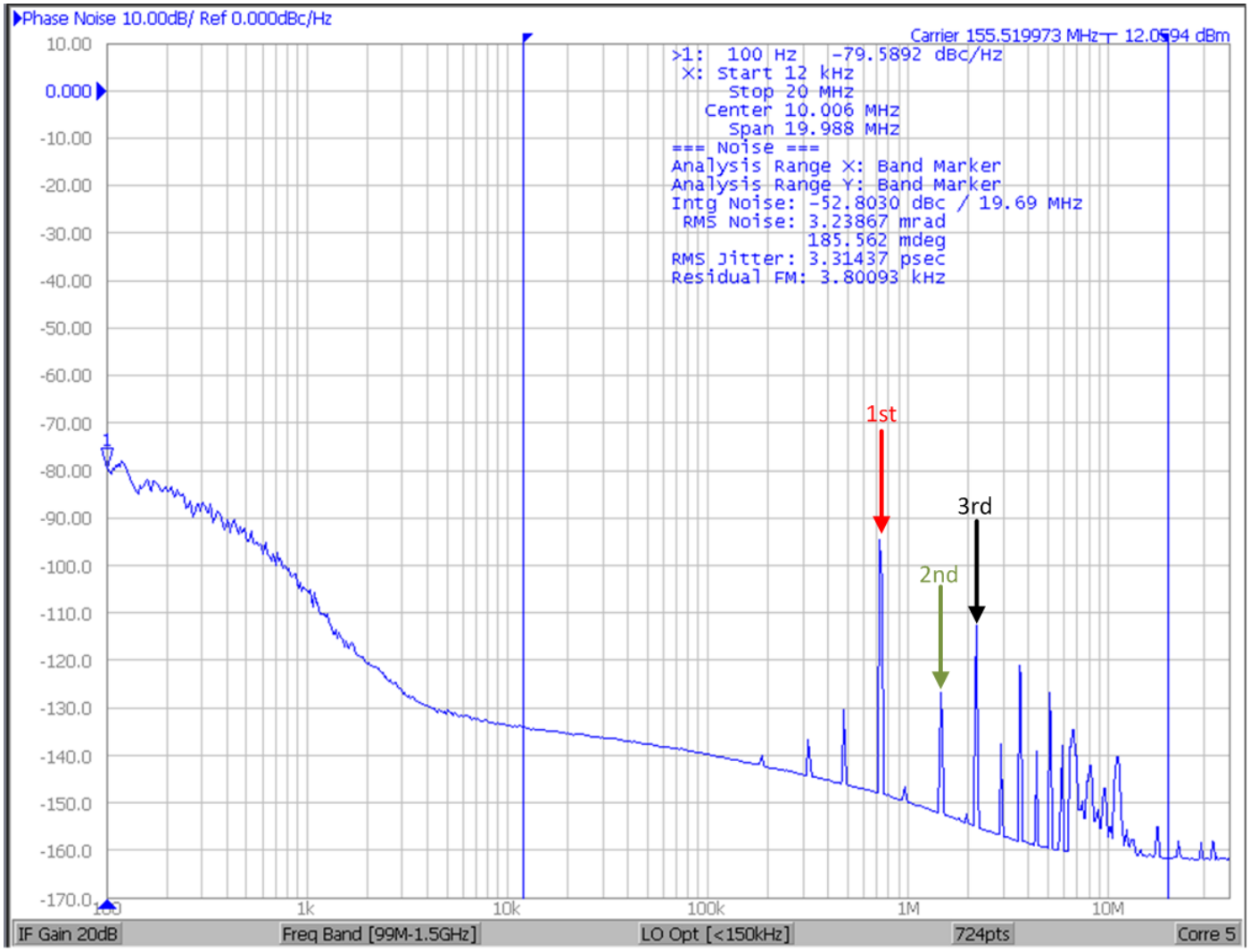

Figure 2.1. Spurs and Harmonics Example for CMOS to CMOS Outputs

3. Conclusion

By following the basic guidelines in this application note, designers can achieve 100 fs class jitter performance with the Si534x jitter attenuators and clock generators. For clocks that demand this level of jitter performance, designers should:

- Select differential formats for all jitter-sensitive clocks.
- Order the output clocks carefully (by frequency and integration bandwidth proximity).
- Separate coupling-sensitive clocks by placing unused outputs between outputs.
- Choose CMOS format only for clocks where jitter performance is not critical.

The ClockBuilder Pro Software has a built-in Clock Placement Wizard, which automatically takes the frequency plan and optimizes the output placements for minimized jitter. For more information on the Clock Placement Wizard, see “AN898: Optimizing Jitter Performance Using the CBPro Clock Placement Wizard”.

4. Appendix—Phase Noise Plots

The following phase noise plots apply to Table 1.1 Table 1 on page 2. The phase noise equipment used was the Agilent E5052B Signal Source Analyzer connected to a Skyworks Si5345-EVB (evaluation board) with a 48 MHz crystal as the XAXB reference. The differential signals had a Pulse Engineering CX2156 balun between the evaluation board and the E5052B. For the plots, all of the clock outputs were 2.5 V LVDS.

Recommended, differential

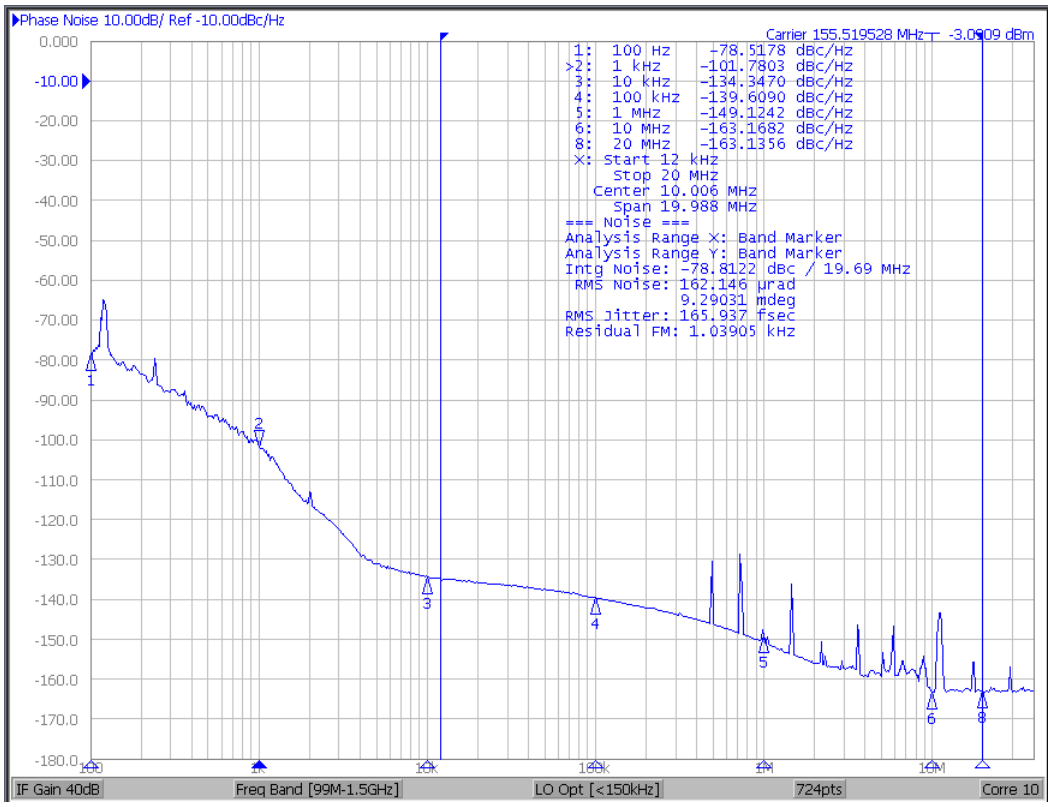

Figure 4.1. Recommended, LVDS, Output 0

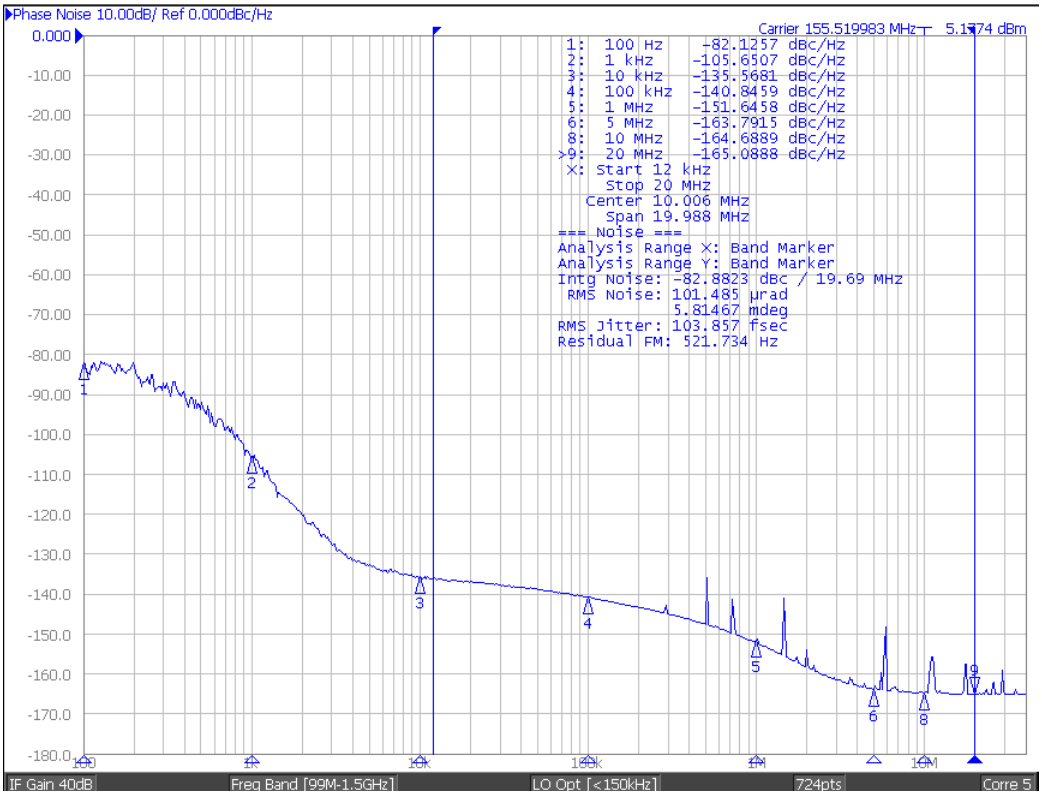

Figure 4.2. Recommended, LVDS, Output 1

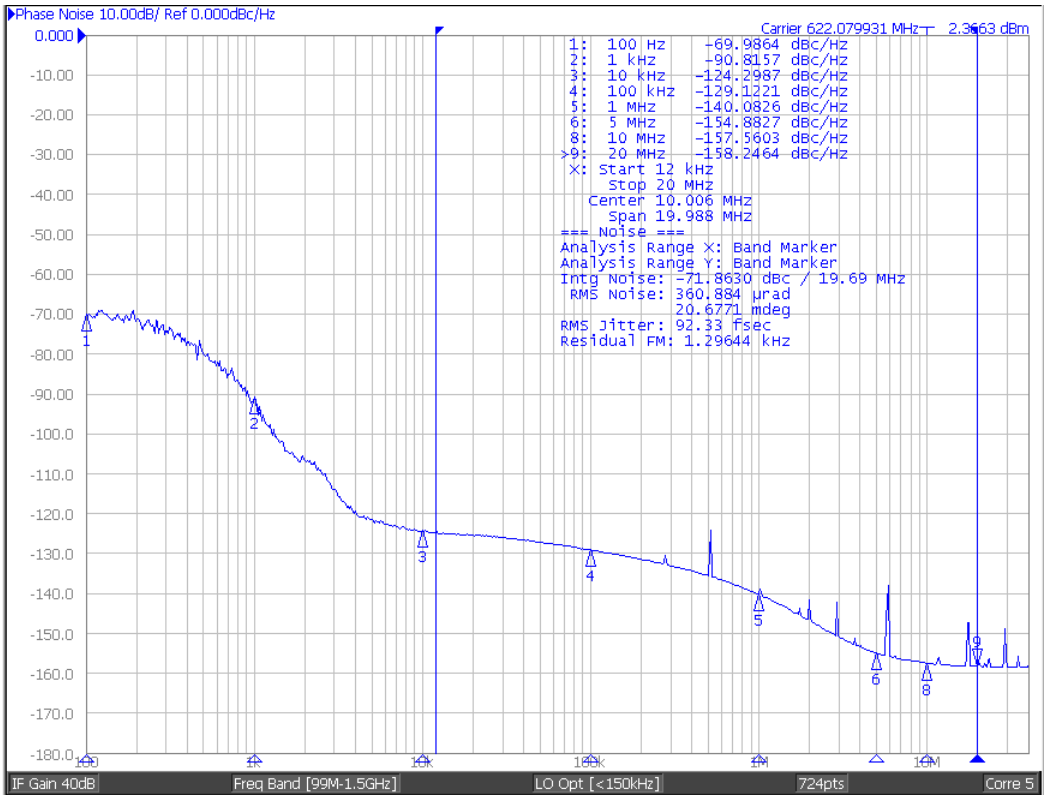

Figure 4.3. Recommended, LVDS, Output 2

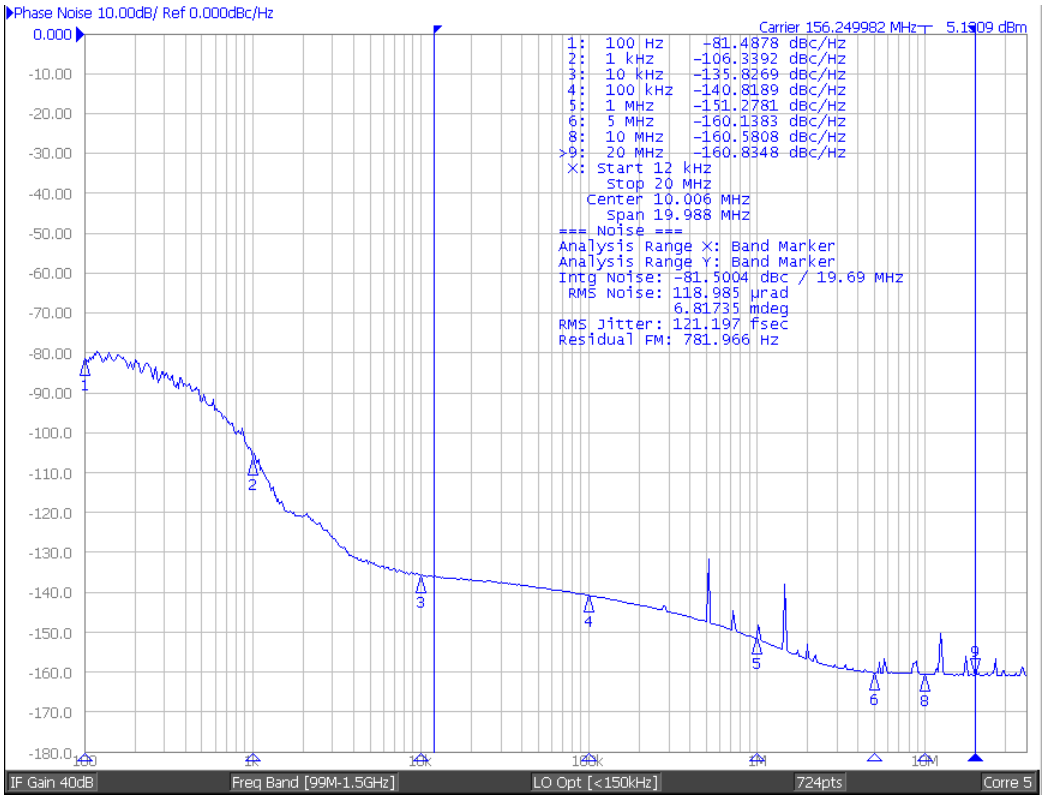

Figure 4.4. Recommended LVDS, Output 4

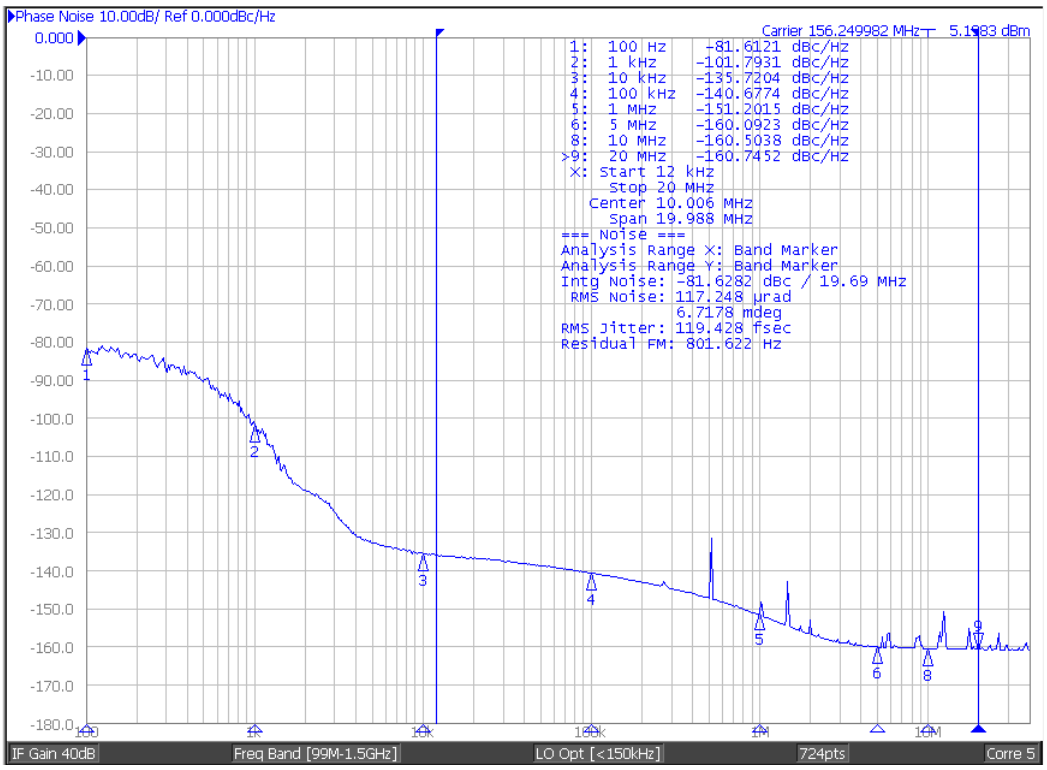

Figure 4.5. Recommended LVDS, Output 5

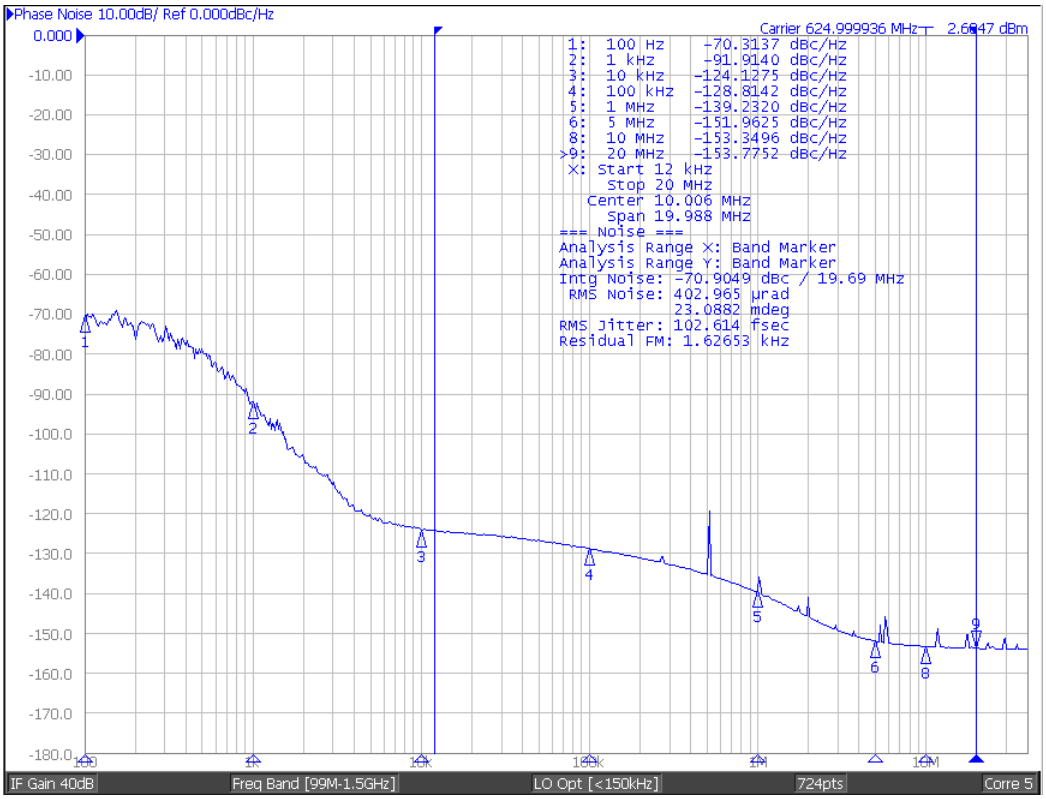

Figure 4.6. Recommended LVDS, Output 6

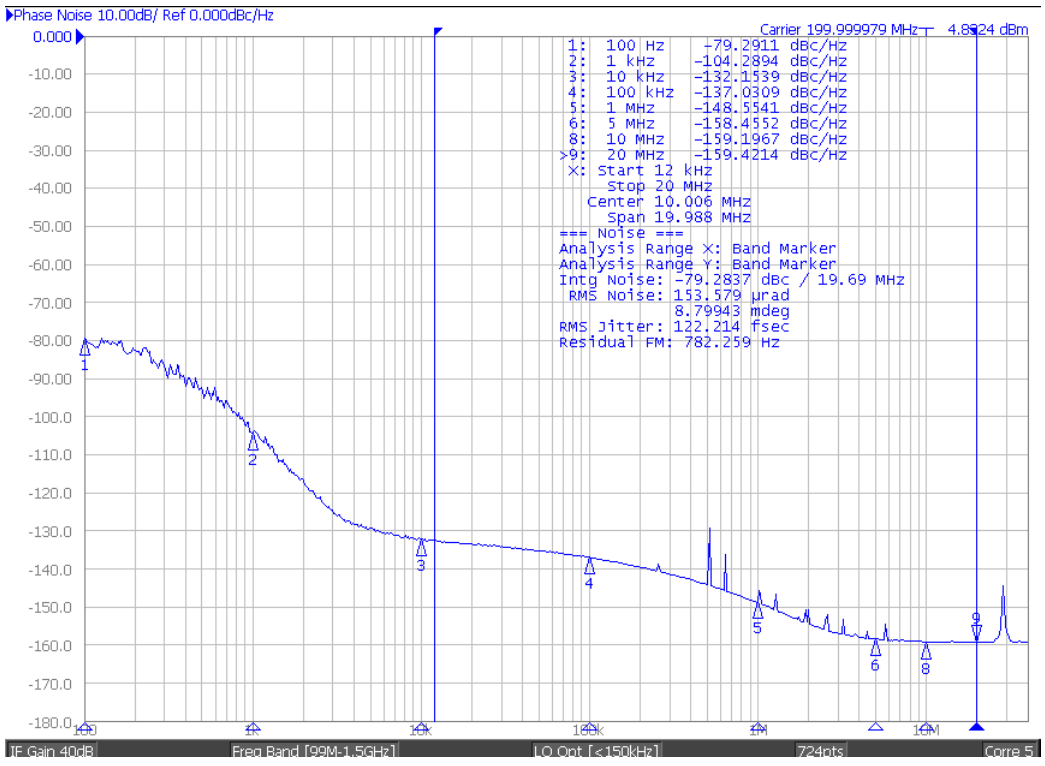

Figure 4.7. Recommended LVDS, Output 8

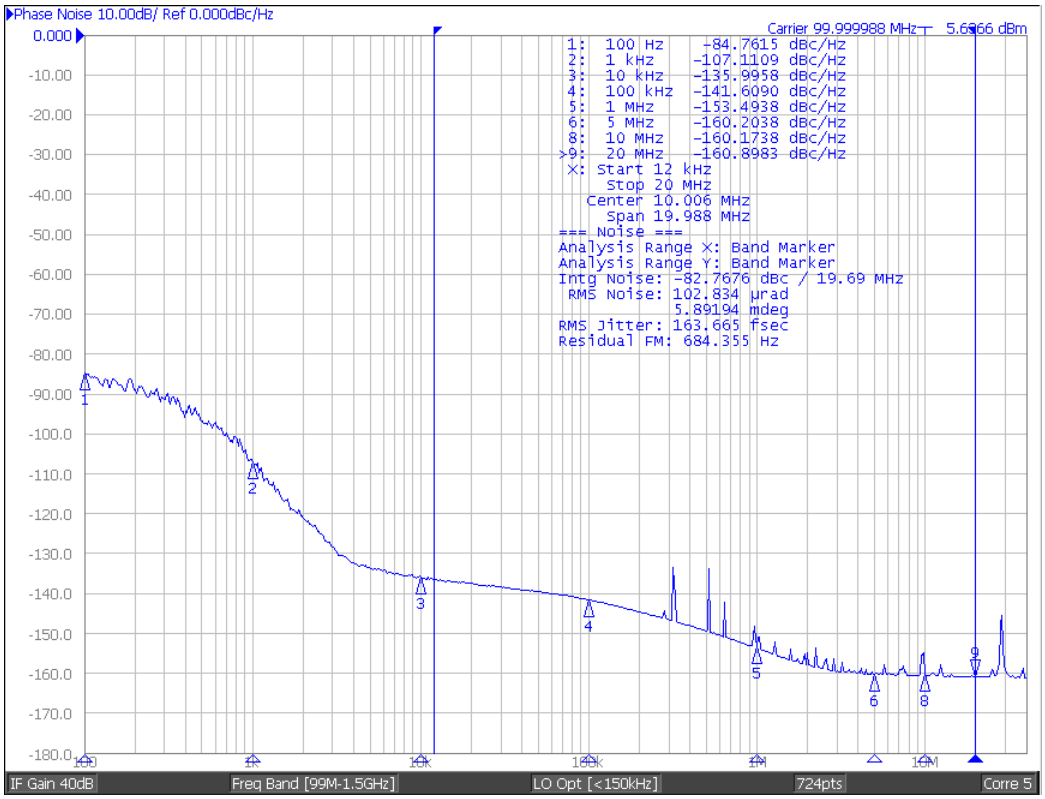

Figure 4.8. Recommended LVDS, Output 9

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