Si5348 Revision D Reference Manual

This Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5348 devices in end applications. The official device specifications can be found in the Si5348 datasheet.

The Si5348 is a high performance jitter attenuating clock multiplier with capabilities to address Telecom Boundary Clock (T-BC), Synchronous Ethernet (SyncE), IEEE-1588 (PTP) slave clock synchronization, and Stratum 3/3E network synchronization applications. The Si5348 is well suited for both traditional and packet based network timing solutions. The device contains three independent DSPLLs of identical performance allowing for flexible single-chip timing architecture solutions. Each DSPLL contains a digitally controlled oscillator (DCO) for precise timing for IEEE 1588 (PTP) clock steering applications. The Si5348 requires both a crystal and a reference input. The TCXO/OCXO reference input determines the frequency accuracy and stability, while the crystal determines the output jitter performance. The TCXO/OCXO input supports all standard frequencies. The Si5348 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up with a known configuration. Programming the Si5348 is made easy with Skyworks' ClockBuilder Pro software available at https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software. Factory preprogrammed devices are available.

RELATED DOCUMENTS

- Si5348 Rev D Data Sheet: https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/Si5348-D-DataSheet.pdf
- Si5348 Rev D -EVB User Guide: https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/user-guides/Si5348-D-EVB.pdf
- Si534x/8x Jitter Attenuators Recommended Crystals, TCXO and OCXOs Reference Manual: https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si534x-8x-9x-recommended-crystals-rm.pdf
- Si5348-EVB Schematics, BOM & Layout
- IBIS models
- To download support files, go to: 16. Accessing Design and Support Collateral

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1. Scope

This Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5348 device in end applications. The official device specifications can be found in the Si5348 data sheet.

2. Overview

The Si5348 is a high performance jitter attenuating clock multiplier with capabilities to address Telecom Boundary Clock (T-BC), Synchronous Ethernet (SyncE), IEEE-1588 (PTP) slave clock synchronization, and Stratum 3/3E network synchronization applications. The Si5348 is well suited for both traditional and packet based network timing solutions. The device contains three independent DSPLLs of identical performance allowing for flexible single-chip timing architecture solutions. Each DSPLL contains a digitally controlled oscillator (DCO) for precise timing for IEEE 1588 (PTP) clock steering applications. The Si5348 requires both a crystal and a reference input. The TCXO/OCXO reference input determines the frequency accuracy and stability, while the crystal determines the output jitter performance. The TCXO/OCXO input supports all standard frequencies. Each DSPLL has access to IN0, IN1 and IN2, and the TCXO/OCXO reference input. These are the main inputs for synchronizing the DSPLLs. DSPLL D has access to two additional CMOS only inputs, IN3 and IN4. Each DSPLL can provide low jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency generation. Each DSPLL supports independent free-run and holdover modes of operation, and offers automatic and hitless input clock switching. The Si5348 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up with a known configuration. Programming the Si5348 is made easy with Skyworks' ClockBuilder Pro software available at https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software. Factory preprogrammed devices are available.

2.1 Work Flow Using ClockBuilder Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the devices in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to Applications Notes and Knowledge Base article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is to enable use of the device without an in-depth understanding of its complexities. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to an EVB and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

2.2 Product Family

The table below lists a comparison of the various Si5348 family members.

Table 2.1. Product Selection Guide

Part Number	# of Inputs	# of DSPLLs	Number of Outputs	Max Frequency	Package Type
Si5348A	5	3	7	720 MHz	64-pin QFN
S5348B	5	3	7	350 MHz	64-pin QFN

3. Functional Description

The Si5348 takes advantage of Skyworks fourth-generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. Each of the DSPLLs operated independently from each other and are controlled through a common serial interface. DSPLLs (A, C and D) all have access to any of the three inputs (IN0 to IN2), as well as the refernece (REF) after having been divided down by the P dividers, which are either fractional or integer. DSPLL D has access to two additional CMOS inputs (IN3 and IN4). Clock selection can be either manual or automatic. Any of the output clocks (OUT0 to OUT6) can be configured to connect to any of the DSPLLs using a flexible crosspoint connection. The reference oscillator uses DSPLL B. Both a Crystal and a Reference must be installed for the device to operate.

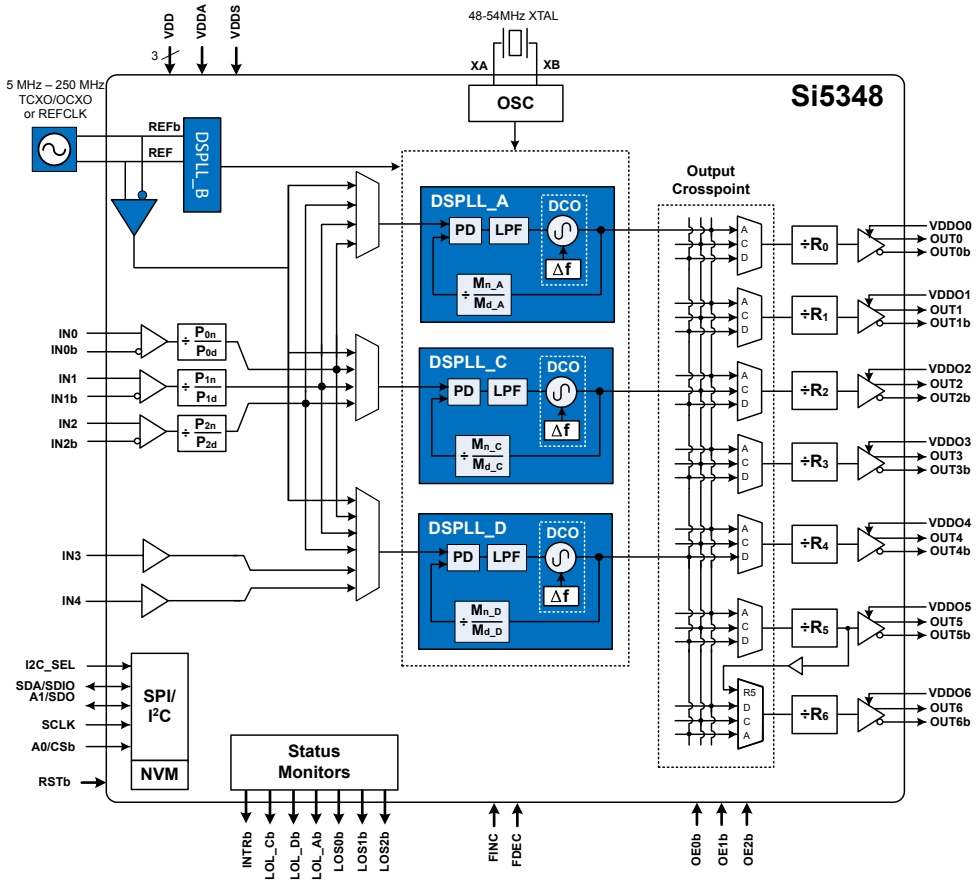


Figure 3.1. Block Diagram

3.1 DSPLL

The DSPLL is responsible for input frequency translation, jitter attenuation and wander filtering. Fractional input dividers (Pn/Pxd) allow the DSPLL to perform hitless switching between input clocks (IN0, IN1, IN2). Input switching is controlled manually or automatically using an internal state machine. The reference input determines the frequency accuracy and stability while in free-run and holdover modes. The external crystal completes the internal oscillator circuit (OSC) which is used by the DSPLL for intrinsic low-jitter performance. A crosspoint switch connects any of the DSPLLs to any of the outputs. An additional integer divisor (R) determines the final output frequency.

The frequency configuration of the DSPLL is programmable through the SPI or I2C serial interface and can also be storied in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md) and integer output division (Rn) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined by using the ClockBuilder Pro software.

Because a jitter reference is required for all applications, either a crystal or an external clock source needs to be connected to the XAXB pins. See 10. Recommended Crystals and External Oscillators and 11. Crystal and Device Circuit Layout Recommendations for more information.

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings of from 1 mHz up to 4 kHz are available for selection for each of the DSPLLs and for the reference DSPLL (DSPLL B). Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. Note that after changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (DSPLL A = 0x0414, REF B = 0x0514, DSPLL C = 0x0614, DSPLL D = 0x0715) must be set high to latch the new values into operation. SOFT_RST_PLLx will not update the BW registers so that BW_UPDATE_PLLx should typically be asserted when SOFT_RST_PLLx is asserted. Note each of these update bits will latch both loop and fastlock bandwidths.
The higher the PLL bandwidth is set relative to the phase detector frequency (Fpfd) the more chance that Fpfd will cause a spur in the Phase Noise plot of the output clock and increase the output jitter. To guarantee the best phase noise/jitter, it is recommended that the normal PLL bandwidth be kept less than Fpfd/160, although ratios of Fpfd/100 will typically work fine.

Table 3.1. DSPLL Loop Bandwidth Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
BW_PLLA	0408[7:0] - 040D[7:0]	This group of registers determine the loop bandwidth for DSPLL A, C, D and B (reference). They are all independently selectable in the range from 1 mHz up to 4 kHz. Register values determined by ClockBuilderPro.
BW_PLLC	0608[7:0] - 060D[7:0]	
BW_PLLD	0709[7:0] - 070E[7:0]	
BW_PLLB	0508[7:0] - 070E[7:0]	

3.2.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range from 100 Hz up to 4 kHz are available. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The fastlock feature can be enabled or disabled independently for each of the DSPLLs. If Fastlock is enabled, then when LOL is asserted, Fastlock settings are applied. When LOL is not asserted, Fastlock is not applied. Note that after changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (0x0414,0x0514, 0x0614, 0x0715) must be set high to latch the new values into operation. Note that each of these update bits will latch both loop and fastlock bandwidths.

Table 3.2. Fastlock Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
FASTLOCK_AUTO_EN_PLLA	0x042B[0]	Auto Fastlock Enable/Disable. Manual Fastlock must be 0 for this bit to have effect. 0: Disable Auto Fastlock 1: Enable Auto Fastlock (default)
FASTLOCK_AUTO_EN_PLLC	0x062B[0]	
FASTLOCK_AUTO_EN_PLLD	0x072C[0]	
FASTLOCK_AUTO_EN_PLLB	0x052B[0]	
FAST_BW_PLLA	0x040E[7:0] -0x0413[7:0]	Fastlock bandwidth is selectable in the range of 100 Hz up to 4 kHz. Register values determined using ClockBuilder Pro.
FAST_BW_PLLC	0x060E[7:0] - 0x0613[7:0]	
FAST_BW_PLLD	0x070F[7:0] -0x0714[7:0]	
FAST_BW_PLLB	0x050E[7:0] - 0x0513[7:0]	The reference fastlock bandwidth is selectable in the range of 1mHz to 4kHz
FASTLOCK_EXTEND_EN_PLL(A,B,C,D)	0x00E5[4:7]	Enables FASTLOCK_EXTEND

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
FASTLOCK_EXTEND_PLLA	[0x00E9[4:0] 0x00E8[7:0] 0x00E7[7:0] 0x00E6[7:0]]	Set by CBPro to minimize phase transients when switching the PLL bandwidth
FASTLOCK_EXTEND_PLLB	[0x00ED[4:0] 0x00EC[7:0] 0x00EB[7:0] 0x00EA[7:0]]	
FASTLOCK_EXTEND_PLLC	[0x00F1[4:0] 0x00F0[7:0] 0x00EF[7:0] 0x00EE[7:0]]	
FASTLOCK_EXTEND_PLLD	[0x00F5[4:0] 0x00F4[7:0] 0x00F3[7:0] 0x00F2[7:0]]	
FASTLOCK_EXTEND_SCL_PLLA	0x0294[3:0]	Set by CBPro
FASTLOCK_EXTEND_SCL_PLLB	0x0294[7:4]	
FASTLOCK_EXTEND_SCL_PLLC	0x0295[3:0]	
FASTLOCK_EXTEND_SCL_PLLD	0x0295[7:4]	
HOLDEXIT_BW_SEL0	0x059B[6]	Set by CBPro
HOLDEXIT_BW_SEL1	0x052C[4]	Set by CBPro
LOL_SLW_VALWIN_SELX_PLL(A,B,C,D)	0x0296[3:0]	Set by CBPro
FASTLOCK_DLY_ONSW_PLLA	0x02A6[19:0]	Set by CBPro
FASTLOCK_DLY_ONSW_PLLB	0x02A9[19:0]	
FASTLOCK_DLY_ONSW_PLLC	0x02AC[19:0]	
FASTLOCK_DLY_ONSW_PLLD	0x02AF[19:0]	
FASTLOCK_DLY_ON-LOL_EN_PLL(A,B,C,D)	0x0299[3:0]	Set by CBPro
FASTLOCK_DLY_ONLOLA	0x029A[19:0]	Set by CBPro
FASTLOCK_DLY_ONLOLB	0x029D[19:0]	
FASTLOCK_DLY_ONLOLC	0x02A0[19:0]	
FASTLOCK_DLY_ONLOLD	0x02A3[19:0]	

3.3 Dividers Overview

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs (A,C,D) to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

There are five main divider classes within the Si5348. See 3. Functional Description for a block diagram that shows them. Additionally, the DCO step word is used to scale the nominal output frequency in DCO mode. See 7. Digitally Controlled Oscillator (DCO) Mode for more information and block diagrams on DCO mode.

1. PXAXB: Reference input divider (0x0206)
   - Divide reference clock by 1, 2, 4, or 8 to obtain an internal reference < 54 MHz
2. P0-P2: Input clock wide range dividers (0x0208-0x022F)
   - Integer or Fractional divide values
   - Min. value is 1, Max. value is 2^{24}
   - 48-bit numerator, 32-bit denominator
   - Practical P divider range of (Fin/2 MHz) < P < (Fin/8 kHz)
   - Each P divider has a separate update bit for the new divider value to take effect
3. MA-MD: DSPLL feedback dividers (0x0415-0x041F, 0x0515-0x051F, 0x0615-0x061F, 0x0716-0x0720))
   - Integer or Fractional divide values
   - Min. value is 1, Max. value is 2^{24}
   - 56-bit numerator, 32-bit denominator
   - Practical M divider range of (Fdco/2 MHz) < M < (Fdco/8 kHz)
   - Each M divider has a separate update bit for the new divider value to take effect
   - Soft reset will also update M divider values
4. FSTEPW: DSPLL DCO step words (0x0423-0x0429, 0x0623-0x0629, 0x0724-0x072A)
   - Positive Integers, where FINC/FDEC select direction
   - Min. value is 0, Max. value is 2^{24}
   - 56-bit step size, relative to 32-bit M numerator
5. R0-R6: Output dividers (0x0250-0x026A)
   - Even integer divide values: 2, 4, 6, etc.
   - Min. value is 2, Max. value is 2^{24}
   - 24-bit word where Value = 2 x (Word + 1), for example Word=3 gives an R value of 8

4. Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run mode, Lock Acquisition Mode, Locketd Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

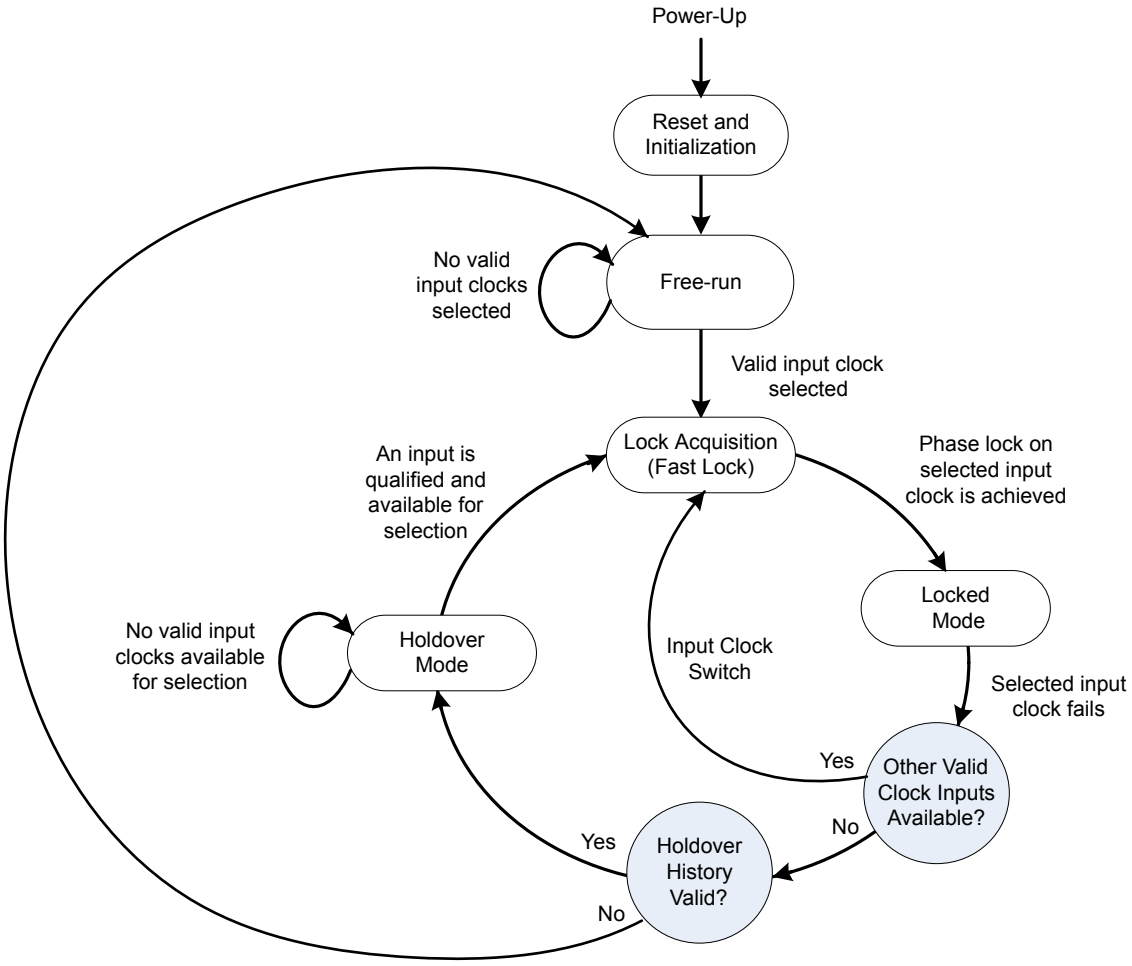


Figure 4.1. Modes of Operation

4.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete.

There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can affect all or each DSPLL individually.

Table 4.1. Reset Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
HARD_RST	0x001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST_ALL	0x001C[0]	Resets the device without re-downloading the register configuration from NVM.
SOFT_RST_PLLA	0x001C[1]	Performs a soft reset on DSPLL A only.
SOFT_RST_PLLB	0x001C[2]	Performs a soft reset on DSPLL B, affecting all PLLs.
SOFT_RST_PLLC	0x001C[3]	Performs a soft reset on DSPLL C only.
SOFT_RST_PLLD	0x001C[4]	Performs a soft reset on DSPLL D only.

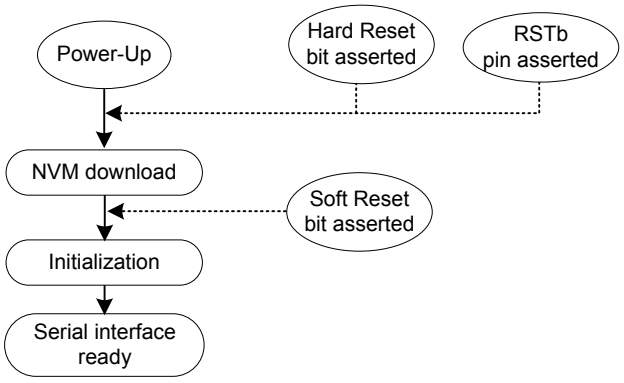


Figure 4.2. Initialization from Hard Reset and Soft Reset

The Si5348 is fully configurable using the serial interface (I2C or SPI). At power up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8 V) and VDDA (3.3 V) pins. Neither VDDOx or VDDS supplies are required to write the NVM.

4.2 Changing Registers while Device in Operation

ClockBuilder Pro generates all necessary control register writes for the entire device, including the ones described below. This is the case for both “Export” generated files as well as when using the GUI. This is sufficient to cover most applications. However, in some applications it is desirable to modify only certain sections of the device while maintaining unaffected clocks on the remaining outputs. If this is the case, please contact Skyworks Technical Support for further information: https://www.skyworksinc.com/support-ia.

If certain registers are changed while the device is in operation, it is possible for the PLL to become unresponsive (i.e. lose lock indefinitely). The following are the affected registers:

Table 4.2. Registers Affecting PLL Lock Status

Control	Register(s)
PXAXB	0x0206[1:0]
MXAXB_NUM	0x0235 – 0x023A
MXAXB_DEN	0x023B – 0x023E

The issue can easily be avoided by using the preamble and post-amble write sequence below when one of these registers is modified or large frequency steps are made. ClockBuilder Pro software adds these writes to the output file by default when exporting register files.

1. First, write the preamble.

   Write 0x0B24 = 0xC0

   Write 0x0B25 = 0x04

   Write 0x0540 = 0x01 (NOTE: for all new designs it is recommend that this register be written as part of the preamble. In some rare cases, omitting this write may result in a one-time LOL occurrence. However, if this issue has not occurred with your current frequency plan it is not likely to occur)
2. Wait 300 ms.
3. Then perform the desired register modifications.
4. Write SOFT_RST 0x001C[0] = 1
5. Write the post-amble

   Write 0x0540 = 0x00 (NOTE: for all new designs it is recommend that this register be written as part of the post-amble. In some rare cases, omitting this write may result in a one-time LOL occurrence. However, if this issue has not occurred with your current frequency plan it is not likely to occur)

   Write 0x0B24 = 0xC3

   Write 0x0B25 = 0x06

4.2.1 Revision D

The revision D and later revisions have preamble and postamble values for updating certain registers during device operation which have changed after revision B. Be sure to check the revision of the device and make sure to have the latest reference manual from the web as this information can be updated.

Either the new or old values below may be written to revision D or later devices without issue. No system software changes are necessary for legacy systems. When writing old values, note that reading back these registers will not give the written old values, but will reflect the new values. Skyworks recommends using the new values for all revision D and later designs, since the write and read values will match.

The device revision can be determined in the setting DEVICE_REV, register 0x0005.

DEVICE_REV = 0x02 or higher: New Values

4.2.2 NVM Programming

Devices have two categories of non-volatile memory: user NVM and SiLab NVM. Each type is segmented into NVM banks. There are three user NVM banks, one of which is used for factory programming (whether a base part or an Orderable Part Number). User NVM can be therefore be burned in the field up to two times. SiLab NVM cannot be modified, and contains fixed configuration information for the device.

The ACTIVE_NVM_BANK device setting can be used to determine which user NVM bank is currently being used and therefore how many banks, if any, are available to burn. The following table describes possible values:

Active NVM BANK Value (Decimal)	Number of User Banks Burned	Number of User Banks Available to Burn
3 (factory state)	1	2
15	2	1
63	3	0

Note: In-circuit programming is supported over the temperature range of 0°C to 25°C. While polling DEVICE_READY during the procedure below, the following conditions must be met in order to ensure that the correct values are written into the NVM:

- VDD and VDDA power must both be stable throughout the process.
- No additional registers may be written or read during DEVICE_READY polling. This includes the PAGE register at address 0x01. DEVICE_READY is available on every register page, so no page change is needed to read it.
- Only the DEVICE_READY register (0xFE) should be read during this time.

The procedure for writing registers into NVM is as follows:

1. Write all registers as needed. Verify device operation before writing registers to NVM.
2. You may write to the user scratch space (Registers 0x026B to 0x0272 DESIGN_ID0-DESIGN_ID7) to identify the contents of the NVM bank.
3. Write 0xC7 to NVM_WRITE register.
4. Poll DEVICE_READY until DEVICE_READY=0x0F.
5. Set NVM_READ_BANK 0x00E4[0]=1. This will load the NVM contents into non-volatile memory.
6. Poll DEVICE_READY until DEVICE_READY=0x0F.
7. Read ACTIVE_NVM_BANK and verify that the value is the next highest value in the table above. For example, from the factory it will be a 3. After NVM_WRITE, the value will be 15.

Alternatively, steps 5 and 6 can be replaced with a Hard Reset, either by RSTb pin, HARD_RST register bit, or power cycling the device to generate a POR. All of these actions will load the new NVM contents back into the device registers.

The ClockBuilder Pro Field Programmer kit is a USB attached device to program supported devices either in-system (wired to your PCB) or in-socket (by purchasing the appropriate field programmer socket). ClockBuilder Pro software is then used to burn a device configuration (project file). Learn more at ClockBuilder Pro Field Programmer.

Table 4.3. NVM Programming Registers

Register Name	Hex Address [Bit Field]	Function
ACTIVE_NVM_BANK	0x00E2[7:0]	Identifies the active NVM bank.
NVM_WRITE	0x00E3[7:0]	Initiates an NVM write when written with value 0xC7.
NVM_READ_BANK	0x00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	0x00FE[7:0]	Indicates that the device is ready to accept commands when value = 0x0F.

Warning: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming and may corrupt the register contents, as they are read from NVM. Note that this includes accesses to the PAGE register.

4.3 Free Run Mode

Once power is applied to the Si5348 and initialization is complete, all three DSPLLs will automatically enter freerun mode, generating the frequencies determined by the NVM. The frequency accuracy and stability of the generated output clocks in freerun mode is entirely dependent on the reference clock (REF/REFb), while the external crystal at the XA/XB pins determines the jitter performance of the output clocks. For example, if the reference frequency is ±10 ppm, then all the output clocks will be generated at their configured frequency ±10ppm in freerun mode. Any drift of the reference frequency will be tracked at the output clock frequencies in this mode.

4.4 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.5 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own LOL pin and status bit to indicate when lock is achieved.

4.6 Holdover Mode

Any of the DSPLLs will automatically enter holdover when the selected input clock becomes invalid (i.e., when either OOF or LOS are asserted) and no other valid input clocks are available for selection. Each DSPLL calculates a historical average of the input frequency while in locked mode to minimize the initial frequency offset when entering the holdover mode. The averaging circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window with the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value is used to ignore frequency data that may be corrupt just before the input clock failure. Each DSPLL computes its own holdover frequency average to maintain complete holdover independence between the DSPLLs.

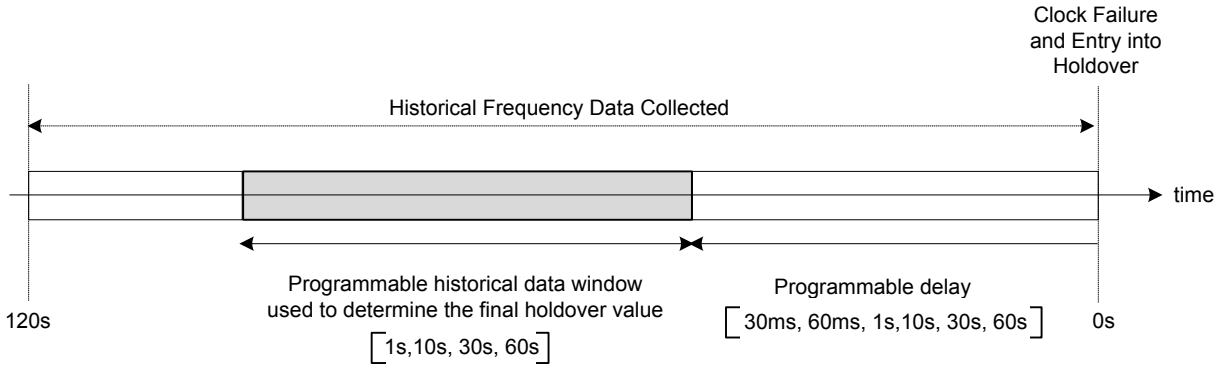


Figure 4.3. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated average holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF/REFb pins. If a clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves adjusting the output clock to achieve frequency and phase lock with the new input clock.

The recommended mode of exit from holdover is a ramp in frequency. Just before the exit begins, the frequency difference between the output frequency while in holdover and the desired, new output frequency is measured. It is quite possible (even likely) that the new output clock frequency will not be the same as the holdover output frequency because the new input clock frequency might have changed and the holdover history circuit may have changed the holdover output frequency. The ramp logic calculates the difference in frequency between the holdover frequency and the new, desired output frequency. Using the user selected ramp rate, the correct ramp time is calculated. The output ramp rate is then applied for the correct amount of time so that when the ramp ends, the output frequency will be the desired new frequency. Using the ramp, the transition between the two frequencies is smooth and linear. The ramp rate can be selected to be very slow (0.2 ppm/sec), very fast (40,000 ppm/sec) or any of ~40 values that are in between. The loop BW values do not limit or affect the ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. Ramped exit from holdover is also used for ramped input clock switching. See 5.3.2 Ramped Input Switching.

Table 4.4. DSPLL Holdover Control and Status Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
HOLD_HIST_LEN_PLLA	042E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $(2^{LEN}-1)*268ns$
HOLD_HIST_LEN_PLLC	062E[4:0]	
HOLD_HIST_LEN_PLLD	072F[4:0]	
HOLD_HIST_DELAY_PLLA	042F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $(2^{DELAY})*268ns$
HOLD_HIST_DELAY_PLLC	062F[4:0]	
HOLD_HIST_DELAY_PLLD	0730[4:0]	
FORCE_HOLD_PLLA	0435[0]	These bits allow forcing any of the DSPLLs into holdover.
FORCE_HOLD_PLLC	0635[0]	
FORCE_HOLD_PLLD	0736[0]	
HOLD_EXIT_BW_SEL_PLLA	042C[4]	Selects the exit from holdover bandwidth. Options are: 0: Exit of holdover using the fastlock bandwith 1: Exit of holdover using the DSPLL loop bandwidth
HOLD_EXIT_BW_SEL_PLLC	062C[4]	
HOLD_EXIT_BW_SEL_PLLD	072D[4]	
Holdover Status		
HOLD_PLLA HOLD_PLLC HOLD_PLLD	000E[4] 000E[6] 000E[7]	Holdover status indicator. Indicates when a DSPLL is in holdover or free-run mode and is not synchronized to the input reference. The DSPLL goes into holdover only when the historical frequency data is valid, otherwise the DSPLL will be in free-run mode.
HOLD_FLG_PLLA HOLD_FLG_PLLC HOLD_FLG_PLLD	0013[4] 0013[6] 0013[7]	Holdover status monitor sticky bits. Sticky bits will remain asserted when a holdover event occurs. Writing a zero to a sticky bit will clear it.
HOLD_HIST_VALID_PLLA	043F[1]	Holdover historical frequency data valid indicates if there is enough historical frequency data collected for valid holdover history.
HOLD_HIST_VALID_PLLC	063F[1]	
HOLD_HIST_VALID_PLLD	0740[1]	
Holdover Control and Settings		
HOLD_RAMP_BYP_PLLA	042C[3]	Enable Frequency Ramping on Holdover Exit
HOLD_RAMP_BYP_PLLC	062C[3]	
HOLD_RAMP_BYP_PLLD	072D[3]	
RAMP_STEP_SIZE_PLLA	04A6[2:0]	During frequency ramping, size of a DCO frquency step in ppm.
RAMP_STEP_SIZE_PLLC	06A6[2:0]	
RAMP_STEP_SIZE_PLLD	07A6[2:0]	

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
RAMP_STEP_INTERVAL_PLLA	042C[4]	During frequency ramping, this is how often a DCO step in frequency occurs.
RAMP_STEP_INTERVAL_PLLC	042C[6]	
RAMP_STEP_INTERVAL_PLLD	042C[7]	

5. Clock Inputs (IN0, IN1, IN2, REF, IN3, IN4)

There are four inputs that can be used to synchronize DSPLLs A, C and D. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs (IN0, IN1, IN2, REF) to be connected to DSPLLA, DSPLLC or DSPLLD as shown in the figure below. DSPLL D has two additional inputs (IN3 and IN4) that support LVCMOS input format only. Automatic clock selection can be used on any four inputs for PLLD as long as only one of IN3 or IN4 is in use. If 5 inputs are used, then they must be manually selected and there is no automatic entry into holdover from IN3 or IN4. A reference (REF) must be connected to DSPLLB as a minimum but may be connected also to the other DSPLLs as well.

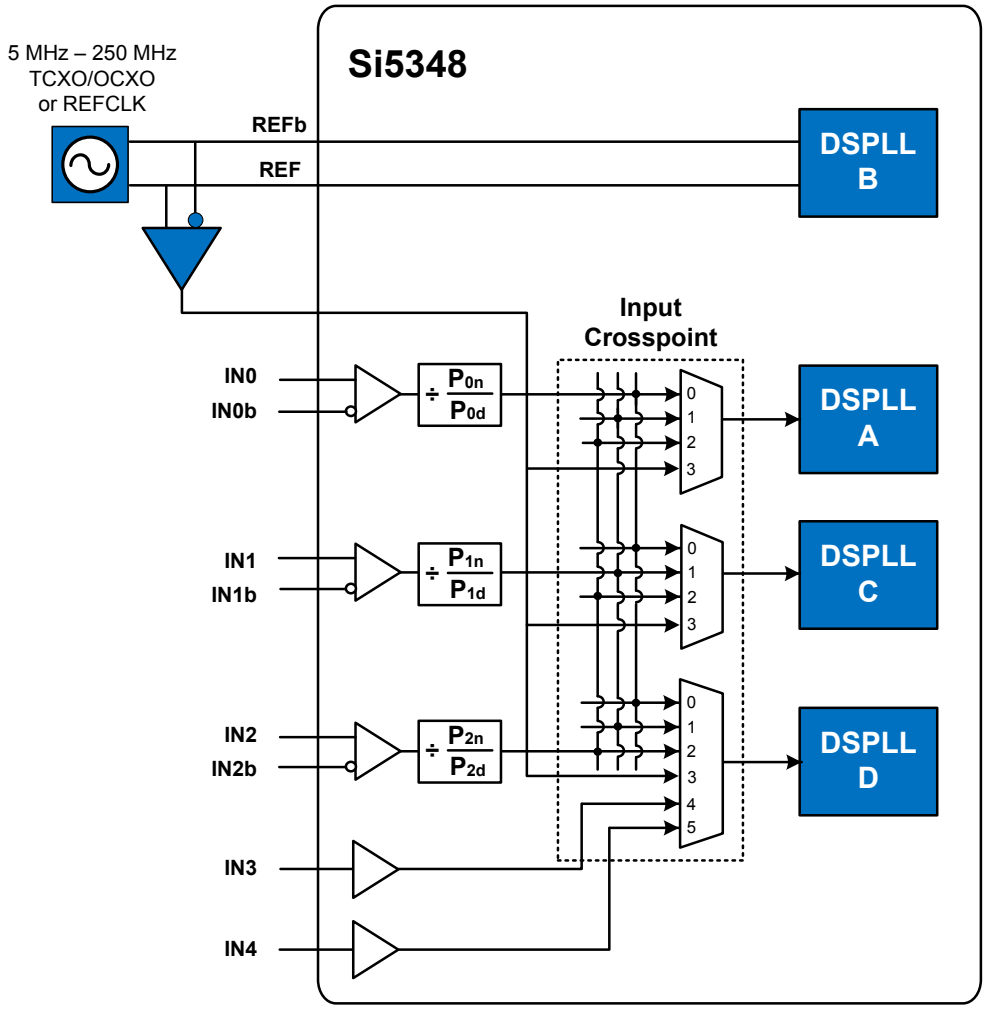


Figure 5.1. DSPLL Input Selection Crosspoint

5.1 Input Configuration and Terminations

Each of the differential inputs IN0-IN2, and REF are compatible with standard LVDS, LVPECL, HCSL, CML, and single-ended LVCMOS formats, or as a low duty cycle pulsed CMOS format. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” Input Buffer selection as these pins are internally dc-biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown in the figure below. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance.

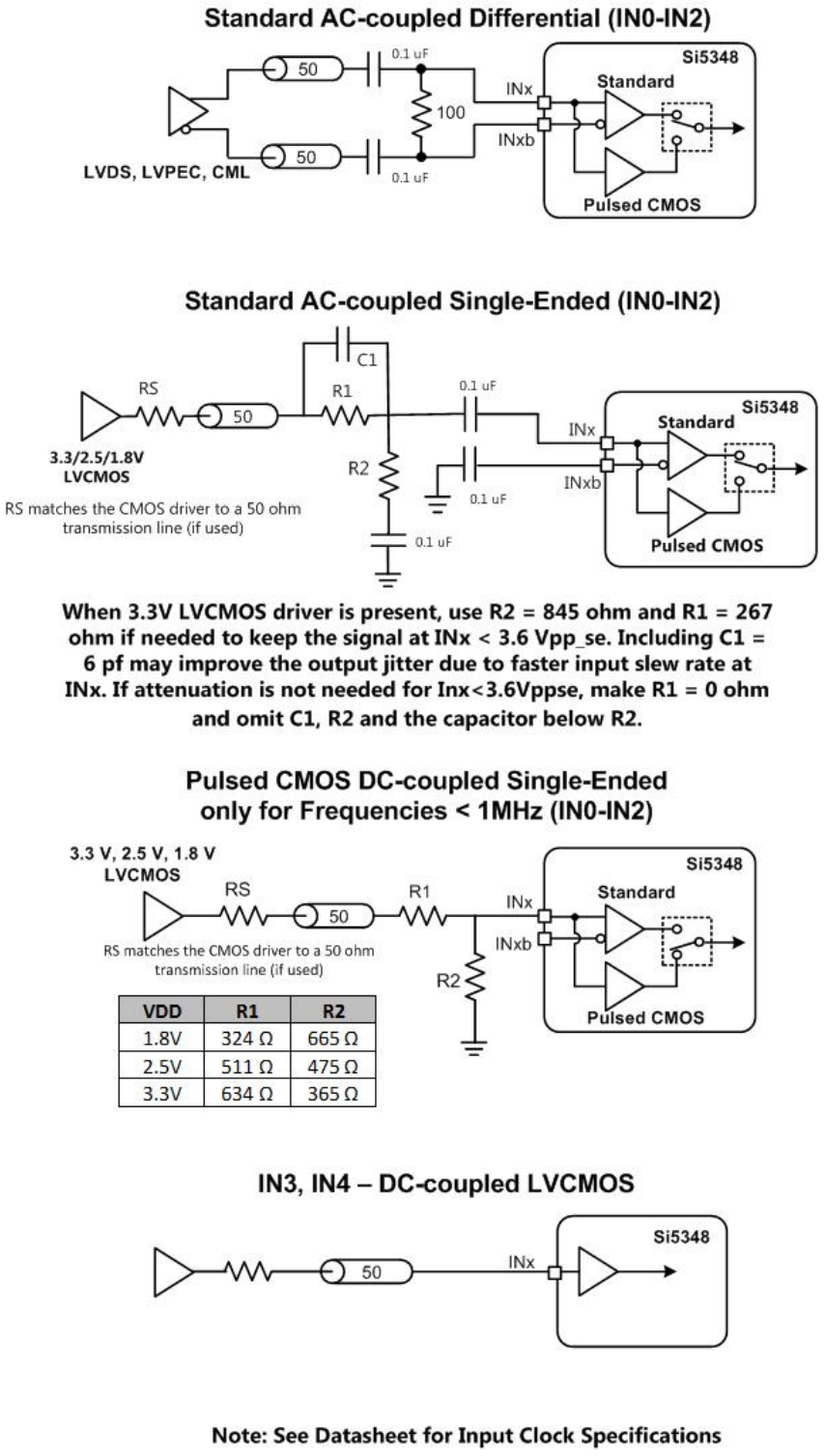


Figure 5.2. Termination of Differential and LVCMOS Input Signals

5.2 Input Source Selection

Input source selection for each of the DSPLLs can be made manually through register control or automaticallly using an internal state machine. Inputs IN3 and IN4 can only be made manually selected by DSPLL D.

Table 5.1. Manual or Automatic Input Clock Selection Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
CLK_SWITCH_MODE_PLLA	0436[1:0]	Selects manual or automatic switching mode for DSPLL A, C, D. 0: For manual 1: For automatic, non-revertive 2: For automatic, revertive 3: Reserved
CLK_SWITCH_MODE_PLLC	0636[1:0]	
CLK_SWITCH_MODE_PLLD	0737[1:0]	
CONFIGx_CMOS_PLLD	07AA[5:4] and [2:0]	Selects which 4 inputs (max) are used in automatic clock selection

In manual mode the input selection is made by writing to a register clock. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode.

Table 5.2. Manual Input Select Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
IN_SEL_PLLA	042A[1:0]	Selects the clock input used to synchronize DSPLL A, C, or D. Selections are: IN0, IN1, IN2 corresponding to the values 0, 1, and 2. Note that for PLL A and PLL C the selections are IN0-IN2, while for PLL D the selections are IN0-IN4.
IN_SEL_PLLC	062A[1:0]	
IN_SEL_PLLD	072B[2:0]	

When configured in automatic mode, the DSPLL automatically selects a valid input that has the highest configured priority. The priority arrangement is independently configurable for each DSPLL and supports revertive or non-revertive selection. When the currently selected clock is no longer valid, the highest priority clock that is valid will be selected. All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). By default, inputs asserting either or both LOS or OOF cannot be selected as a source for any DSPLL. However, these restrictions may be removed by writing to the registers described below. If there is no valid input clock, the DSP will enter either Holdover or Free Run mode depending on whether the holdover history is valid at that time or not.

Note: PLLA and PLLC have 4 available inputs IN0, IN1, IN2 and REF and all can be used in automatic selection. PLLD has 6 available inputs IN0, IN1, IN2, REF, IN3 and IN4 of which 4 can be selected using automatic input control. If more than 4 clock inputs are used in a PLLD application, then manual clock selection must be used.

Table 5.3. Automatic Input Select Control Registers

Setting Name	Function
IN(3,2,1,0)_PRIORITY_PLLA	Selects the automatic selection priority for [REF, IN2, IN1, IN0] for each DSPLL A, C, D. Selections are: 1st, 2nd, 3rd, or never select. Default is IN0=1st, IN1=2nd, IN2=3rd, REF never selected.
IN(3,2,1,0)_PRIORITY_PLLC	
IN(3,2,1,0)_PRIORITY_PLLD	

Setting Name	Function
IN(3,2,1,0)_LOS_MSK_PLLA	Determines if the LOS status for [REF, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, C, D. Default is LOS is enabled (un-masked).
IN(3,2,1,0)_LOS_MSK_PLLC	
IN(3,2,1,0)_LOS_MSK_PLLD	
IN(3,2,1,0)_OOF_MSK_PLLA	Determines if the OOF status for [REF, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, C, D. Default is enabled (un-masked).
IN(3,2,1,0)_OOF_MSK_PLLC	
IN(3,2,1,0)_OOF_MSK_PLLD	
IN_OOF_MSK_PLLB	Default is set to mask the Reference Input.

5.3 Types of Inputs

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for Ref, IN2, IN1 and IN0. Floating clock inputs are noise sensitive. Add a cap to non-CMOS unused clock inputs. Unused clock inputs for IN2, IN1 and IN0 may be powered down and left unconnected at the system level. IN3 and IN4 must be terminated when unused. For standard mode inputs, both input pins must be properly connected as shown in the figure above, including the “Standard AC Coupled Single Ended” case. In Pulsed CMOS mode, it is not necessary to connect the inverting INx input pin. To place the input buffer into Pulsed CMOS mode, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4] for Reference, IN2, IN1 and IN0.

Table 5.4. Input Clock Control and Configuration Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
IN_EN	0x0949[3:0]	Enable each of the input clock buffers for reference (REF) and IN2 through IN0.
IN_PULSED_CMOS_EN	0x0949[7:4]	Enable Pulsed CMOS mode for each input reference (REF) and IN2 through IN0.

5.3.1 Hitless Clock Switching with Phase Build Out

Hitless clock switching with phase buildout is a feature that prevents a phase change from propagating to the output when switching between two clock inputs that have exactly the same frequency and a fixed phase relationship (i.e. they are frequency locked, but with different phases). When phase buildout is enabled, the DSPLL absorbs the phase difference between the two input clocks during a clock switch. When phase buildout is disabled, the phase difference between the two inputs is propagated to the output at a rate that is determined by the DSPLL loop bandwidth. The phase buildout feature supports clock frequencies down to the minimum input frequency of 8 kHz. Phase buildout can be enabled on a per DPSLL basis. If a fractional P input divider is used, the input frequency must be 300 MHz or higher in order to ensure proper performance.

Note: Hitless switching is not available for either of the CMOS inputs (IN3/IN4).

Table 5.5. DSPLL Hitless Switching Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
HSW_EN_PLLA	0436[2]	Hitless Switching Enable/Disable for DSPLL A, C, D. Hitless switching is enabled by default.
HSW_EN_PLLC	0636[2]	
HSW_EN_PLLD	0737[2]	
RAMP_SWITCH_EN_PLLA	04A6[3]	Enable frenquency ramping on an input switch.
RAMP_SWITCH_EN_PLLC	06A6[3]	
RAMP_SWITCH_EN_PLLD	07A6[3]	
HSW_MODE_PLLA	043A[1:0]	Hitless switching mode select.
HSW_MODE_PLLC	063A[1:0]	
HSW_MODE_PLLD	073A[1:0]	

5.3.2 Ramped Input Switching

If switching between input clocks that are not exactly the same frequency (i.e. are plesiochronous), ramped switching should be enabled to ensure a smooth transition between the two input frequencies. In this situation, it is also advisable to enable phase buildout to minimize the input-to-output clock skew after the clock switch ramp has completed.

When ramped clock switching is enabled, the Si5348 will very briefly go into holdover and then immediately exit from holdover. This means that ramped switching will behave the same as an exit from holdover. This is particularly important when switching between two input clocks that are not the same frequency because the transition between the two frequencies will be smooth and linear. Ramped switching should be turned off when switching between input clocks that are always frequency locked (i.e. are the same exact frequency). Because ramped switching avoids frequency transients and over shoot when switching between clocks that are not the same frequency, CBPro defaults to ramped clock switching. The same ramp rate settings are used for both exit from holdover and clock switching. For more information on ramped exit from holdover including the ramp rate, see 4.6 Holdover Mode.

5.3.3 Hitless Switching, LOL (loss of lock) and Fastlock

When doing a clock switch between clock inputs that are frequency locked, LOL might momentarily be asserted. If so programmed, the assertion of LOL with invoke Fastlock. Because Fastlock temporarily increases the loop BW by asynchronously inserting new filter parameters into the DSPLL's closed loop, there may be transients at the clock outputs when Fastlock is either entered or exited. For this reason, it is suggested that automatic entry into Fastlock be disabled by writing a zero to FASTLOCK_AUTO_EN at 0x52B[0] whenever a clock switch might occur. For more details on hitless switching please refer to AN1057: Hitless Switching using Si534x/8x Devices.

5.3.4 External Clock Switching

External clock switches should be avoided because the Si5348 has no way of knowing when a clock switch will or has occurred. Because of this, neither the phase buildout engine or the ramp logic can be used. If expansion beyond the four clock inputs is an important issue, please see AN1111: Si534x/8x Input Clock Expander which describes how an external FPGA can be used for this purpose.

5.3.5 Synchronizing to Gapped Input Clocks

The DSPLL supports locking to a gapped input clock with missing clock edges. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its edges. Gapping a clock significantly increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter, periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of 2 missing cycles out of every 8.

When properly configured, locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification for a maximum phase transient, when the switch occurs during a gap in either input clocks. The figure below shows a 100 MHz clock with one cycle removed every 10 cycles that results in a 90 MHz periodic non-gapped output clock.

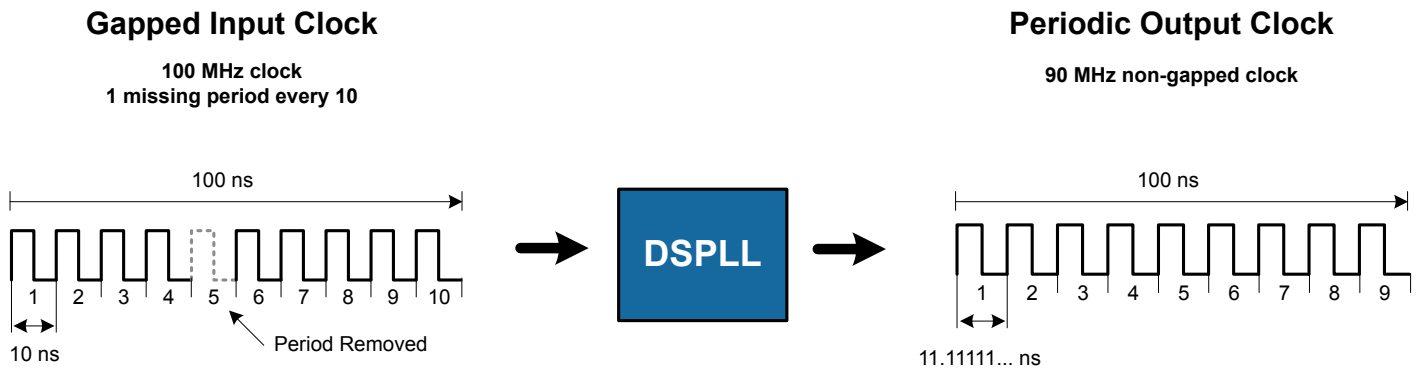


Figure 5.3. Gapped Input Clock Use

5.3.6 Rise Time Considerations

It is well known that slow rise time signals with low slew rates are a cause of increased jitter. In spite of the fact that the low loop BW of the Si5348 will attenuate a good portion of the jitter that is associated with a slow rise time clock input, if the slew rate is low enough, the output jitter will increase. The following figure shows the effect of a low slew rate on RMS jitter for a differential clock input. The figure shows the relative increase in the amount of RMS jitter due to slow rise time and is not intended to show absolute jitter values.

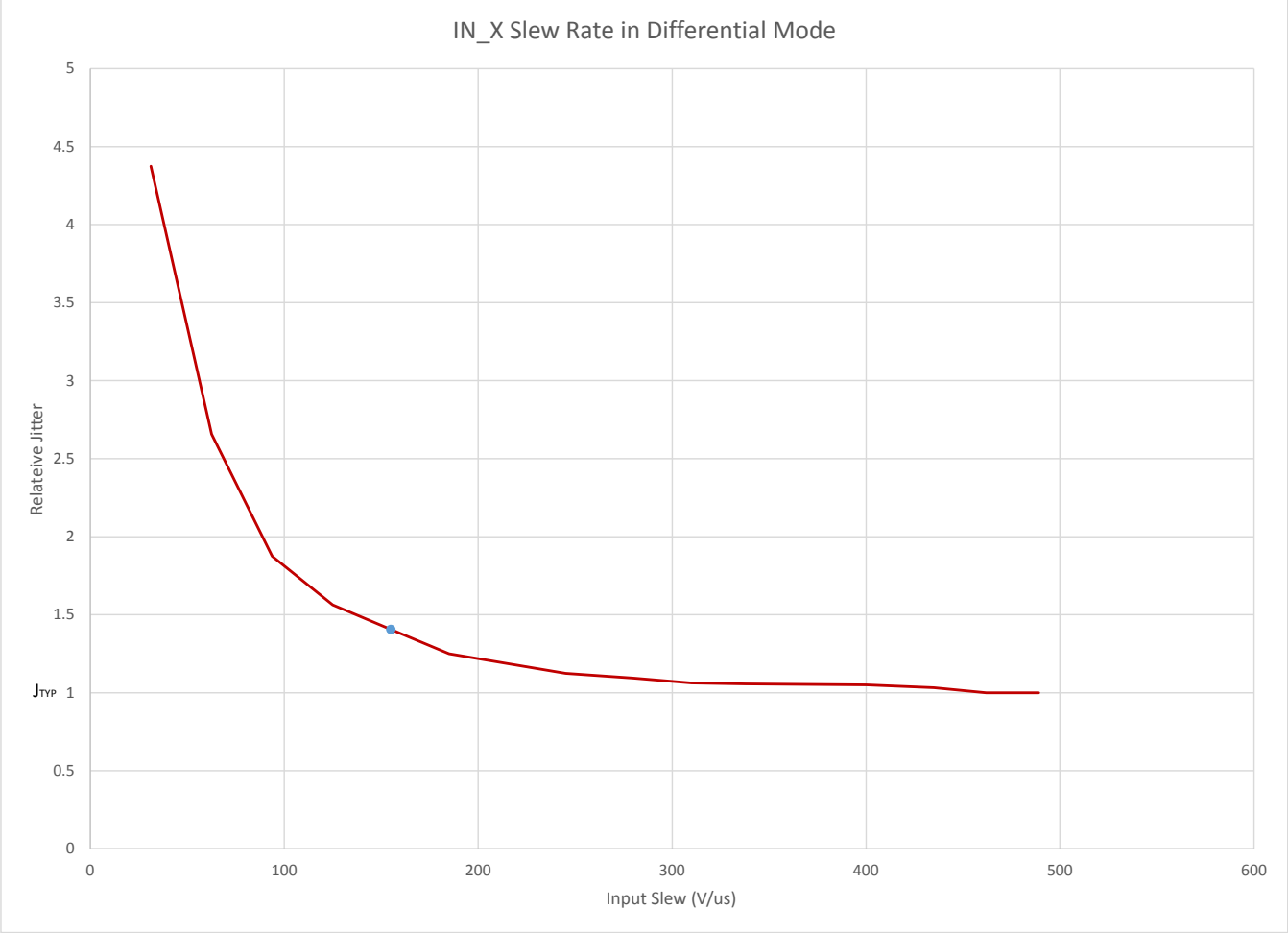


Figure 5.4. Effect of Low Slew Rate on RMS Jitter

5.4 Fault Monitoring

Input clocks (IN0, IN1, IN2, IN3, IN4) and the reference input REF/REFb are monitored for loss of signal (LOS) and input clocks (IN0, IN1, IN2) monitored for a out-of-frequency (OOF) as shown in the figure below. The REF/REFB input is used as the "reference monitor" to help determine an OOF on IN0, IN1, or IN2. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has a Loss Of Lock (LOL) indicator, which is asserted when synchronization is lost with their selected input clock.

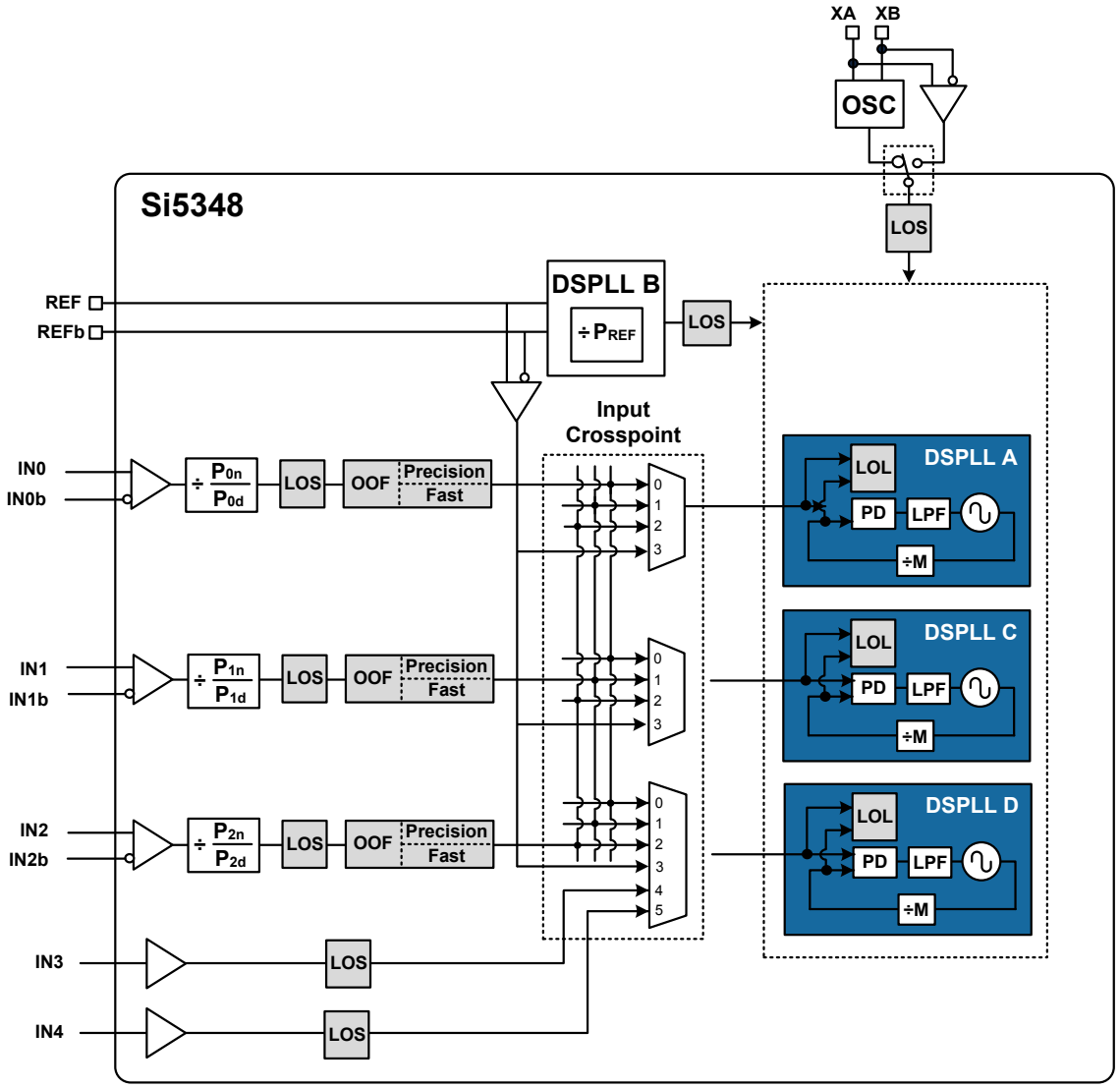


Figure 5.5. Fault Monitors

5.4.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register, when set, always stays asserted until cleared. When DSPLLD is configured to use both IN3 and IN4 the LOS outputs are not connected to the holdover entry/exit logic. When configured for one of either IN3 or IN4 (but not both) the LOS for the input clock is connected to the holdover entry/exit logic.

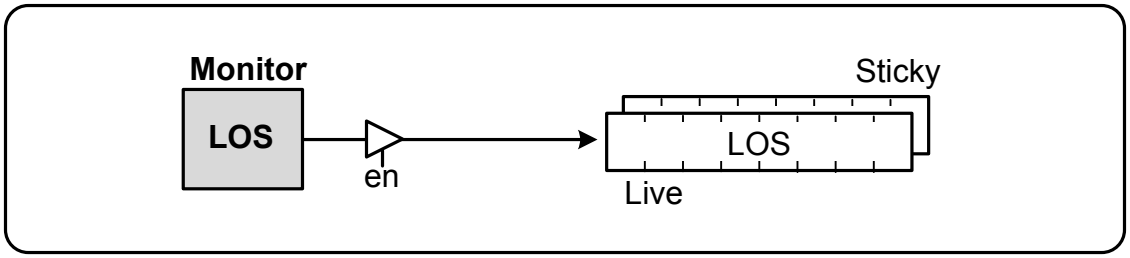


Figure 5.6. LOS Status Indicator

5.4.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valiid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

Table 5.6. LOS Status Monitor Registers

Setting Name	Hex Address [Bit Field]	Function
LOS (REF, 2,1,0)	000D[3:0]	LOS Status monitor for Reference (REF), IN2, IN1, IN0. Indicates if a valid clock is detected or if a LOS condition is present
LOS_CMOS (1,0)	000C[7:6]	LOS Status monitor for IN3 and IN4. Indicates if a valid clock is detected or if a LOS condition is present
LOSXAXB	000C[1]	LOS status monitor for the XTAL at the XAXB pins.
LOS (REF, 2,1,0)_FLG	0012[3:0]	LOS Status monitor sticky bits for Reference (REF), IN2, IN1, IN0. Sticky bitss will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOS_CMOS_FLG (1,0)	0011[7:6]	LOS Status monitor sticky bits for IN3 and IN4. Sticky bitss will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOSXAXB_FLG	0011[1]	LOS Status monitor sticky bits for XAXB. Sticky bitss will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOS Fault Monitor Controls and Settings		
LOS (REF,2,1,0)_EN	002C[3:0]	LOS monitor enable for Reference (REF), IN2, IN1, IN0. Allows disabling the monitor if unused
LOS_CMOS_EN (4,3)	02BC[2:1]	LOS monitor enable for IN3 and IN4. Allows disabling the monitor if unused
LOS(REF,2,1,0)_TRG_THR	002E[7:0]-0035[7:0]	LOS trigger threshold for Reference (REF), IN2, IN1, IN0.
LOS_CMOS(1,0)_TRG_THR	02BE[7:0]-02C0[7:0]	LOS trigger threshold for CMOS IN3 and IN4.
LOS(REF,2,1,0)_CLR_THR	0036[7:0]-003D[7:0]	Sets the LOS trigger clear sensitivity for the Reference, IN2,IN1,and IN0 and additionally the CMOS IN3, IN4. These 16 bit values are determined in ClockBuilder Pro.
LOS_CMOS(1,0)_CLR_THR	02C2[7:0]-02C4[7:0]	
LOS_CMOS_VAL_TIME	02BD[3:0]	LOS validation time for IN3 and IN4. This sets the time that an input must have a valid clock before the LOS conditions are cleared. Setting 2 ms, 100 ms, 300 ms and 2 s are available.

5.4.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its "0 ppm" reference. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared. Typically, the OOF reference will be the REF input because it will be more accurate and stable than the crystal at the XAXB pins. Because of this there is no OOF alarm for DSPLLB.

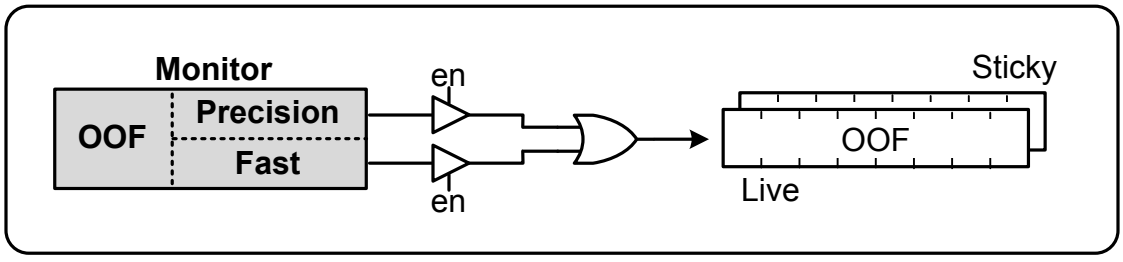


Figure 5.7. OOF Status Indicator

5.4.4 LOL Detection

The Loss of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are four parameters to the LOL monitor.

1. Assert to set the LOL
   - User sets the threshold in ppm in CBPro.
2. Fast assert to set the LOL
   - CBPro sets this to ~100 times the slow assert threshold.
   - A very large ppm error in a short time will assert the LOL.
3. De-assert to clear the LOL
   - User sets the threshold in ppm in CBPro.
4. Clear delay
   - CBPro set this based upon the project plan.

A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

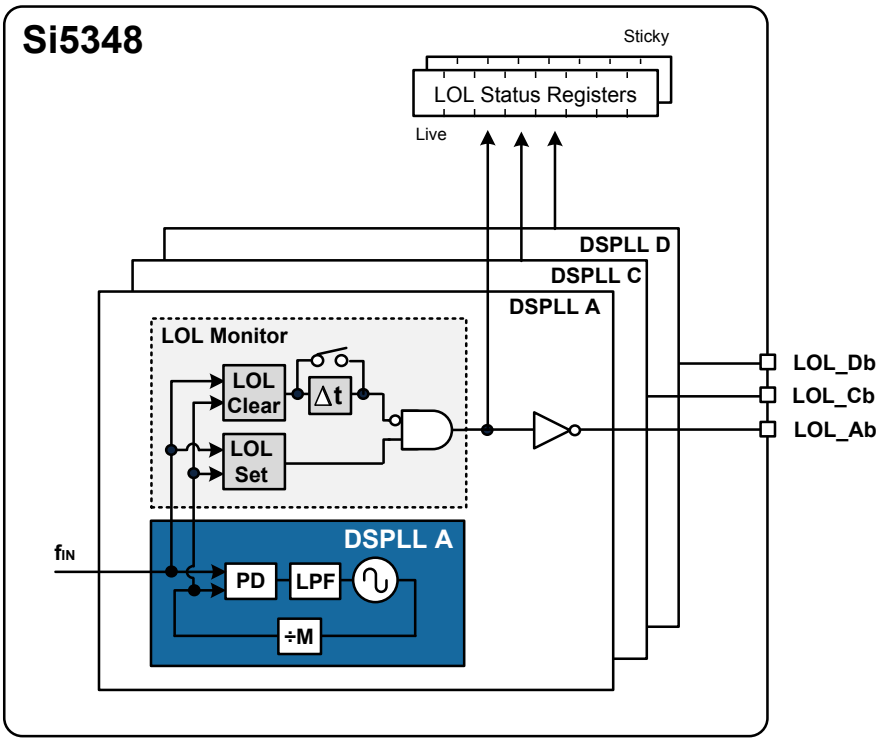


Figure 5.8. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity which is register configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated is shown below. There is less than 1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 10 ppm frequency difference.

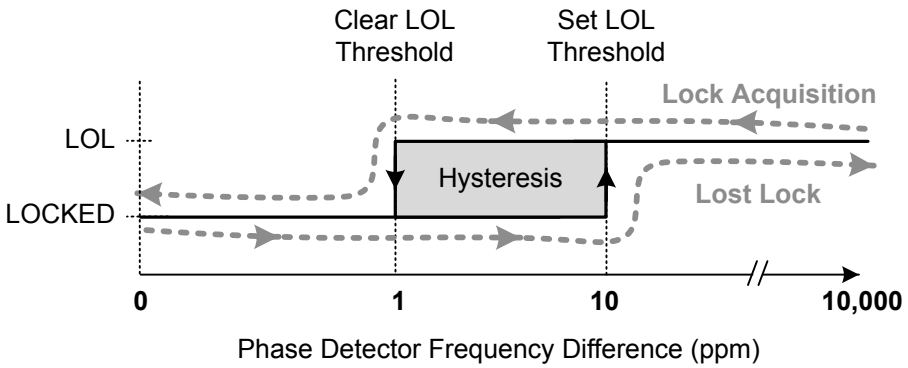


Figure 5.9. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

It is important to know that, in addition to being status bits, LOL enables Fastlock.

Table 5.7. LOL Status Monitor Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
LOL Status Indicators		
LOL_PLL(D,C,B,A)	000E[3:0]	Status bit that indicates if DSPLL A, B (Reference), C, or D is locked to an input clock.
LOL_FLG_PLL(D,C,B,A)	0013[3:0]	Sticky bits for LOL_[D,C,B,A]_STATUS register. Writing a zero to a sticky bit will clear it.
LOL Fault Monitor Controls and Settings		
LOL_SET_THR_PLL(D,C,B,A)	009E[7:0] - 009F[7:0]	Configures the loss of lock set thresholds for DSPLL A, B, C, D. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 0.2 ppm.
LOL_CLR_THR_PLL(D,C,B,A)	00A0[7:0] - 00A1[7:0]	Configures the loss of lock clear thresholds for DSPLL A, B, C, D. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 2 ppm.
LOL_CLR_DELAY_PLL(D,C,B,A)	00A3[7:0] - 00B6[7:0]	This is a 35-bit register that configures the delay value for the LOL Clear delay. Selectable from 4 ns over 500 seconds. This value depends on the DSPLL frequency configuration and loop bandwidth. It is calculated using ClockBuilder Pro utility.
LOL_TIMER_EN_PLL(D,C,B,A)	00A2[3:0]	Allows bypassing the LOL Clear timer for DSPLL A, B, C, D. 0- bypassed, 1-enabled. When enabled, the LOL_CLR_DELAY is active.

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
LOL_NOSIG_TIME_PLL(D,C,B,A)	0x02B7 ([7:6],[5:4],[3:2],[1:0])	Sets 417 ms as time without an input to assert LOL. Set by CBPro
FASTLOCK_EXTEND_EN_PLL(D,C,B,A)	0x00E5 [7:4]	Enable FASTLOCK_EXTEND
FASTLOCK_EXTEND_PLL(D,C,B,A)	0x00F2 [28:0] - 0x00E6 [28:0]	Set by CBPro to minimize phase transients when switching the PLL bandwidth
FASTLOCK_EXTEND_SCL_PLL(D,C,B,A)	0x0295 [7:4], [3:0], 0x0294 [7:4], [3:0]	Set by CBPro
LOL_SLW_VALWIN_SELX_PLL(D,C,B,A)	0x0296 [3:0]	Set by CBPro
FAST-LOCK_DLY_ONSW_EN_PLL(D,C,B,A)	0x0297 [3:0]	Set by CBPro
FASTLOCK_DLY_ONSW_PLL(D,C,B,A)	0x02AF[19:0] - 0x02A6[19:0]	Set by CBPro
FASTLOCK_DLY_ON-LOL_EN_PLL(D,C,B,A)	0x0299 [3:0]	Set by CBPro
FASTLOCK_DLY_ONLOL_PLL(D,C,B,A)	0x02A3[19:0] - 0x029A[19:0]	Set by CBPro

The settings in the table above are handled by ClockBuilder Pro. Manual settings should be avoided.

5.4.5 Interrupt Pin (INTRb)

There is an interrupt pin available on the device which is used to indicate a change in state of one or several of the status indicators. Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the status register that caused the interrupt. If an interrupt occurs the various status registers from the unmasked flags must be checked and then cleared.

Table 5.8. Interrupt Mask Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
LOS(REF, 2, 1, 0)_INTR_MSK	0018[3:0]	Prevents Reference (REF), IN2, IN1, IN0 LOS from asserting the INTRb pin
OOF(REF,2, 1, 0)_INTR_MSK	0018[7:4]	Prevents REF, IN2, IN1, IN0 OOF from asserting the INTRb pin
LOSXAXB_INTR_MSK	0017[1]	Prevents XAXB LOS from asserting the INTRb pin
LOS_CMOS_INTR_MSK	0017[7:6]	Prevents IN3 and IN4 from asserting the INTRb pin
LOL_INTR_MSK_PLL(D,B,C,A)	0019[3:0]	Prevents DSPLL D, B,C, A LOL from asserting the INTRb pin
HOLD_INTR_MSK_PLL(D,C,A)	0019[7:4]	Prevents DSPLL D, C, A HOLD from asserting the INTRb pin
CAL_FLG_PLL(D,C,B,A)_MSK	001A[7:4]	Prevents DSPLL D, C, B, A calibration from asserting the INTRb pin.
SMBUS_TIMEOUT_INTR_MKS	0017[5]	Prevents SMBUS Timeout from asserting the INTRb pin.
SYSINCAL_INTR_MSK	0017[0]	Prevents SYSINCAL from asserting the INTRb pin.

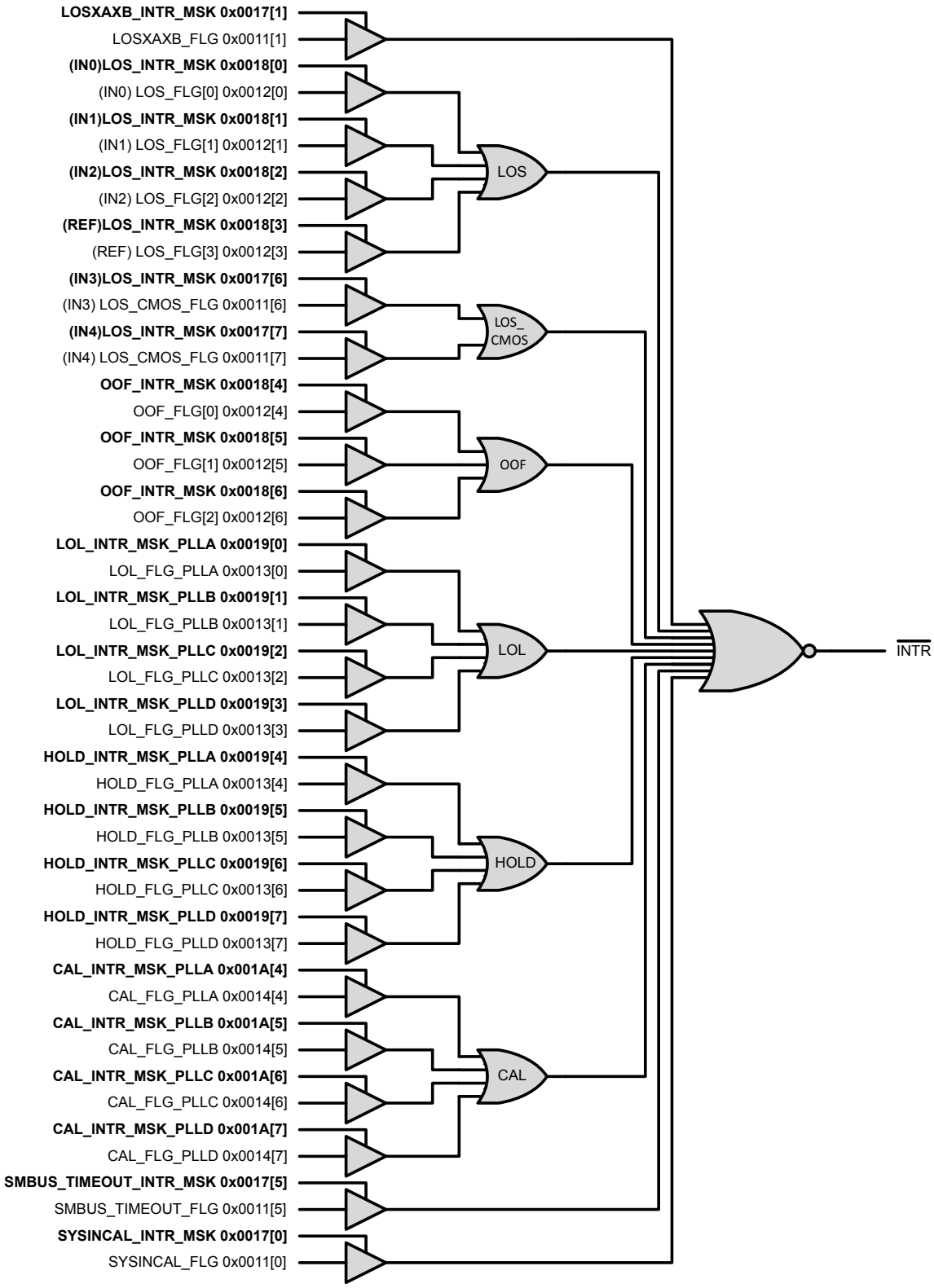


Figure 5.10. Interrupt Triggers and Masks

The _FLG bits are "sticky" versions of the alarm bits and will stay high until cleared. A _FLG bit can be cleared by writing a zero to the _FLG bit. When a _FLG bit is high and its corresponding alarm bit is low, the _FLG bit can be cleared.

During run time, the source of an interrupt can be determined by reading the _FLG register values and logically ANDing them with the corresponding _MSK register bits (after inverting the _MSK bit values). If the result is a logic one, then the _FLG bit will cause an interrupt.

For example, if LOS_FLG[0] is high and LOS_INTR_MSK[0] is low, then the INTRb pin will be active (low) and cause an interrupt. If LOS[0] is zero and LOS_MSK[0] is one, writing a zero to LOS_MSK[0] will clear the interrupt (assuming that there are no other interrupt sources). If LOS[0] is high, then LOS_FLG[0] and the interrupt cannnot be cleared.

Note: The INTRb pin may toggle during reset.

6. Output Clocks

6.1 Outputs

The Si5348 supports seven differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, with CML-compatible amplitudes. In addition to supporting differential signals, any of the outputs can be configured as dual single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 14 single-ended outputs, or any combination of differential and single-ended outputs.

6.1.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

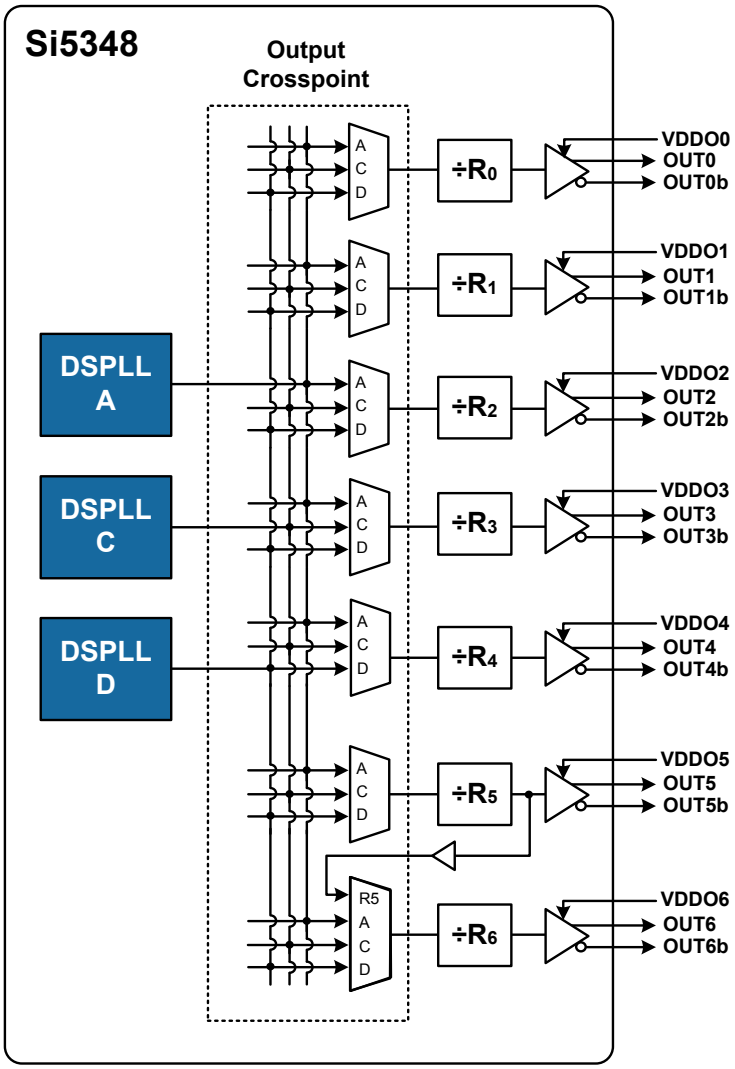


Figure 6.1. DSPLL to Output Driver Crosspoint

6.1.2 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment. Resetting the device using the RSTb pin or asserting the hard reset bit 0x001E[1] will give the same result. Soft reset does not affect output alignment.

6.1.3 Support for 1 Hz Output (1 pps)

Output 6 of the Si5348 can be configured to generate a 1 Hz clock by cascading the R5 and R6 dividers. Output 5 is still usable in this case but is limited to a frequency of 33.5 MHz or less. ClockBuilder Pro automatically determines the optimum configuration when generating a 1 Hz output.

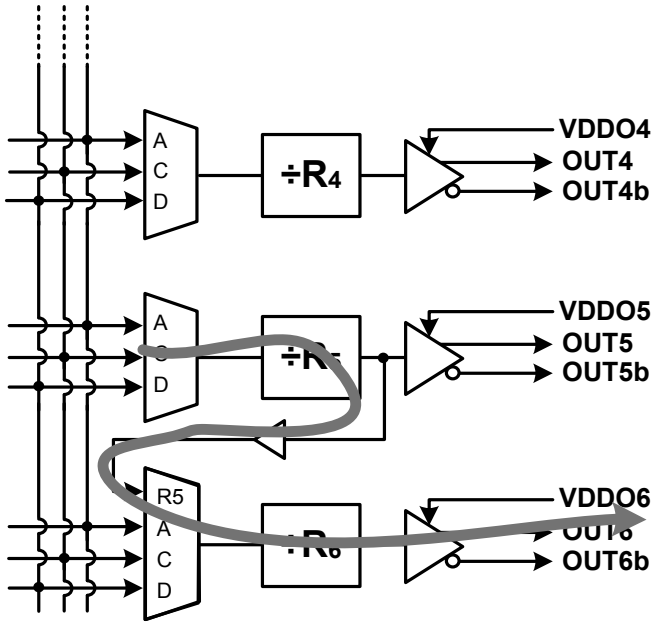


Figure 6.2. Generating a 1 Hz Output using the Si5348

6.2 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another, the laws of physics dictate that there will be some amount of crosstalk. The jitter generation of the Si5348 is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the crosstalk will come from the Si5348, and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources since the Si5348 must be attached to a board in order to measure jitter.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in the table that follows.

Table 6.1. Example of Output Clock Placement

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	622.08	156.25
5	625	156.25
6	Not used	625

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. For example, a 155.52 MHz clock should not be placed next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are allowed, and these outputs should be grouped together when possible. Noting that because 155.52 MHz x 4 = 622.08 MHz and 156.25 MHz x 4 = 625 MHz, it is okay to place each pair of these frequency values close to one another.
3. Unused outputs can be used to separate clock inputs that might otherwise interfere with one another. In this case, see OUT3.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided in jitter-sensitive applications. When CMOS clocks are unavoidable, even greater care must be taken with respect to the above guidelines.For more information on these issues, see AN862: "Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems."

The ClockBuilder Pro Clock Placement Wizard is an easy way to reduce crosstalk for a given frequency plan. This feature can be accessed on the "Define Output Frequencies" page of ClockBuilder Pro in the lower left hand corner of the GUI. It is recommended to use this tool after each project frequency plan change.

6.2.1 Output Crosspoint and Differential Signal Format Selection

The differential output swing and common mode voltage are both fully programmable and compatible with a wide variety of signal formats, including LVDS, LVPECL, HCSL, and CML. The differential formats can be either normal- or low-power mode. Low-power format uses less power for the same amplitude but has the drawback of slower rise/fall times. See 15. Custom Differential Amplitude Controls for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 20 single-ended outputs or any combination of differential and single-ended outputs. Note also that CMOS can create much more crosstalk than differential outputs, so extra care must be taken in their pin placement so that other clocks that need the lowest jitter are not on nearby pins. With all outputs, see “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for additional information on frequency planning considerations.

Table 6.2. Output Crosspoint Selection Registers

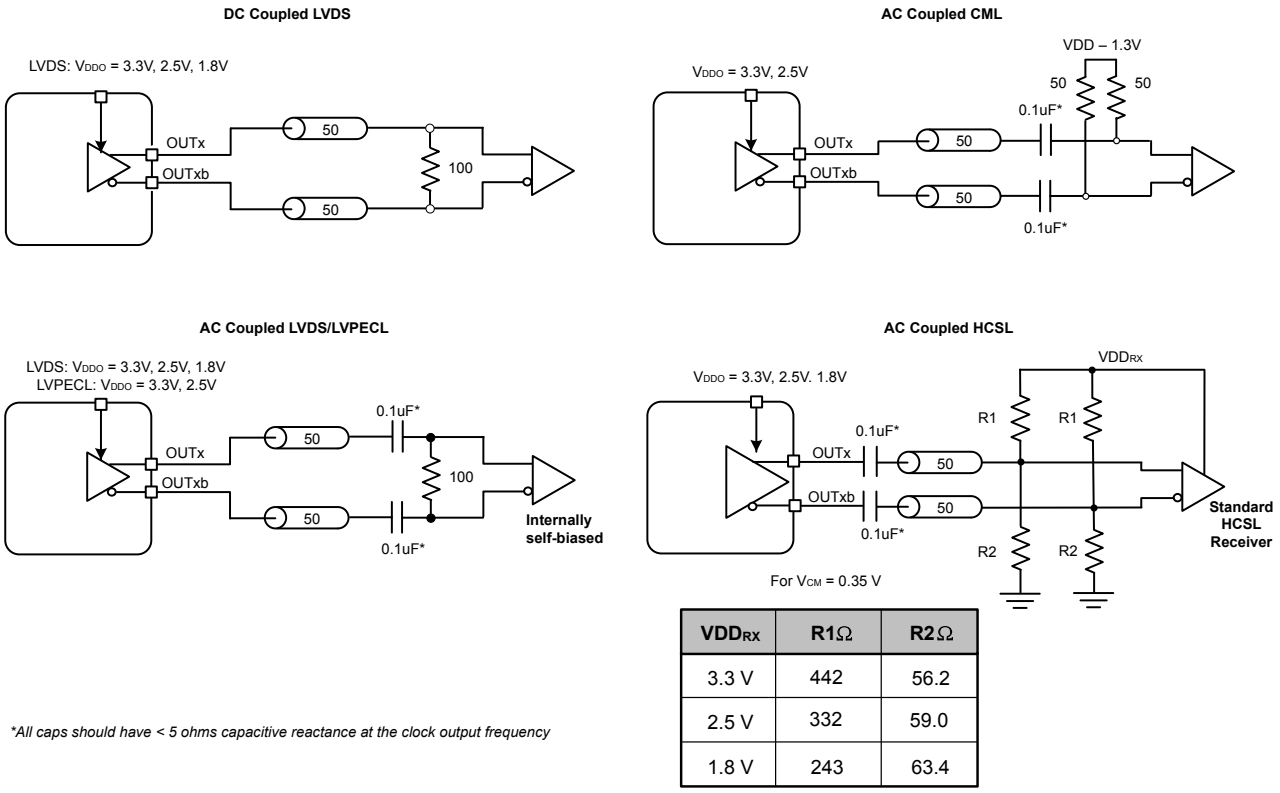
Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUT0_MUX_SEL	0115[2:0]	Selects the DSPLL that each of the outputs are connected to. Options are DSPLL_A, DSPLL_C, or DSPLL_D.
OUT1_MUX_SEL	011A[2:0]	
OUT2_MUX_SEL	011F[2:0]	
OUT3_MUX_SEL	0129[2:0]	
OUT4_MUX_SEL	012E[2:0]	
OUT5_MUX_SEL	0133[2:0]	
OUT6_MUX_SEL	013D[2:0]	

Table 6.3. Output Signal Format Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUT0_FORMAT	0113[2:0]	Selects the output signal format as differential or LVCMOS.
OUT1_FORMAT	0118[2:0]	
OUT2_FORMAT	011D[2:0]	
OUT3_FORMAT	0127[2:0]	
OUT4_FORMAT	012C[2:0]	
OUT5_FORMAT	0131[2:0]	
OUT6_FORMAT	013B[2:0]	

6.2.2 Differential Output Terminations

The differential output drivers support both ac coupled and dc coupled terminations as shown in the figure below.



VDDRX	R1Ω	R2Ω
3.3 V	442	56.2
2.5 V	332	59.0
1.8 V	243	63.4

Figure 6.3. Output Terminations for Differential Outputs

6.3 Differential Outputs

6.3.1 Differential Output Amplitude Controls

The differential amplitude of each output can be controlled with the following registers. See Chapter 15. Custom Differential Amplitude Controls for register settings for non-standard amplitudes.

Table 6.4. Differential Output Voltage Amplitude (Swing) Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUT0_AMPL	0114[6:4]	Sets the differential voltage swing (amplitude) for the output drivers in both normal and low-power modes. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 39 recommended settings.
OUT1_AMPL	0119[6:4]	
OUT2_AMPL	011E[6:4]	
OUT3_AMPL	0128[6:4]	
OUT4_AMPL	012D[6:4]	
OUT5_AMPL	0132[6:4]	
OUT6_AMPL	013C[6:4]	

6.3.2 Differential Output Common Mode Voltage Selection

The common mode voltage (VCM) for differential output normal and low-power modes is selectable depending on the supply voltage provided at the output's VDDO pin. See Chapter 15. Custom Differential Amplitude Controls for recommended OUTx_CM settings when using custom output amplitude.

Table 6.5. Differential Output Common Mode Voltage Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUT0_CM	0114[3:0]	Sets the common mode voltage for the differential output driver. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 39 recommended settings.
OUT1_CM	0119[3:0]	
OUT2_CM	011E[3:0]	
OUT3_CM	0128[3:0]	
OUT4_CM	012D[3:0]	
OUT5_CM	0132[3:0]	
OUT6_CM	013C[3:0]	

6.3.3 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

1. Normal or Low Power Format
2. Amplitude (sometimes called Swing)
3. Common Mode Voltage
4. Stop High or Stop Low

The Normal mode setting includes an internal 100 ohms resistor between the OUT/OUTb pins. In Low Power mode, this resistor is removed, resulting in a higher output impedance. The increased impedance creates larger amplitudes for the same power while reducing edge rates that may increase jitter or phase noise. In either mode, the differential receiver must be properly terminated to the PCB trace impedance for good system signal integrity. Note that ClockBuilder Pro does not provide low-power mode settings. Contact Skyworks Technical Support for assistance with low-power mode use.

Amplitude controls are as described in the previous section and also in more detail in Chapter 15. Custom Differential Amplitude Controls. Common mode voltage selection is also described in more detail in Chapter 15. Custom Differential Amplitude Controls. The Stop High or Stop Low choice is described above.

Table 6.6. Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML

Standard	VDDOx	Mode	OUTx_FORMAT	OUTx_CM	OUTx_AMPL
	(V)		(decimal)	(decimal)	(decimal)
LVPECL	3.3	Normal	1	11	6
LVPECL	2.5	Normal	1	11	6
LVPECL	3.3	Low-Power	2	11	3
LVPECL	2.5	Low-Power	2	11	3
LVDS	3.3	Normal	1	3	3
LVDS	2.5	Normal	1	11	3
Sub-LVDS [1]	1.8	Normal	1	13	3
LVDS	3.3	Low-Power	2	3	1
LVDS	2.5	Low-Power	2	11	1
Sub-LVDS [1]	1.8	Low-Power	2	13	1
HCSL[2]	3.3	Low-Power	2	11	3
HCSL[2]	2.5	Low-Power	2	11	3
HCSL[2]	1.8	Low-Power	2	13	3

Note:

1. The Sub-LVDS common mode voltage is not compliant with LVDS standards. Therefore, AC coupling the driver to an LVDS receiver is highly recommended.
2. Creates HCSL compatible signals, see HCSL receiver biasing network in Figure 16.

The output differential driver can also produce a wide range of CML compatible output amplitudes. See Chapter 15. Custom Differential Amplitude Controlsfor additional information.

6.4 LVCMOS Outputs

6.4.1 LVCMOS Output Terminations

LVCMOS outputs may be ac- or dc-coupled, as shown in the figure in 6.2.2 Differential Output Terminations. AC coupling is recommended for best jitter and phase noise performance. For dc-coupled LVCMOS, as shown again in the figure below, series termination resistors are required in order to increase the total source resistance to match the trace impedance of the circuit board.

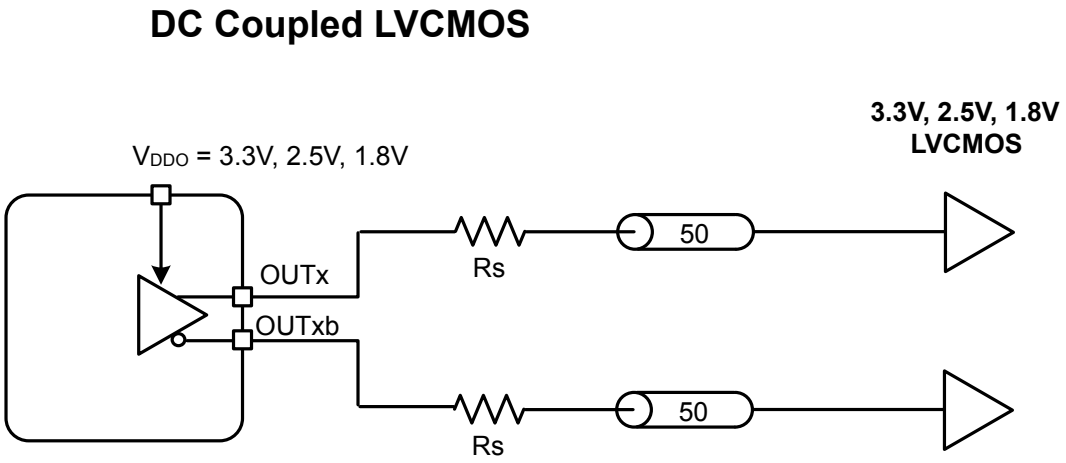


Figure 6.4. LVCMOS Output Terminations

6.4.2 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A series source termination resistor (Rs) is recommended close to the output to match the selected output impedance to the trace impedance (i.e. Rs = Trace Impedance – Zs). There are multiple programmable output impedance selections for each VDDO option as shown in the table below. Generally, the lowest impedance for a given supply voltage is preferable, since it will give the fastest edge rates.

Table 6.7. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x03*	31 Ω	5 mA

Note:
1. Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.

Table 6.8. LVCMOS Drive Strength Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUT0_CMOS_DRV	0113[7:6]	LVCMOS output impedance. See the table above.
OUT1_CMOS_DRV	0118[7:6]	
OUT2_CMOS_DRV	011D[7:6]	
OUT3_CMOS_DRV	0127[7:6]	
OUT4_CMOS_DRV	012C[7:6]	
OUT5_CMOS_DRV	0131[7:6]	
OUT6_CMOS_DRV	013B[7:6]	

6.4.3 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

6.4.4 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTx pin is generated with the same polarity (in phase) with the clock on the OUTxb pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

Table 6.9. LVCMOS Output Polarity Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUT0_INV	0115[7:6]	Controls output polarity of the OUTx and OUTxb pins when in LVCMOS mode. Selections are:
OUT1_INV	011A[7:6]	
OUT2_INV	011F[7:6]	
OUT3_INV	0129[7:6]	
OUT4_INV	012E[7:6]	
OUT5_INV	0133[7:6]	
OUT6_INV	013D[7:6]	

6.5 Output Enable/Disable

The Si5348 allows enabling/disabling outputs by either pin, register control, or a combination of both. Three output enable pins are available (OE0b, OE1b, OE2b). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0b controls all of the outputs while OE1b and OE2b pins are unmapped and have no affect until configured. The figure below shows an example of a output enable mapping scheme that is register configurable and can be stored in NVM as the default at power-up.

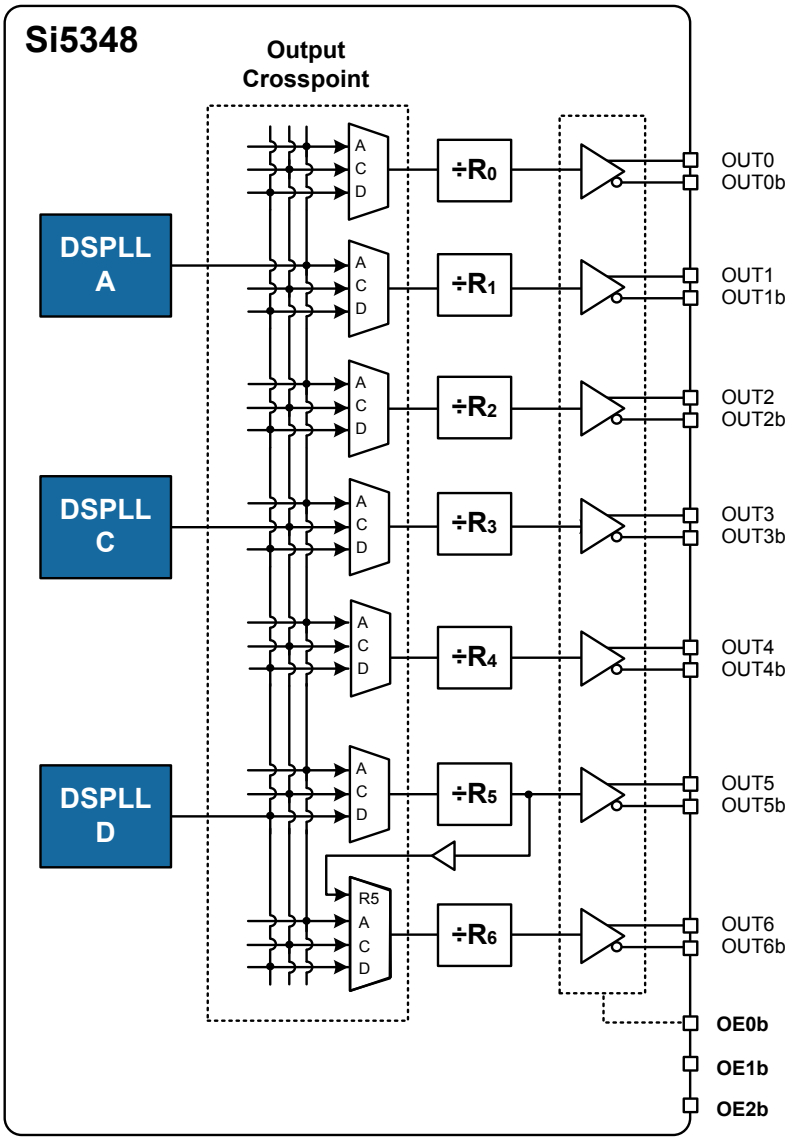
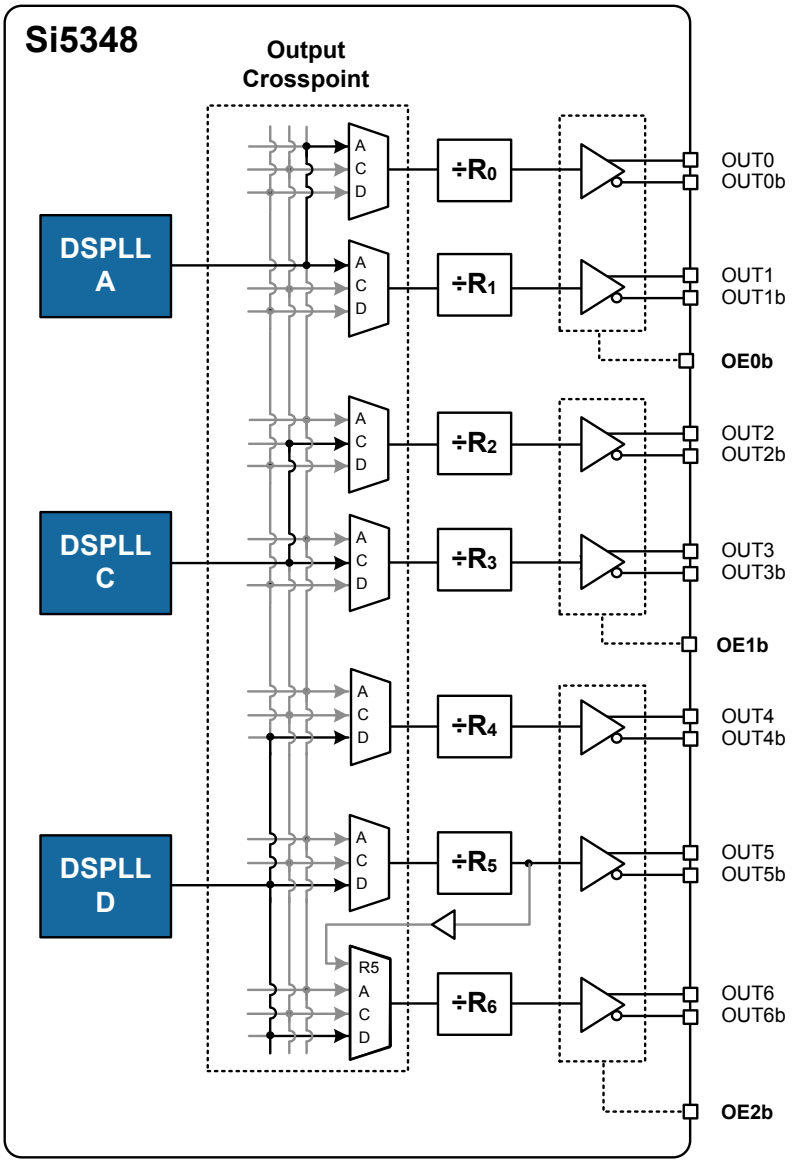


Figure 6.5. Example of Configuring Output Enable Pins

In its default state the OE0b pin enables/disables all outputs. The OE1b and OE2b pins are not mapped and have no effect on outputs.



An example of a configurable output enable scheme. In this case, OE0b controls the outputs associated with DSPLLb A, OE1b controls the outputs for DSPLLb C, and OE2b controls the outputs for DSPLL D.

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the OEb pin(s) has them enabled. By default the output enable register settings are configured to allow the OEb pins to have full control.

6.5.1 Output Disable State Selection

When the output driver is disabled, the outputs will drive either logic high or logic low, selectable by the user. The output common mode voltage is maintained while the driver is disabled, reducing enable/disable transients.

By contrast, powering down the driver rather than disabling it increases output impedance annd shuts off the output common mode voltage. For all output drivers connected in the system, it is recommended to use Disable rather than Powerdown to reduce enable/disable common mode transients. Unused outputs may be left unconnected, powered down to reduce current draw, and, with the corresponding VDDOx, left unconnected.

6.5.2 Output Disable During LOL

By default a DSPLL that is out of lock will generate an output clock. There is an option to disable the outputs when a DSPLL is out of lock (LOL). This option can be useful to force a downstream PLL into holdover.

6.5.3 Output Disable During XAXB_LOS

The internal oscillator circuit, in combination with the external crystal, provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm.

6.5.4 Output Driver State When Disabled

The disabled state of an output driver is register-configurable as disable low or disable high.

Table 6.10. Output Enable/Disable Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
OUTALL_DISABLE_LOW	0102[0]	Allows disabling all output drivers: 0 - all outputs disabled, 1 - all outputs controlled by the OUTx_OE bits. Note that if the OEb pin is held high (disabled), then all assigned outputs will be disabled regardless of the state of this register bit.
OUT0_OE OUT1_OE OUT2_OE OUT3_OE OUT4_OE OUT5_OE OUT6_OE	0112[1] 0117[1] 011C[1] 0126[1] 012B[1] 0130[1] 013A[1]	Allows enabling/disabling individual output drivers. Note that the OEb pin must be held low in order to enable an output with these register bits.
OUT_DIS_MASK_LOL_PLL(D,C,B,A)	0142[3:0]	Determines if the outputs are disabled during an LOL condition. 0 = outputs disable on LOL, 1 = outputs remain enabled during LOL (default). This option is independently configured for each DSPLL. See DRVx_DIS_SRC registers.
OUT_DIS_MSK_LOSXAXB	0141[6]	Determines if outputs are disabled during an LOSXAXB condition. 0 = all outputs disabled on LOSXAXB (default), 1 = outputs remain enabled during LOSXAXB condition.
OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE OUT4_DIS_STATE OUT5_DIS_STATE OUT6_DIS_STATE	0113[5:4] 0118[5:4] 011D[5:4] 0127[5:4] 012C[5:4] 0131[5:4] 013B[5:4]	Sets the state for the outputs when they are disabled.

6.5.5 Synchronous/Asynchronous Output Selection

Outputs can be configured to enable and disable either synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

Table 6.11. Synchronous/Asynchronous Disable Control Registers

Setting Name	Address: 0xXX:XX[Bit]	Function
	Si5348	
OUT0_SYNC_EN	0113[3]	Selects Synchronous or Asynchronous output disable. 1= synchronous, 0 = asynchronous. Default is asynchronous mode.
OUT1_SYNC_EN	0118[3]	
OUT2_SYNC_EN	011D[3]	
OUT3_SYNC_EN	0127[3]	
OUT4_SYNC_EN	012C[3]	
OUT5_SYNC_EN	0131[3]	
OUT6_SYNC_EN	013B[3]	

6.5.6 Output Driver Disable Source Summary

There are a number of conditions that may cause the outputs to be automatically disabled. The user may mask out unnecessary disable sources to match the system requirements. Any one of the unmasked sources may cause the outputs to be disabled; this is more powerful but similar in concept to open source “wired-OR” configurations. The table below summarizes the output disable sources with additional information for each source.

Table 6.12. Output Driver Disable Sources Summary

Output Driver Disable Source	Disable Outputs when Source	Individually Assignable?	Maskable?	Related Registers[Bits] (Hex)	Comments
				Si5348	
OUTALL_DISABLE_LOW	Low	N	N	0102[0]	User Controllable
OUT0_OE	Low	Y	N	0112[1]	User Controllable
OUT1_OE				0117[1]	
OUT2_OE				011C[1]	
OUT3_OE				0126[1]	
OUT4_OE				012B[1]	
OUT5_OE				0130[1]	
OUT6_OE				013A1]	
LOL_PLL[D:A]	High	Y	Y	000D[3:0], 0142[3:0]	Maskable separately for each DSPLL
LOS_XAXB	High	N	Y	000C[1], 0141[6]	Maskable
SYSINCAL	High	N	N	000C[0]	Automatic, not user-controllable or maskable

6.5.7 Output Buffer Voltage Selection

The power supply setting is used to calculate VCM and amplitude levels for the various output logic options. The OUTx_VDD_SEL_EN is always enabled and set to a logic 1. The power supply voltages on the VDDOx pins should match the voltage settings used in CBPro. Register values should be updated if any changes are made to the VDDOx voltages.

Table 6.13. Output Driver Voltage Selection

Setting Name	Reg Address	Descrption
OUT0_VDD_SEL_EN	0x0115 [3]	These bits are set to 1 and should not be changed.
OUT1_VDD_SEL_EN	0x011A [3]	
OUT2_VDD_SEL_EN	0x011F [3]	
OUT3_VDD_SEL_EN	0x0129 [3]	
OUT4_VDD_SEL_EN	0x012E [3]	
OUT5_VDD_SEL_EN	0x0133 [3]	
OUT6_VDD_SEL_EN	0x013D [3]	
OUT0_VDD_SEL	0x0115 [5:4]	These bits are set by CBPro to match the expected VDDOx voltage. 0: 3.3V, 1: 1.8V, 2: 2.5V, 3: Reserved.
OUT1_VDD_SEL	0x011A [5:4]	
OUT2_VDD_SEL	0x011F [5:4]	
OUT3_VDD_SEL	0x0129 [5:4]	
OUT4_VDD_SEL	0x012E [5:4]	
OUT5_VDD_SEL	0x0133 [5:4]	
OUT6_VDD_SEL	0x013D [5:4]	

7. Digitally Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in pre-defined steps defined by frequency step words (FSTEPW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in either Free Run or locked mode. The DCO mode is mainly used in IEEE1588 (PTP) applications where a clock needs to be generated based on recovered timestamps. In this case timestamps are recovered by the PHY/MAC. A processor containing servo software controls the DCO to close the timing loop between the master and slave IEEE1588 nodes. The processor has the option of using the FINC/FDEC pin controls to update the DCO frequency or by controlling it through the serial interface. Note that the maximum FINC/FDEC update rate, by either hardware or software, is 1 MHz. See *AN909* for additional details.

Note: DCO mode is not available when in free run.

7.1 Frequency Increment/Decrement Using Pin Controls

Controlling the output frequency with pin controls (FINC/FDEC) is available on the Si5348. This feature involves asserting the FINC or FDEC pins to increment or decrement the DSPLL frequency. The DSPLL selection is done through SPI commands M_FSTEP_MSK_PLLx. A set of mask bits selects the DSPLL(s) that is affected by the frequency change. The frequency step words (FSTEPW) defines the amount of frequency change for each FINC or FDEC. The FSTEPW may be written once or may be changed after every FINC/FDEC assertion. Both the FINC and FDEC inputs are rising-edge-triggered and must meet the Minimum Pulse Width specifications. The FINC and FDEC pins can also be used to trigger a frequency change. Note that both the FINC and FDEC register bits are rising-edge-triggered and self-clearing.

Note: When the FINC/FDEC pins on the Si5348 are unused, the FDEC pin must be pulled down with an external pull-down resistor or jumper. The FINC pin has an internal pull-down and may be left unconnected when not in use.

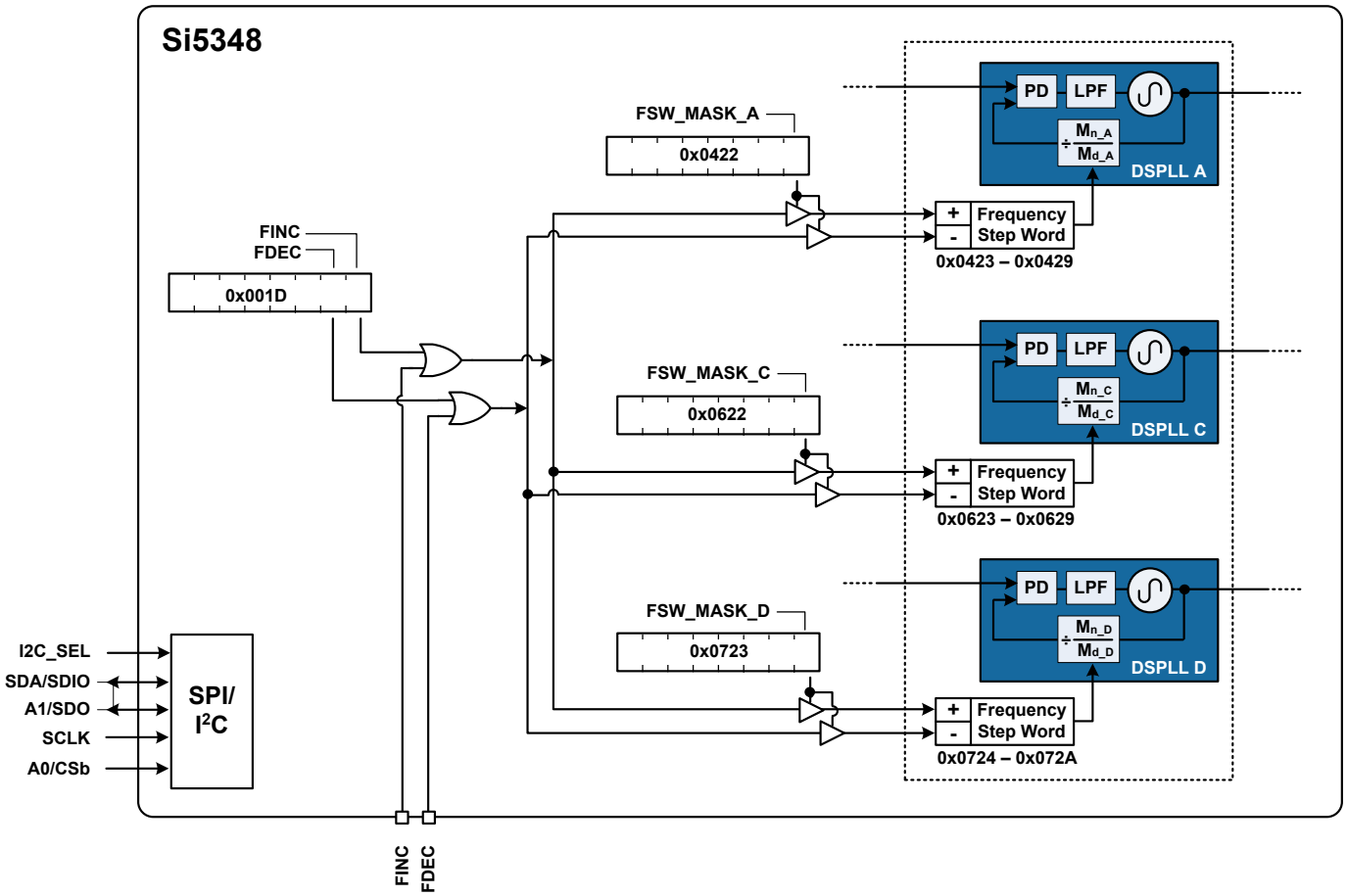


Figure 7.1. Controlling the DCO Mode by Serial Interface

Table 7.1. Frequency Increment/Decrement Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
FINC	001D[0]	Asserting this bit will increase the DSPLL output frequency by the frequency step word.
FDEC	001D[1]	Asserting this bit will decrease the DSPLL output frequency by the frequency step word.
M_FSTEPW_PLLA	0423[7:0] - 0429[7:0]	This is a 56-bit frequency step word for DSPLL A, C, D. The FSTEPW will be added or subtracted to the DSPLL output frequency during assertion of the FINC/FDEC bits or pins. The FSTEPW is calculated based on the frequency configuration and is easily calculated using ClockBuilder Pro utility.
M_FSTEPW_PLLC	0623[7:0] - 0629[7:0]	
M_FSTEPW_PLLD	0724[7:0] - 072A[7:0]	
M_FSTEP_MSK_PLLA	0422[0]	This mask bit determines if a FINC or FDEC affects DSPLL A, C, D. 0 = FINC/FDEC will increment/decrement the FSTEPW to the DSPLL. 1 = Ignores FINC/FDEC.
M_FSTEP_MSK_PLLC	0622[0]	
M_FSTEP_MSK_PLLD	0723[0]	

8. Serial Interface

Configuration and operation of the Si5348 is controlled by reading and writing registers using the I²C or SPI serial interface. The I2C_SEL pin selects between I²C or SPI operation. The Si5348 supports communication with either a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit. See Figure 21 for supported modes of operation and settings. The I²C pins are open drain and are ESD clamped to 3.3 V, regardless of the host supply level. The I²C pins are clamped to 3.3 V so that they may be externally pulled up to 3.3 V regardless of IO_VDD_SEL (in register 0x0943).

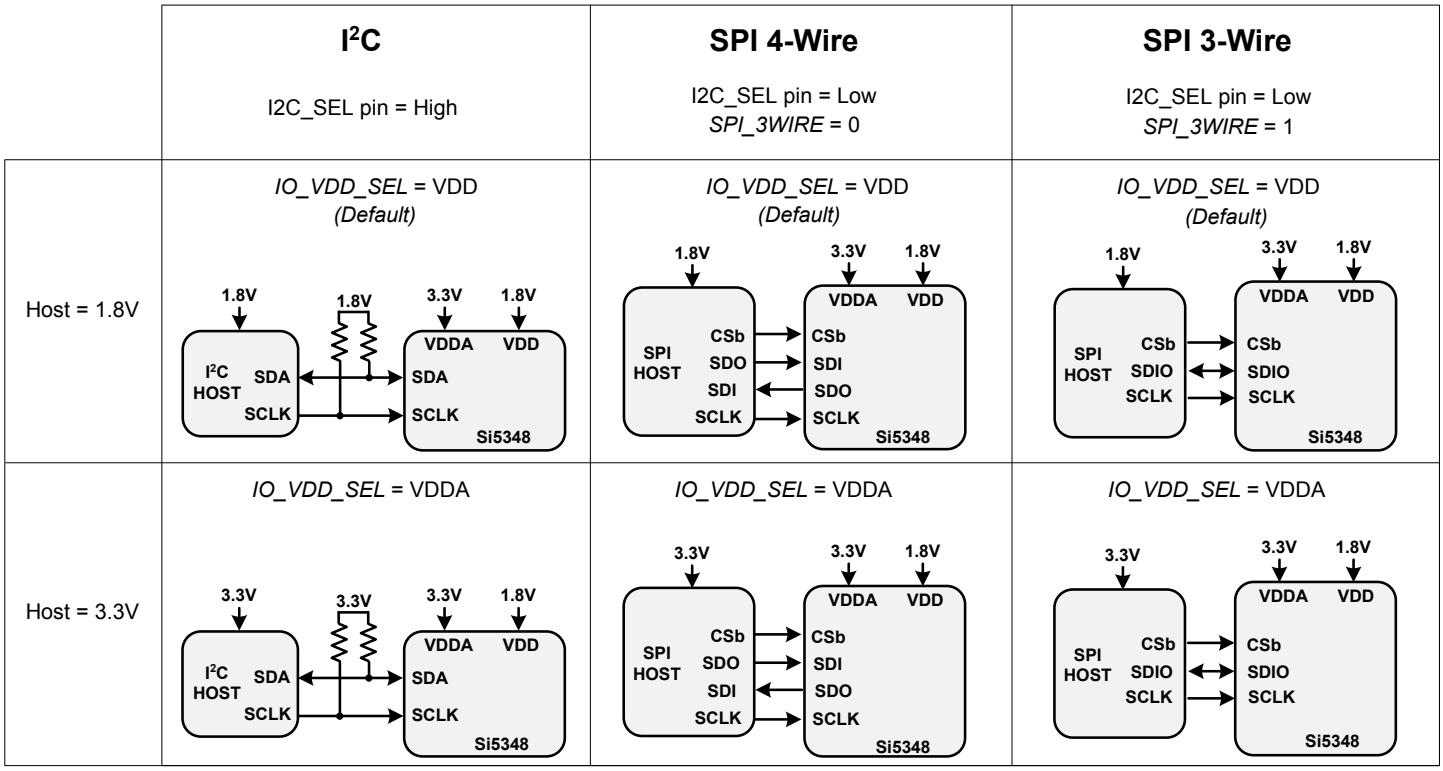


Figure 8.1. I²C/SPI Device Connectivity Configurations

The table below lists register settings of interest for the I²C/SPI.

If neither serial interface is used, pull pins I2C_SEL, A1/SDO, A0/CSb, SDA/SDIO, and SCLK low. Note that the Si5348 is not I2C failsafe upon loss of power. Applications that require failsafe operation should isolate the device from a shared I2C bus.

Table 8.1. I2C/SPI Register Settings

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
IO_VDD_SEL	0x0943[0]	This bit determines whether the VDD or VDDA supply voltage is used for the serial port, control pins and status pin voltage references. The IO_VDD_SEL configuration bit optimizes the V_{IL}, V_{IH}, V_{OL}, and V_{OH} thresholds to match the VDDS voltage. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the deviceVDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5348 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.
SPI_3WIRE	0x002B[3]	The SPI_3WIRE configuration bit selects the option of 4-wire or 3-wire SPI communication. By default, this configuration bit is set to the 4-wire option. In this mode the Si5348 will accept write commands from a 4-wire or 3- wire SPI host allowing configuration of device registers. For full bidirectional communication in 3-wire mode, the host must write the SPI_3WIRE configuration bit to “1”.

8.1 I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. The I2C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in the figure called I²C Write Operation in this section. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I2C specification as shown in the figure below. Two address select bits (A0, A1) are provided allowing up to four Si5348 devices to communicate on the same bus. This also allows four choices in the I2C address for systems that may have other overlapping addresses for other I²C devices.

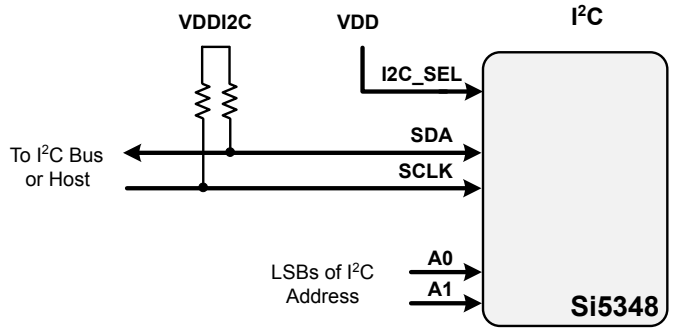


Figure 8.2. I²C Configuration

The 7-bit slave device address of the Si5348 consists of a 5-bit fixed address plus two pins that are selectable for the last two bits, as shown in the figure below.

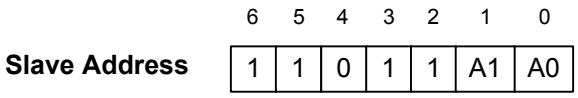


Figure 8.3. 7-bit I²C Slave Address Bit-Configuration

Data is transferred MSB first in 8-bit words as specified by the I2C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in the figure titled SPI Interface Connections in 8.2 SPI Interface. A write-burst operation is also shown where subsequent data words are written using to an auto-incremented address.

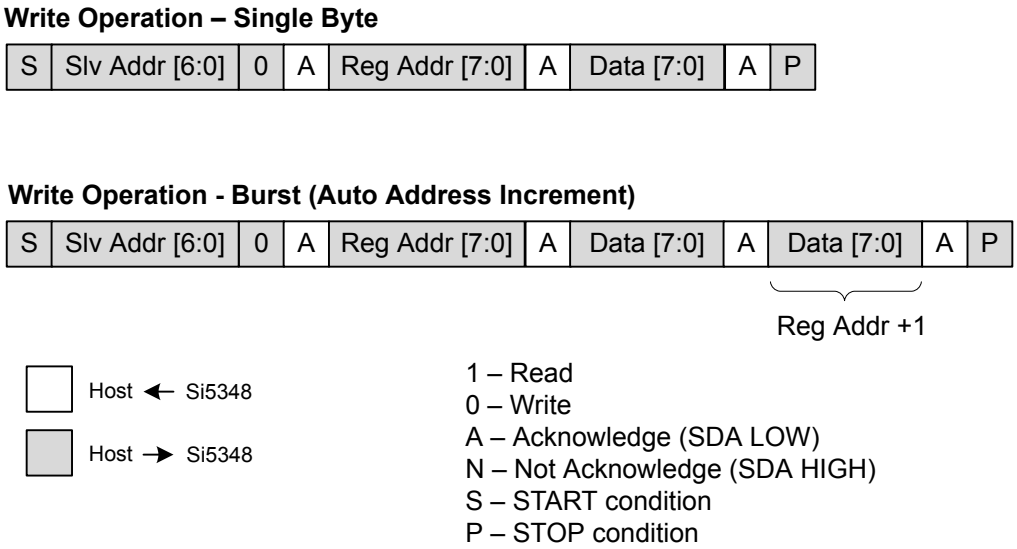
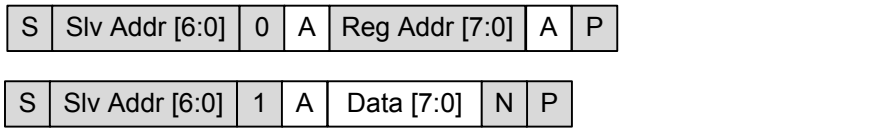


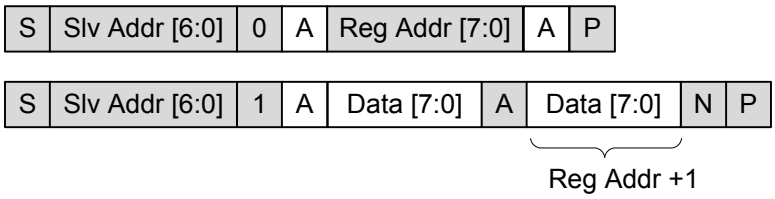
Figure 8.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the figure below.

Read Operation – Single Byte



Read Operation - Burst (Auto Address Increment)



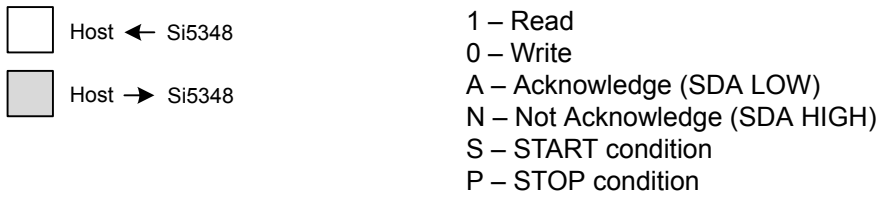


Figure 8.5. I^2C Read Operation

8.2 SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit. The 4-wire interface consists of a clock input (SCLK), a chip select input (CSb), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in the figure below.

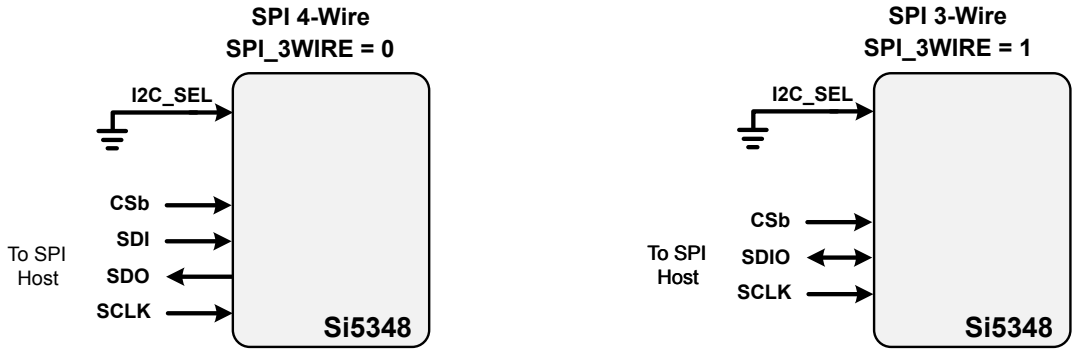


Figure 8.6. SPI Interface Connections

Table 8.2. SPI Command Format

Instruction	Ist Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Note:

1. X = don't care (1 or 0).
2. The Burst Write Command is terminated by de-asserting /CSb (/CSb = high).
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a "Set Address" command followed by a "Write Data" or "Read Data" command. The 'Write Data + Address Increment' or "Read Data + Address Increment" commands are available for cases where multiple byte operations in sequential address locations is necessary. The "Burst Write Data" instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. The figure below shows an example of writing three bytes of data using the write commands. As can be seen, the "Write Burst Data" command is the most efficient method for writing data to sequential address locations. The second figure below provides a similar comparison for reading data with the read commands. Note that there is no equivalent burst read; the read increment function is used in this case.

‘Set Address’ and ‘Write Data’

‘Set Addr’	Addr [7:0]	‘Write Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Write Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Write Data’	Data [7:0]

‘Set Address’ and ‘Write Data + Address Increment’

‘Set Addr’	Addr [7:0]	‘Write Data + Addr Inc’	Data [7:0]
‘Write Data + Addr Inc’	Data [7:0]		
‘Write Data + Addr Inc’	Data [7:0]		

‘Burst Write Data’

‘Burst Write Data’	Addr [7:0]	Data [7:0]	Data [7:0]	Data [7:0]

Figure 8.7. Example Writing Three Data Bytes using the SPI Write Commands

‘Set Address’ and ‘Read Data’

‘Set Addr’	Addr [7:0]	‘Read Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Read Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Read Data’	Data [7:0]

‘Set Address’ and ‘Read Data + Address Increment’

‘Set Addr’	Addr [7:0]	‘Read Data + Addr Inc’	Data [7:0]
‘Read Data + Addr Inc’	Data [7:0]		
‘Read Data + Addr Inc’	Data [7:0]		

Figure 8.8. Example of Reading Three Data Bytes Using the SPI Read Comments

The timing diagrams for the SPI commands are shown in the following figures.

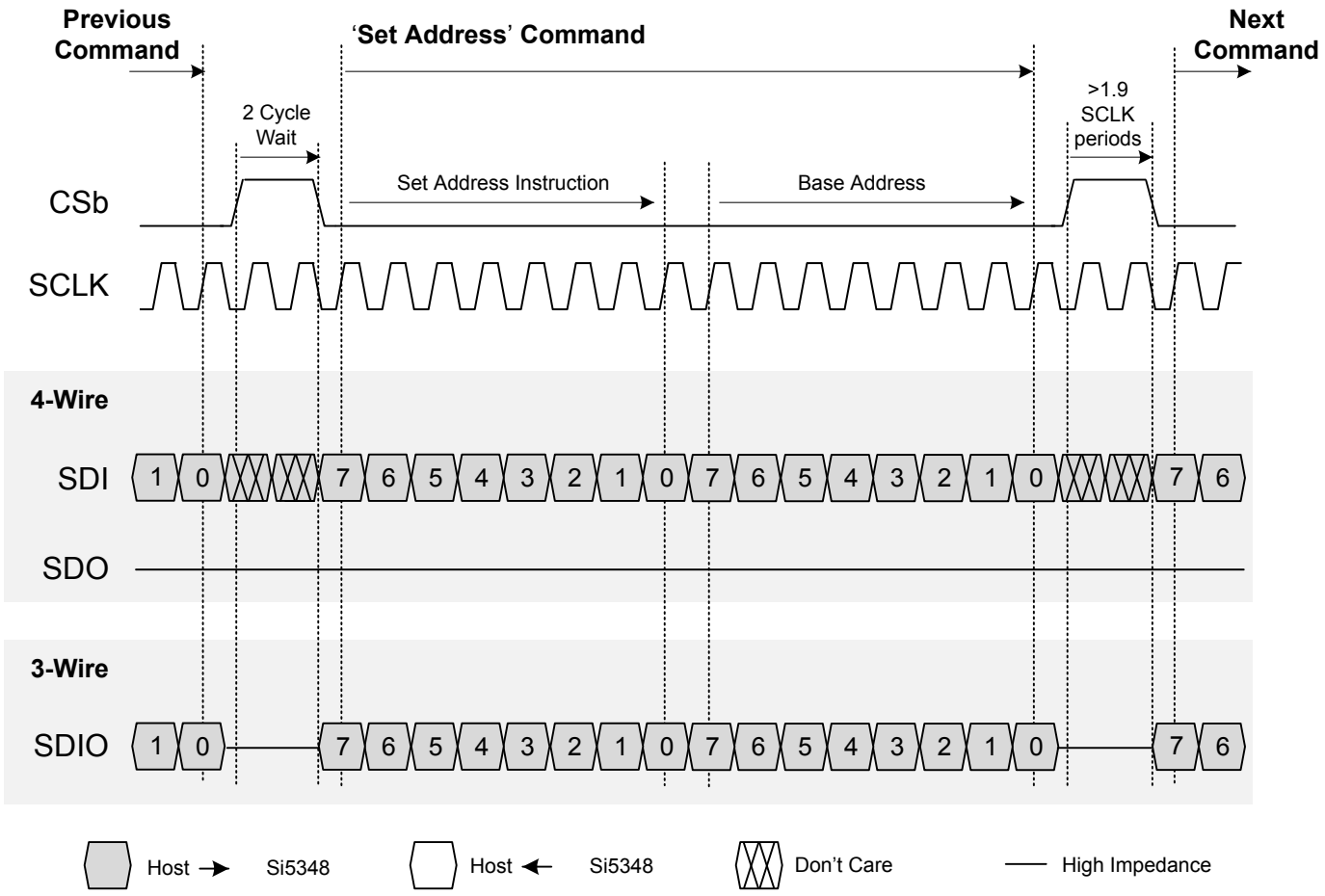


Figure 8.9. SPI "Set Address" Command Timing

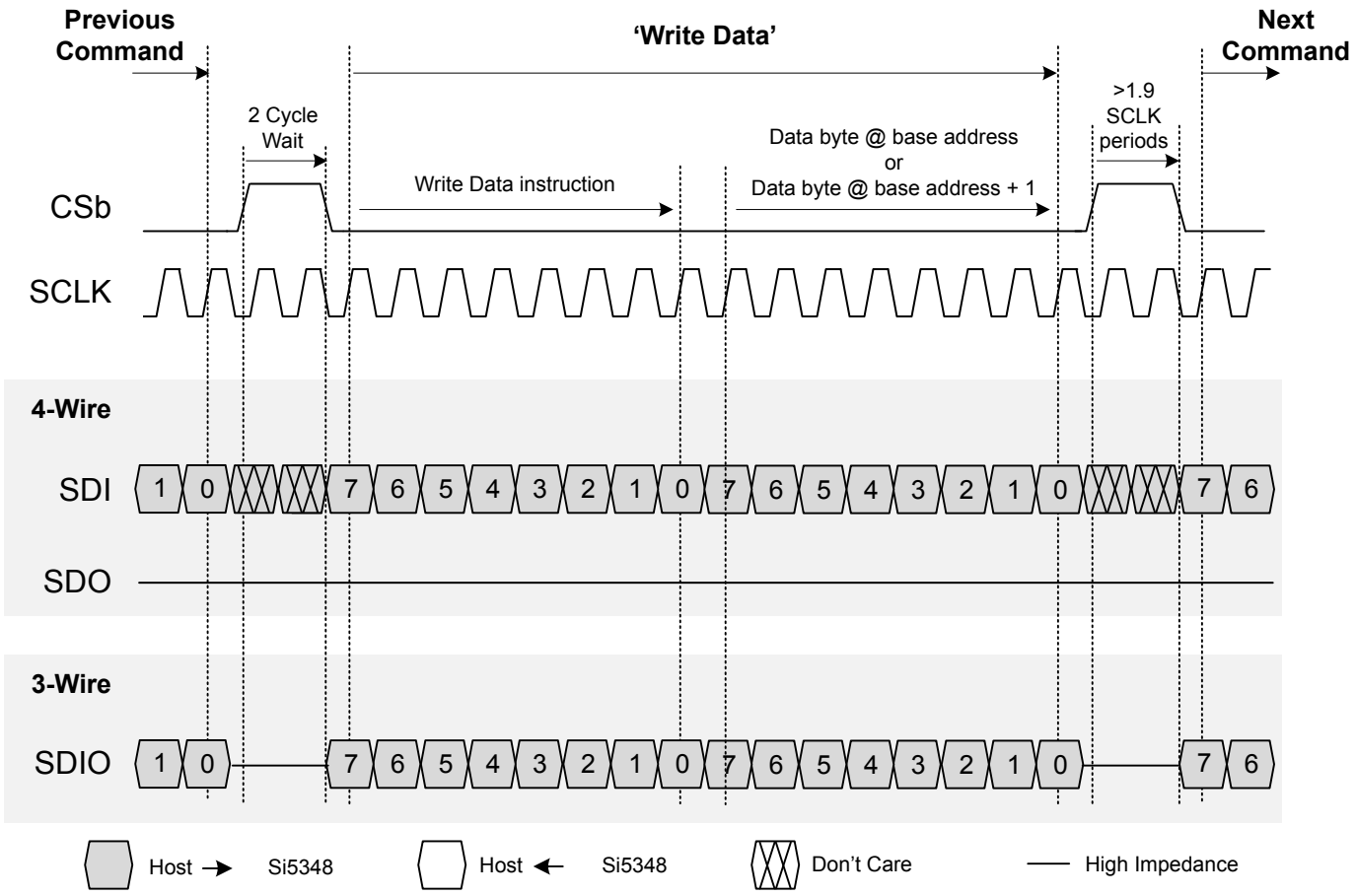


Figure 8.10. SPI "Write Data" and "Write Data + Address Increment" Instruction Timing

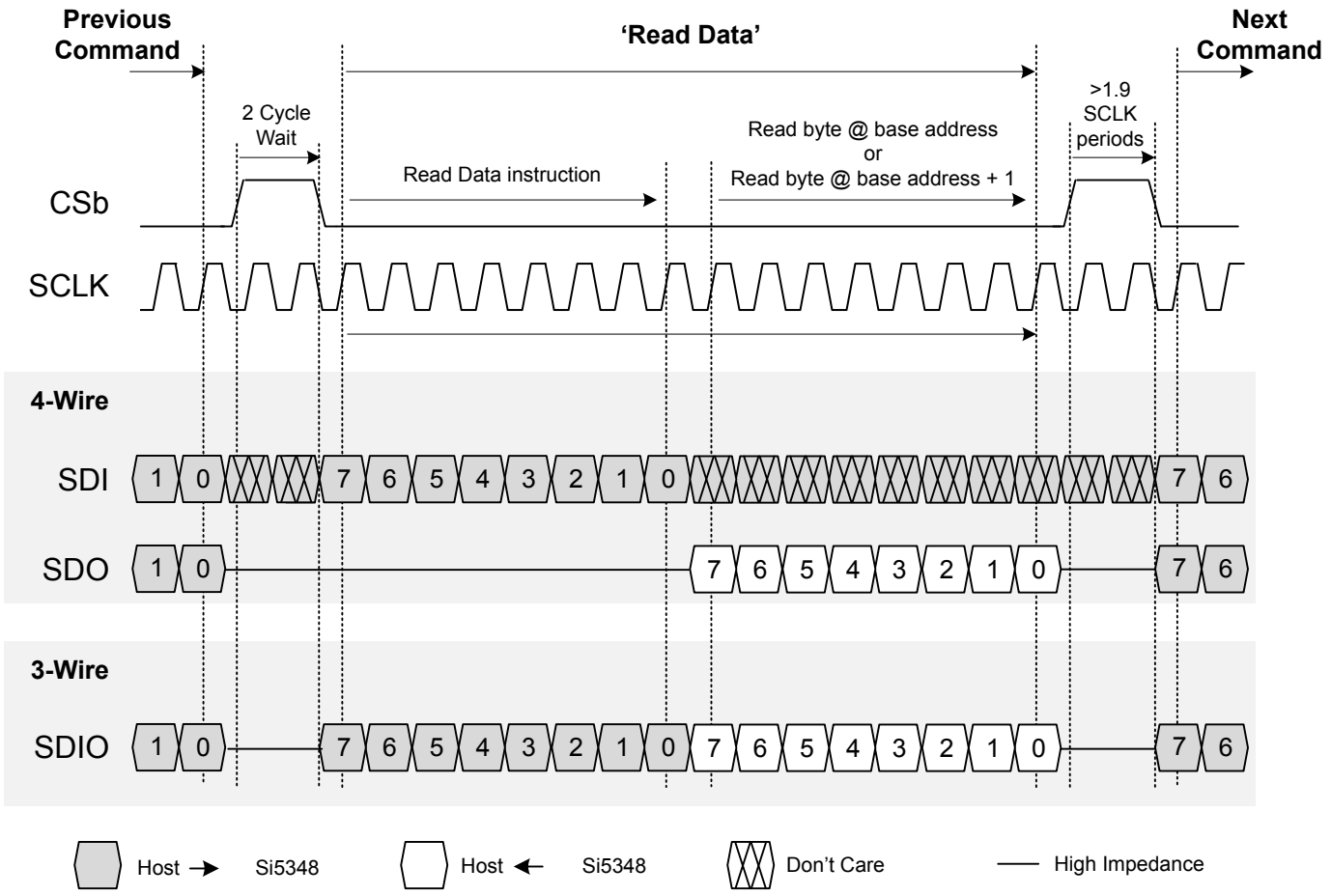


Figure 8.11. SPI "Read Data" and "Read Data + Address Increment" Instruction Training

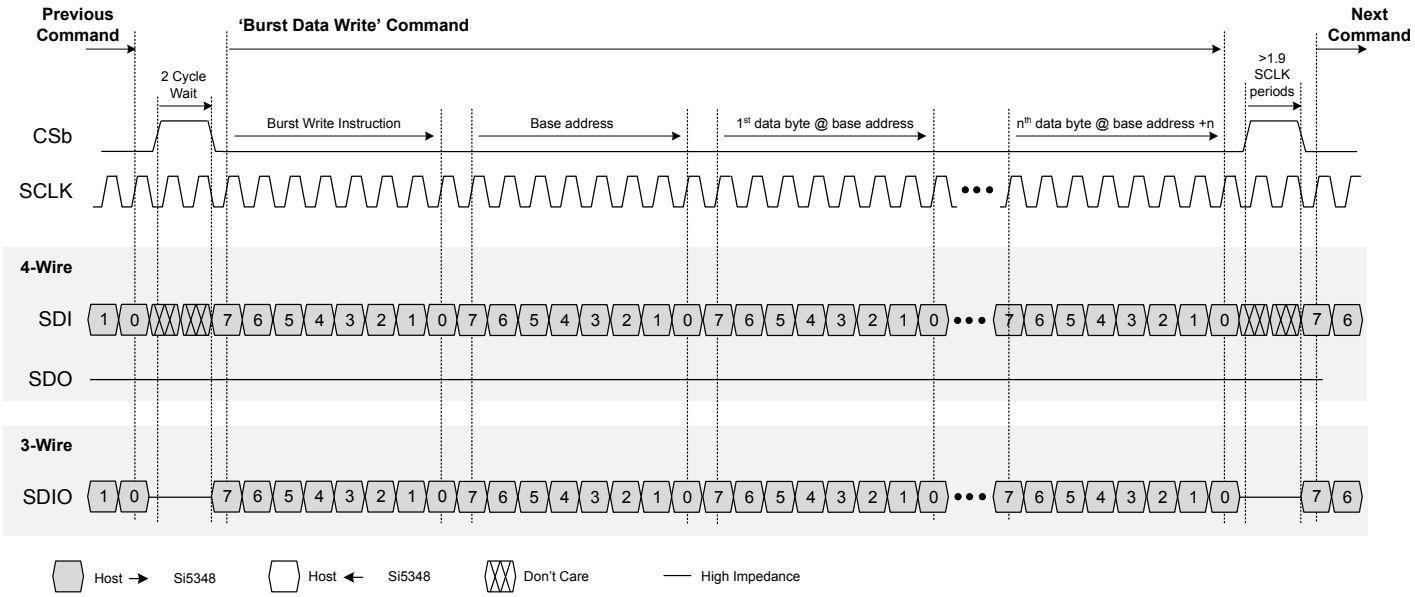


Figure 8.12. SPI "Burst Data Write" Instruction Timing

Note that for all SPI communication the chip select (CS) must be high for the minimum time period between commands. When chip select goes high it indicates the termination of the command. The SCLK can be turned off between commands, particularly if there are very long delays between commands.

9. Field Programming

To simplify design and software development of systems using the Si5348, a field programmer is available in addition to the evaluation board. The ClockBuilder Pro Field Programmer supports both “in-system” programming (for devices already mounted on a PCB), as well as “in-socket” programming of Si5348 devices. Refer to https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software for information about this kit.

10. Recommended Crystals and External Oscillators

10.1 External Reference (XA/XB, REF/REFb)

The external crystal at the XA/XB pins determines jitter performance of the output clocks, and the external reference clock at the REF/REFb pins determines the frequency accuracy, wander and stability during free-run or holdover modes. Jitter from the external clock on the REF/REFb pins will have little effect on the output jitter performance, depending upon the selected bandwidth.

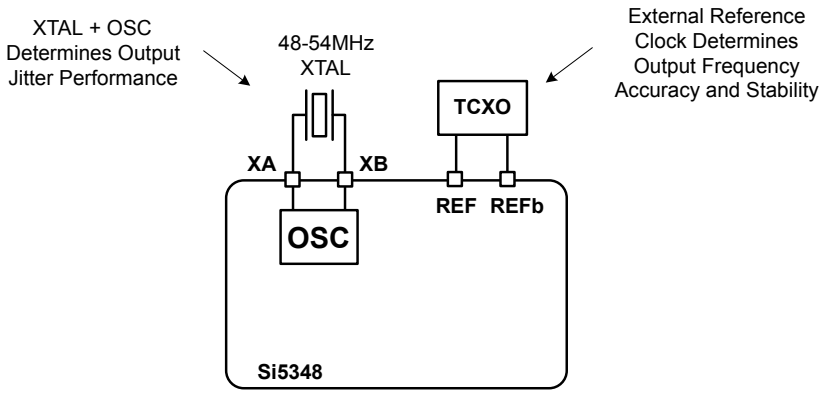


Figure 10.1. External Reference Connections

10.1.1 External Crystal (XA/XB)

The external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLLs. The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. Although ***not*** recommended, the device can also accommodate an external clock at the XA/XB pins instead of a crystal. Selection between the external crystal or clock is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in this mode. Chapter 11. Crystal and Device Circuit Layout Recommendations provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Contact Skyworks Applications Engineering for additional information.

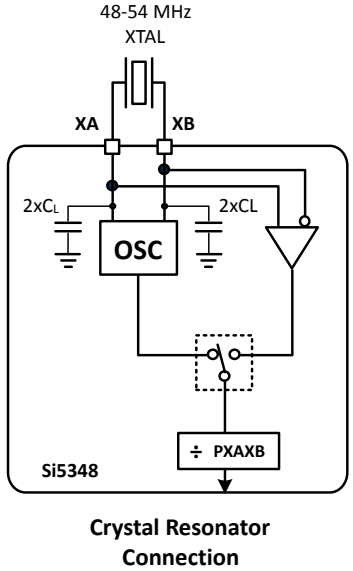


Figure 10.2. Crystal Resonator Connections

10.1.2 External Reference (REF/REFb)

The external reference at the REF/REFb pins is used to determine output frequency accuracy and stability during free-run and holdover modes. This reference is usually from a TCXO or OCXO and can be connected differentially or single-ended as shown in the figure below:

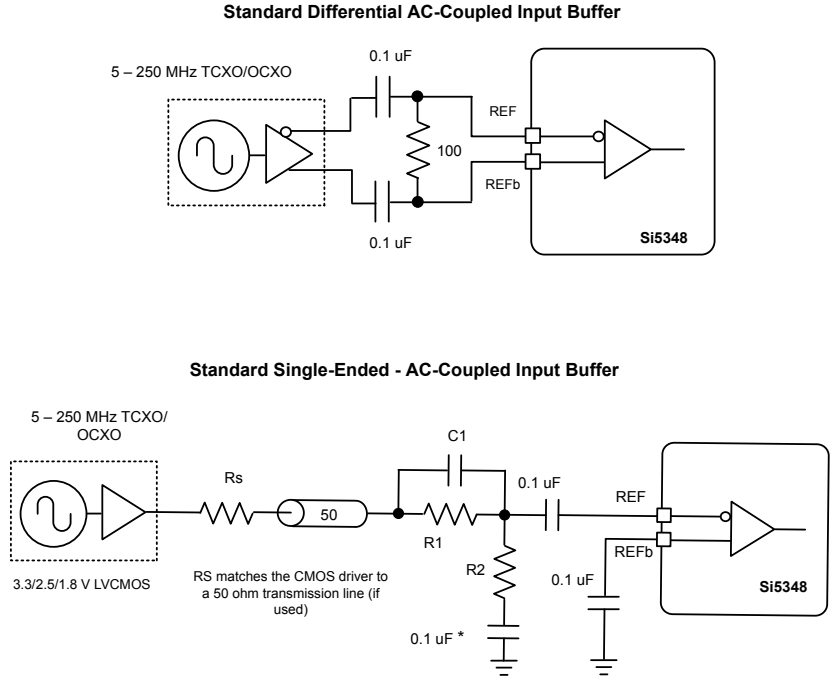


Figure 10.3. External Reference Connections

10.2 Recommended Crystals and External Oscillators

Please refer to the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for more information.

11. Crystal and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered include the following:

- Number and size of the ground vias for the Epad (see 12.4 Grounding Vias on pae 63.)
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace sampling
- Xtal signal coupling
- Xtal layout

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins to provide the best possible performance. The shield should not be connected to the ground plane(s), and the layers underneath should have as little area under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

11.1 64-Pin QFN Si5348 Layout Recommendations

This section details the recommended guidelines for the crystal layout of the 64-pin Si5348 device using an example 8-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals
- Layer 2: crystal shield
- Layer 3: ground plane
- Layer 4: power distribution
- Layer 5: power routing layer
- Layer 6: input clocks
- Layer 7: output clocks layer
- Layer 8: ground layer

The following figure shows the top layer layout of the Si5348 device mounted on the top PCB layer. The crystal area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

11.1.1 Si5348 Crystal Guidelines

The following are five recommended crystal guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. *Do not* connect the crystal's X1 or X2 pins to PCB ground.
3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal shield placed around and under the crystal. See the first figure below at the bottom left for an illustration of how to create a crystal shield by placing vias connecting the top layer traces to the shield layer underneath. Note the zoom view of the crystal shield layer on the next layer down is shown in the figure titled Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2) below.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digitial signals.
5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5348 should have all layers underneath the ground shield removed.

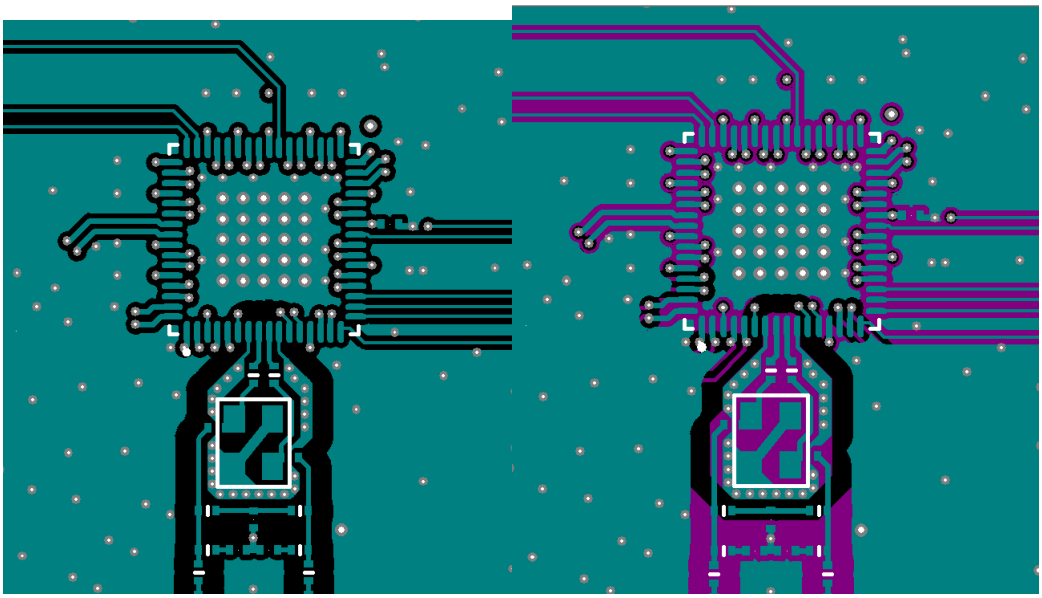


Figure 11.1. 64-pin Si5348 Crystal Layout Recommendations Top Layer (Layer 1)

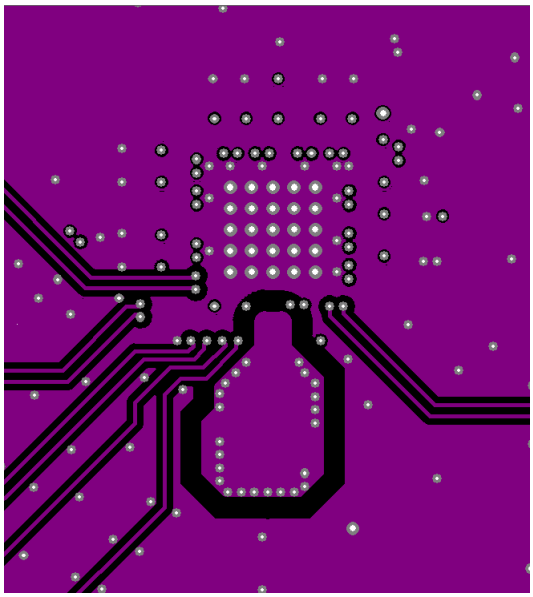


Figure 11.2. Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2)

The figure above shows the layer that implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2 they have a ground shield above below and on the sides for protection.

The figure below left is the ground plane and shows a void underneath the crystal shield. The figure below right is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued.

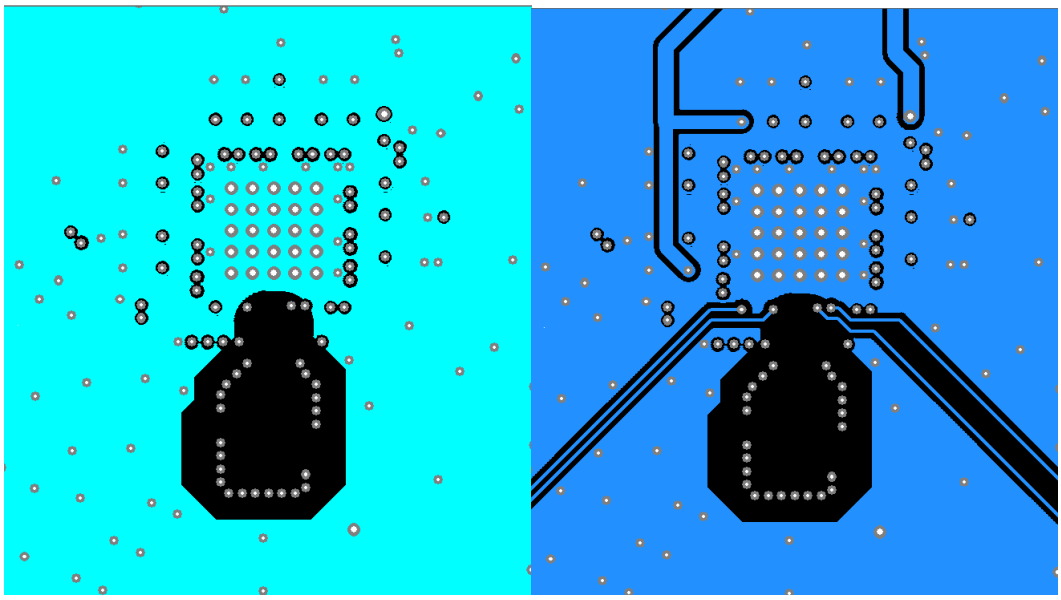


Figure 11.3. Crystal Ground Plane (Layer 3)

The figure below shows layer 5, which is the power plane with the power routed to the clock output power pins.

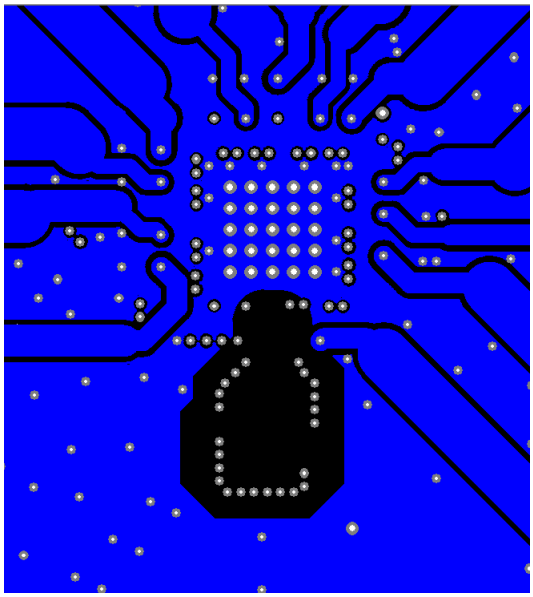


Figure 11.4. Layer 5 Power Routing on Power Plane (Layer 5)

The figure below is another ground plane similar to layer 3.

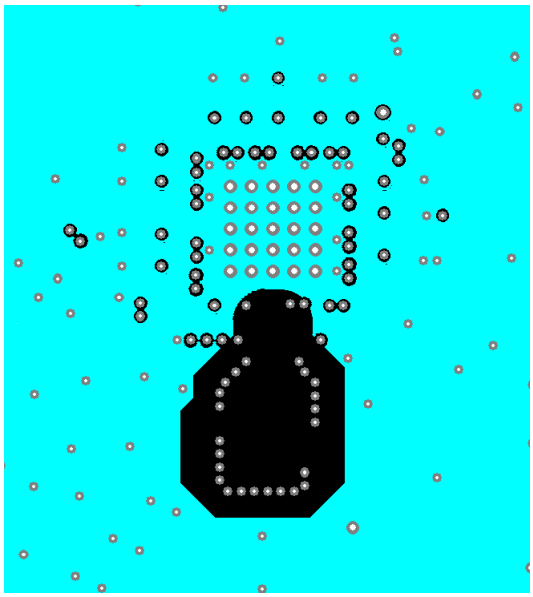


Figure 11.5. Ground Plane (Layer 6)

11.1.2 Si5348 Output Clocks

The figure below shows the output clocks. Similar to the input clocks, the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is a ground flooding between the clock output pairs to avoid crosstalk. There shouuld be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential paris has a low inductance path to the ground plane on layers 3 and 6.

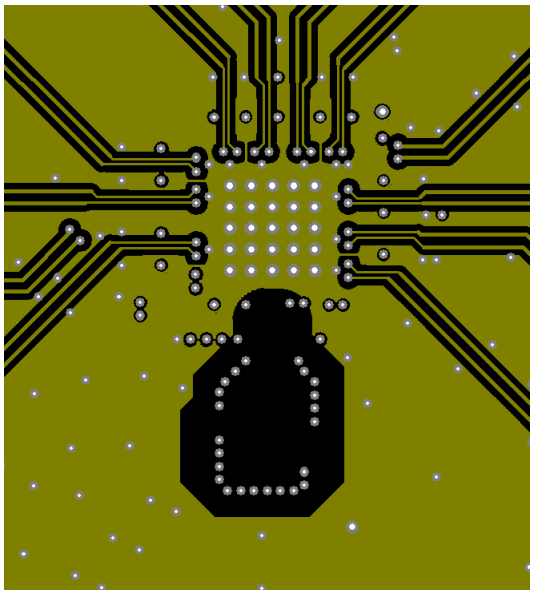


Figure 11.6. Output Clock Layer (Layer 7)

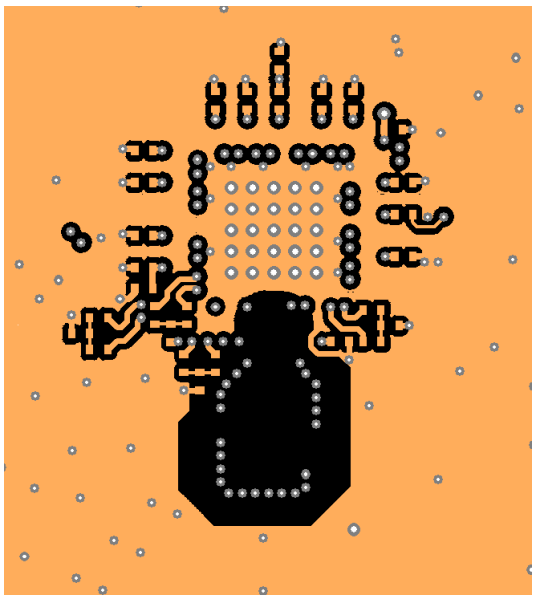


Figure 11.7. Bottom Layer Ground Flooded (Layer 8)

12. Power Management

12.1 Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed in the table below are used for powering down different features.

Table 12.1. Power Management Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5348	
PDN	0x001E[0]	This bit allows powering down the device. The serial interface remains powered during power down mode and the registers are available to be read and written.
OUT0_PDN	0x0112[0]	Powers down unused clock outputs.
OUT1_PDN	0x0117[0]	
OUT2_PDN	0x011C[0]	
OUT3_PDN	0x0126[0]	
OUT4_PDN	0x012B[0]	
OUT5_PDN	0x0130[0]	
OUT6_PDN	0x013A[0]	
OUT_PDN_ALL	0x0145[0]	Power down all output drivers

12.2 Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5348 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 1 µF 0402 ceramic capacitor on each VDD for optimal performance. It is also suggested to include an optional, single 0603 (resistor/ferrite) bead in series with each supply to enable additional filtering if needed.

12.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5348:

1. VDD = 1.8 V ± 5% (Core digital supply)
2. VDDA = 3.3 V ± 5% (Analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)
4. VDDS = 1.8/3.3 V ± 5% (Digital I/O supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. VDDS has no effect on output clock alignment.

If output-to-output alignmment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT_RST_ALL 0x001C[0] or Hard Reset 0x001E[1] register bits or driving the RSTb pin. Note tha using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

Note: One may observe that when powering up the VDD = 1.8 V rail first, that the VDDA = 3.3 V rail will initially follow the 1.8 V rail. Likewise, if the VDDA rail is powered down first then it will not drop far below VDD until VDD itself is powered down. This is due to the pad I/O circuits which have large MOSFET switches to select the local supply from either the VDD or VDDA rails. These devices are relatively large and yield a parasitic diode between VDD and VDDA. Please allow for both VDD and VDDA to power-up and power-down before measuring their respective voltages.

12.4 Grounding Vias

The pad on the bottom of the device functions as both the sole electrical ground annd prmary heat transfer path. Hence it is important to minmize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

13. Base vs. Factory Preprogrammed Devices

The Si5348 devices can be ordered as "base" or "factory-preprogrammed" (also known as "custom OPN") versions.

13.1 "Base" Devices (Also Known as "Blank" Devices)

- Example "base" orderable part numbers (OPNs) are of the form "Si5348A-B-GM" or "Si5348B-B-GM".
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.
- Base devices do not power up in a usable state (all output clocks are disabled).
- Base devices are, however, configured by default to use a 48 MHz crystal on the XAXB reference and a 1.8V compatible I/O voltage setting for the host I2C/SPI interface.
- Additional programming of a base device is mandatory to achieve a usable configuration.
- See the online lookup utility at https://www.skyworksinc.com/en/Application-Pages/Timing-Lookup-Customize to access the default configuration plan and register settings for any base OPN.

13.2 "Factory Preprogrammed" (Custom OPN) Devices

- Factory preprogammed devices using a "custom OPN", such as Si5348A-B-xxxxx-GM, where "xxxxx" is a sequence of characters assigned by Skyworks for each customer-specific configuration. These characters are referred to as the "OPN ID." Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XAXB referencec frequency/type, the input reference, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file that Skyworks uses to preprogram all devices with custom orderable part number ("custom OPN").
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: https://www.skyworksinc.com/en/Application-Pages/Timing-Lookup-Customize.
- Custom OPN devices include a device top mark that includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both "base" and "factory preprogrammed" devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see 4.2.2 NVM Programming).

14. Register Map

14.1 Register Map Overview and Default Settings Values

The Si5348 family parts have large register maps that are divided into separate “Pages” of register banks. This allows more register addresses than either the I2C or SPI serial interface standards 8-bit addressing provide. Each page has a maximum of 256 addresses, however not all addresses are used on every page. Every register has a maximum data size of 8-bits, or 1 byte. Writing the page number to the 8-bit serial interface address of 0x01 on any page (0x0001, 0x0101, 0x0201, etc.) updates the page selection for subsequent register reads and writes. For example, to access the value in register 0x040E, it is first necessary to write the page value 0x04 to serial interface register address 0x01. At this point, the value of serial interface address 0x0E (0x040E) may be read or written. Note that is it not necessary to write the page select register again when accessing other registers on the same page. Similarly, the read-only DEVICE_READY status is available from every page at serial interface address 0xFE (0x00FE, 0x01FE, 0x02FE, etc.).

It is recommended to use dynamic Read-Modify-Write methods when writing to registers which contain multiple settings, such as register 0x0011. To do this, first read the current contents of the register. Next, update only the select bit or bits that are being modified. This may involve using both logical AND and logical OR operations. Finally, write the updated contents back to the register. Writing to pages, registers, or bits not documented below may cause undesired behavior in the device.

Details of the register and settings information are organized hierarchically below. To find the relevant information for your application, first choose the section corresponding to the base part number, Si5348 for your design. Then, choose the section under that for the page containing the desired register(s).

Default register contents and settings differ for each device part number, or OPN. This information may be found by searching for the Custom OPN for your device using the link below. Both Base/Blank and Custom OPNs are available there. See the previous section on “Base vs. Factory Preprogrammed Devices" for more information on part numbers. The Private Addendum to the datasheet lists the default settings and frequency plan information. You must be logged into the Skyworks website to access this information. The Public addendum gives only the general frequency plan information https://www.skyworksinc.com/en/Application-Pages/Timing-Lookup-Customize.

Table 14.1. Register Map Page Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, and other configuration
Page 1	0100h	256	Output clock configuration
Page 2	0200h	512	P and R dividers, user scratch area
Page 3	0300h	768	Internal divider value updates
Page 4	0400h	1024	DSPLLA
Page 5	0500h	1280	DSPLLB (Reference DSPLL)
Page 6	0600h	1536	DSPLLC,
Page 7	0700h	1792	DSPLLD,
Page 9	0900h	2304	Control IO configuration
Page A	0A00h	2560	Internal divider enables
Page B	0B00h	2816	Internal clock disables and control

14.2 Si5348 Register Map

14.2.1 Page 0 Registers Si5348

Table 14.2. Register 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Select” register is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 14.3. Register 0x0002-0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x48	Four-digit "base" part number, one nibble per digit. Example: Si5348A-D-GM. The base part number (OPN) is 5348, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Table 14.4. Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/synthesis mode. 0 = A 1 = B 2 = C 3 = D

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 14.5. Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5348A-**D**12345-GM, the device revision is D and stored as 3.

Table 14.6. Register 0x0006-0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0006	3:0	R	SPECIAL	ClockBuilder Pro version that was used to generate the NVM image. Major.Minor.Revision.Special
0x0006	7:4	R	REVISION	
0x0007	7:0	R	MINOR	
0x0008	0	R	MINOR	
0x0008	4:1	R	MAJOR	
0x0008	7:5	R	TOOL	
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (-40 °C to 85 °C) ambient conditions.
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5348A-D12345-GM.

Applies to a factory pre-programmed OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.

Si5348A-D-GM.

Applies to a "base" or "blank" OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5348 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 14.7. Register 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address. Note this register is not bank burnable.

I2C Base Address Value = 0x6C

Table 14.8. Register 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	7:6	R	LOS_CMOS	01 is a LOS on IN3 10 is a LOS on IN4 11 is a LOS on IN3 and IN4

Bit 1 is the LOS status monitor for the XTAL at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I2C serial port.

Table 14.9. Register 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input [Ref, 2, 1, 0] is currently LOS.
0x000D	7:4	R	OOF	1 if the clock input [Ref, 2, 1, 0] is currently OOF.

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Reference Input (REF) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Table 14.10. Register 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL is out of lock.
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL is in holdover (or free run).

DSPLL_A corresponds to bit 0,4.

DSPLL_B (Reference) corresponds to bit 1,5.

DSPLL_C corresponds to bit 2,6.

DSPLL_D corresponds to bit 3,7.

Table 14.11. Register 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4.

DSPLL_B (Reference) corresponds to bit 5.

DSPLL_C corresponds to bit 6.

DSPLL_D corresponds to bit 7.

Table 14.12. Register 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIME-OUT_FLG	Sticky version of SMBUS_TIME-OUT. Write a 0 to this bit to clear.
0x0011	7:6	R/W	LOS_CMOS_FLG	01 LOS has been detected on IN3 in the past. 10 LOS has been detected on IN4 in the past.

These are sticky flag versions of 0x000C. They are cleared by writing zero to the bit that has been set.

Table 14.13. Register 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	Sticky version of LOS. Write a 0 to this bit to clear.
0x0012	7:4	R/W	OOF_FLG	Sticky version of OOF. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4].
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5].
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6].
- Reference (REF) corresponds to LOS_FLG 0x0012 [3].

Table 14.14. Register 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	1 if the DSPLL was unlocked.
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	1 if the DSPLL was in holdover (or freerun).

Sticky flag versions of address 0x000E.

- DSPLL_A corresponds to bit 0,4.
- DSPLL_B (Reference) corresponds to bit 1,5.
- DSPLL_C corresponds to bit 2,6.
- DSPLL_D corresponds to bit 3,7.

Table 14.15. Register 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	1 if the DSPLL internal calibration was busy.

These are sticky-flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B (Reference) corresponds to bit 5

DSPLL C corresponds to bit 6

DSPLL D corresponds to bit 7

Table 14.16. Register 0x0016

Reg Address	Bit Field	Type	Setting Name	Description
0x0016	3:0	R/W	LOL_ON_HOLD_PLL[D:A]	Set by CBPro.

Table 14.17. Register 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt.
0x0017	1	R/W	LOSXAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt.
0x0017	3	R/W	XAXB_ERR_INTR_MSK	1 to mask the XAXB error
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt.
0x0017	7:6	R/W	LOS_CMOS_INTR_MSK	1 to mask the LOS_CMOS_INTR_MSK from causing an interrupt.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt. The default for this trigger is 0x035.

Table 14.18. Register 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1: To mask the clock input LOS flag.
0x0018	7:4	R/W	OOF_INTR_MSK	1: To mask the clock input OOF flag.

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018[0], OOF_IN_INTR_MSK 0x0018[4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018[1], OOF_IN_INTR_MSK 0x0018[5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018[2], OOF_IN_INTR_MSK 0x0018[6]
- Reference (REF) corresponds to LOS_IN_INTR_MSK 0x0018[3]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 14.19. Register 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1: To mask the clock input LOL flag.
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1: To mask the holdover flag.

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019[0], HOLD_INTR_MSK_PLL 0x0019[4]
- DSPLL B (Reference) corresponds to LOL_INTR_MSK_PLL 0x0019[1]
- DSPLL C corresponds to LOL_INTR_MSK_PLL 0x0019[2], HOLD_INTR_MSK_PLL 0x0019[6]
- DSPLL D corresponds to LOL_INTR_MSK_PLL 0x0019[3], HOLD_INTR_MSK_PLL 0x0019[7]

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 14.20. Register 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_DSPLL[D:A]	1: To mask the DSPLL internal calibration busy flag.

DSPLL A corresponds to bit 0

DSPLL B (Reference) corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

Table 14.21. Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect. 1: Initialize and calibrate the entire device. This will also align the outputs from the four DSPLLs. The calibration range is ±2000 ppm.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA.
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB (Reference).
0x001C	3	S	SOFT_RST_PLLC	1 initialize and calibrate DSPLLC.
0x001C	4	S	SOFT_RST_PLLD	1 initialize and calibrate DSPLLD.

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x514, 0x0614, and 0x0715. Note that unlike the other SOFT_RST_PLLx bits, a SOFT_RST_PLL_B will affect all of the DSPLLs.

Table 14.22. Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement.

FINC and FDEC will affect the M dividers depending on how their corresponding M_FSTEP_MSK_PLLx bits are programmed.

Table 14.23. Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1: To put the device into low power mode.
0x001E	1	R/W	HARD_RST	0: No reset. 1: Causes hard reset. The same as power up except that the serial port access is not held at reset.
0x001E	2	S	SYNC	Resets all output R dividers to the same state.

Table 14.24. Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI.

Table 14.25. Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable. 1: To enable LOS for a clock input.
0x002C	4	R/W	LOSXAXB_DIS	0: For disable. 1: To enable LOS for the XAXB input.

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Reference (REF): LOS_EN[3]

Table 14.26. Register 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec. 1: For 100 msec. 2: For 200 msec. 3: For one second.
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above.
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above.
0x002D	7:6	R/W	LOS3_VAL_TIME	Reference Clock, same as above.

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 14.27. Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	Calculated by CBPro based on value selected.
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 14.28. Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	Calculated by CBPro based on value selected.
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 14.29. Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	Calculated by CBPro based on value selected.
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 14.30. Register 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	Calculated by CBPro based on value selected.
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for the Reference given a particular frequency plan.

Table 14.31. Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	Calculated by CBPro based on value selected.
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 14.32. Register 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	Calculated by CBPro based on value selected.
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 14.33. Register 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	Calculated by CBPro based on value selected.
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 14.34. Register 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	Calculated by CBPro based on value selected.
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for the Reference, given a particular frequency plan.

Table 14.35. Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable.
0x003F	6:4	R/W	FAST_OOF_EN	1: To enable.

Table 14.36. Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: for IN0 1: for IN1 2: for IN2 3: for Ref 4: for XAXB

Table 14.37. 0x0041–0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 14.38. Register 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.

Table 14.39. Register0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Set Threshold. Range is up to +/-500 ppm in steps of 1/16 ppm.

Table 14.40. Register 0x0050 OOF_ON_LOS

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro

Table 14.41. Register 0x0051-0x0053 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	7:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	7:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm

Reg Address	Bit Field	Type	Setting Name	Description
0x0053	7:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	7:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for the reference, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 14.42. Register 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	7:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	7:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	7:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	7:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for the reference, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 14.43. Register 0x0059 FAST OOFx_DETWIN_SEL

Reg Address	Bit Field	Type	Setting Name	Description
0x0059	1:0	R/W	FAST_OOF0_DETWIN_SEL	The fast OOF0 detection window selection. Set by CBPro.
0x0059	2:3	R/W	FAST_OOF1_DETWIN_SEL	The fast OOF1 detection window selection. Set by CBPro
0x0059	4:5	R/W	FAST_OOF2_DETWIN_SEL	The fast OOF2 detection window selection. Set by CBPro
0x0059	6:7	R/W	FAST_OOF3_DETWIN_SEL	The fast OOF3 detection window selection. Set by CBPro

Table 14.44. Register 0x005A-0x006 OOFx_RATIO_REF

Reg Address	Bit Field	Type	Setting Name	Description
0x005A	25:0	R/W	OOF0_RATIO_REF	Set by CBPro.
0x005E	25:0	R/W	OOF1_RATIO_REF	Set by CBPro.
0x0062	25:0	R/W	OOF2_RATIO_REF	Set by CBPro.
0x0066	25:0	R/W	OOF3_RATIO_REF	Set by CBPro.

Table 14.45. Register 0x0092

Reg Address	Bit Field	Type	Setting Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	0: To disable. 1: To enable.
0x0092	1	R/W	LOL_FST_EN_PLLB	0: To disable. 1: To enable.
0x0092	2	R/W	LOL_FST_EN_PLLC	0: To disable. 1: To enable.
0x0092	3	R/W	LOL_FST_EN_PLLD	0: To disable. 1: To enable.

Table 14.46. Register 0x0092 Fast LOL Detection Window Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0093	3:0	R/W	LOL_FST_DET-WIN_SEL_PLLA	Sets detection window for the Fast LOLA.
0x0093	7:4	R/W	LOL_FST_DET-WIN_SEL_PLLB	Sets detection window for the Fast LOLB.
0x0094	3:0	R/W	LOL_FST_DET-WIN_SEL_PLLC	Sets detection window for the Fast LOLC.
0x0094	7:4	R/W	LOL_FST_DET-WIN_SEL_PLLD	Sets detection window for the Fast LOLD.

Table 14.47. Register 0x0095 Fast LOL Detectection Value Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0095	1:0	R/W	LOL_FST_VAL-WIN_SELL_PLLA	0: 1 1: 16 2:128 3: 1024
0x0095	3:2	R/W	LOL_FST_VAL-WIN_SELL_PLLB	
0x0095	5:4	R/W	LOL_FST_VAL-WIN_SELL_PLLC	
0x0095	7:6	R/W	LOL_FST_VAL-WIN_SELL_PLLD	

Table 14.48. Register 0x0096-0x0097 Fast LOL Set Threshold Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	0: 0.2 ppm 1: 0.6 ppm 2: 2 ppm 3: 6 ppm 4: 20 ppm 5: 60 ppm 6: 200 ppm 7: 600 ppm 8: 2000 ppm 9: 6000 ppm 10: 20000 ppm
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	
0x0097	3:0	R/W	LOL_FST_SET_THR_SEL_PLLC	
0x0097	7:4	R/W	LOL_FST_SET_THR_SEL_PLLD	

Table 14.49. Register 0x0098-0x0099 Fast LOL Clear Threshold Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	0: 0.2 ppm 1: 0.6 ppm 2: 2 ppm 3: 6 ppm 4: 20 ppm 5: 60 ppm 6: 200 ppm 7: 600 ppm 8: 2000 ppm 9: 6000 ppm 10: 20000 ppm
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	
0x0099	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLC	
0x0099	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLD	

Table 14.50. Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	3:0	R/W	LOL_SLW_EN_PLL[D:A]	0: To disable LOL. 1: To enable LOL.

DSPLL A corresponds to bit 0

DSPLL B (Reference) corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 14.51. Register 0x009B-0x009C Slow LOL Detection Window Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x009B	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLA	Sets detection window for the Slow LOLA
0x009B	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLB	Sets detection window for the Slow LOLB
0x009C	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLC	Sets detection window for the Slow LOLC
0x009C	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLD	Sets detection window for the Slow LOLD

Table 14.52. Register 0x009D Slow LOL Detection Value Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	1:0	R/W	LOL_SLW_VAL-WIN_SEL_PLLA	Sets the number of detection windows in slow LOL validation window. Set by CBPro.
0x009D	3:2	R/W	LOL_SLW_VAL-WIN_SEL_PLLB	Sets the number of detection windows in slow LOL validation window. Set by CBPro.
0x009D	5:4	R/W	LOL_SLW_VAL-WIN_SEL_PLLC	Sets the number of detection windows in slow LOL validation window. Set by CBPro.
0x009D	7:6	R/W	LOL_SLW_VAL-WIN_SEL_PLLD	Sets the number of detection windows in slow LOL validation window. Set by CBPro.

Table 14.53. Register 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.

Table 14.54. Register 0x009F LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009F	3:0	R/W	LOL_SLW_SET_THR_PLLC	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm.

The following are the thresholds for the value that is placed in the four bits for DSPLLs.

- 0=0.2 ppm
- 1=0.6 ppm
- 2=2 ppm
- 3=6 ppm
- 4=20 ppm
- 5=60 ppm
- 6=200 ppm
- 7=600 ppm
- 8=2000 ppm
- 9=6000 ppm
- 10=20000 ppm

Table 14.55. Register 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds for the reference. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

Table 14.56. Register 0x00A1 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1	3:0	R/W	LOL_SLW_CLR_THR_PLLC	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

The following are the thresholds for the value that is placed in the four bits for DSPLLs. ClockBuilder Pro sets these values.

- 0=0.2 ppm
- 1=0.6 ppm
- 2=2 ppm
- 3=6 ppm
- 4=20 ppm
- 5=60 ppm
- 6=200 ppm
- 7=600 ppm
- 8=2000 ppm
- 9=6000 ppm
- 10=20000 ppm

Table 14.57. Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	3:0	R/W	LOL_TIMER_EN_PLL	0: To disable. 1: To enable.

LOL_TIMER extends the time after the LOL clear threshold has been met that LOL stays active.

DSPLL A bit 0

DSPLL B (Reference) bit 1

DSPLL C bit 2

DSPLL D bit 3

Table 14.58. Register 0x00A4-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLA	Calculated by CBPro based on value selected.
0x00A5	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A6	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLA	
0x00A7	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLA	

Table 14.59. Register 0x00A9-0x00AC LOL Clear Delay DSPLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLB	Calculated by CBPro based on value selected.
0x00AA	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLB	
0x00AB	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLB	
0x00AC	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLB	

Table 14.60. Register 0x00AE-0x00B1 LOL Clear Delay DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x00AE	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLC	Calculated by CBPro based on value selected.
0x00AF	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLC	
0x00B0	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLC	
0x00B1	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLC	

Table 14.61. Register 0x00B3-0x00B6 LOL Clear Delay DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x00B3	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLD	Calculated by CBPro based on value selected.
0x00B4	15:8	R/W	LOL_CLR_DELAY_DIV256_PLLD	
0x00B5	23:16	R/W	LOL_CLR_DELAY_DIV256_PLLD	
0x00B6	28:24	R/W	LOL_CLR_DELAY_DIV256_PLLD	

Table 14.62. Register 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	5:0	R	ACTIVE_NVM_BANK	0x00 when no NVM has been burned 0x03 when 1 NVM bank has been burned 0x0F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. Contact Skyworks.

Table 14.63. Register 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See 4.2.2 NVM Programming.

Table 14.64. Register 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	1: To download NVM.

Table 14.65. Register 0x00E5 FASTLOCK_EXTEND_EN_PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x00E5	4	R/W	FASTLOCK_EXTEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EXTEND_EN_PLLB	
0x00E5	6	R/W	FASTLOCK_EXTEND_EN_PLLC	
0x00E5	7	R/W	FASTLOCK_EXTEND_EN_PLLD	

Table 14.66. Register 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x00E6	28:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_ EXTEND_SCL_PLLx.

Table 14.67. Register 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x00EA	28:0	R/W	FASTLOCK_EXTEND_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_ EXTEND_SCL_PLLx.

Table 14.68. Register 0x00EE-0x00F1 FASTLOCK_EXTEND_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x00EE	28:0	R/W	FASTLOCK_EXTEND_PLLC	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_ EXTEND_SCL_PLLx.

Table 14.69. Register 0x00F2-0x00F5 FASTLOCK_EXTEND_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x00F2	28:0	R/W	FASTLOCK_EXTEND_PLLD	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_ EXTEND_SCL_PLLx.

Table 14.70. Register 0x00F6 Interurrpt

Reg Address	Bit Field	Type	Setting Name	Description
0x00F6	0	R	REG_0XF7_INTR	0: No alarm 1: Alarm
0x00F6	1	R	REG_0XF8_INTR	0: No alarm 1: Alarm
0x00F6	2	R	REG_0XF9_INTR	0: No alarm 1: Alarm

Table 14.71. Register 0x00F7

Reg Address	Bit Field	Type	Setting Name	Description
0x00F7	0	R	SYSINCAL_INTR	0: Interrupt not set 1: Interrupt set
0x00F7	1	R	LOSXO_INTR	
0x00F7	2	R	LOSREF_INTR	
0x00F7	3	R	LOLIL_INTR	
0x00F7	4	R	LOSVCO_INTR	
0x00F7	5	R	SMBUS_TIME_OUT_INTR	
0x00F7	7:6	R	LOS_CMOS_CK_INTR[4:3]	

Table 14.72. Register 0x00F8

Reg Address	Bit Field	Type	Setting Name	Description
0x00F8	3:0	R	LOS_INTR[IN3:IN0]	0: Interrupt not set 1: Interrupt set
0x00F8	7:4	R	OOF_INTR[IN3:IN0]	

Table 14.73. Register 0x00F9 HOLD(A,B,C,D) abd LOL(A,B,C,D) Interrupt Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x00F9	0	R	LOL_INTR_PLLA	0: No alarm 1: Alarm
0x00F9	1	R	LOL_INTR_PLLB	0: No alarm 1: Alarm
0x00F9	2	R	LOL_INTR_PLLC	0: No alarm 1: Alarm
0x00F9	3	R	LOL_INTR_PLLD	0: No alarm 1: Alarm
0x00F9	4	R	HOLDL_INTR_PLLA	0: No alarm 1: Alarm
0x00F9	5	R	HOLDL_INTR_PLLB	0: No alarm 1: Alarm
0x00F9	6	R	HOLDL_INTR_PLLC	0: No alarm 1: Alarm
0x00F9	7	R	HOLDL_INTR_PLLD	0: No alarm 1: Alarm

Table 14.74. Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready. 0xF3 when device is not ready.

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is most useful after powerup, after a hard reset 0x001E[1], or after an NVM write 0x00E3 to determine when the operation is complete. The “Device Ready” register is available on every page in the device at 0x##FE, where “##” represents the page address.

WARNING! Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming. Note that this includes writes to the PAGE register.

14.2.2 Page 1 Registers Si5348

Table 14.75. Register 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0: Disables all output drivers. 1: Pass through the output enables.

Table 14.76. Register 0x0108, 0x0112, 0x0117, 0x011C, 0x0126, 0x012B, 0x0130, 0x013A

Reg Address	Bit Field	Type	Setting Name	Description
0x0112	0	R/W	OUT0_PDN	0: To power up the regulator. 1: To power down the regulator. Clock outputs will be weakly pulled-low.
0x0117			OUT1_PDN	
0x011C			OUT2_PDN	
0x0126			OUT3_PDN	
0x012B			OUT4_PDN	
0x0130			OUT5_PDN	
0x013A			OUT6_PDN	
0x0112	1	R/W	OUT0_OE	0: To disable the output. 1: To enable the output.
0x0117			OUT1_OE	
0x011C			OUT2_OE	
0x0126			OUT3_OE	
0x012B			OUT4_OE	
0x0130			OUT5_OE	
0x013A			OUT6_OE	
0x0112	2	R/W	OUT0_RDIV_FORCE	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2 ClockBuilder Pro sets this bit automatically when Rx = 2.
0x0117			OUT1_RDIV_FORCE	
0x011C			OUT2_RDIV_FORCE	
0x0126			OUT3_RDIV_FORCE	
0x012B			OUT4_RDIV_FORCE	
0x0130			OUT5_RDIV_FORCE	
0x013A			OUT6_RDIV_FORCE	

The output drivers are all identical. See 6.2 Performance Guidelines for Outputs.

Table 14.77. Register 0x0109, 0x0113, 0x0118, 0x011D, 0x0127, 0x012C, 0x0131, 0x0136 Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT OUT4_FORMAT OUT5_FORMAT OUT6_FORMAT	0: Reserved. 1: Differential Normal mode. 2: Differential Low-Power mode. 3: Reserved. 4: LVCMOS single ended. 5: LVCMOS (+pin only). 6: LVCMOS (-pin only). 7: Reserved.
0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN OUT4_SYNC_EN OUT5_SYNC_EN OUT6_SYNC_EN	0: Disable. 1: Enable.
0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	5:4	R/W	OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE OUT4_DIS_STATE OUT5_DIS_STATE OUT6_DIS_STATE	Determines the state of an output driver when disabled, selectable as: 0: Disable low. 1: Disable high.
0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	7:6	R/W	OUT0_CMOS_DRV OUT1_CMOS_DRV OUT2_CMOS_DRV OUT3_CMOS_DRV OUT4_CMOS_DRV OUT5_CMOS_DRV OUT6_CMOS_DRV	LVCMOS output impedance drive strength see the table titled LVCMOS Drive Strength Control Registers in 6.4.2 LVCMOS Output Impedance and Drive Strength Selection.

The output drivers are all identical.

Table 14.78. Register 0x010A, 0x0114, 0x0119, 0x011E, 0x0128, 0x012D, 0x0132, 0x0137 Output

Reg Address	Bit Field	Type	Setting Name	Description
0x0114 0x0119 0x011E 0x0128 0x012D 0x0132 0x013C	3:0	R/W	OUT0_CM OUT1_CM OUT2_CM OUT3_CM OUT4_CM OUT5_CM OUT6_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 39.
0x0114 0x0119 0x011E 0x0128 0x012D 0x0132 0x013C	6:4	R/W	OUT0_AMPL OUT1_AMPL OUT2_AMPL OUT3_AMPL OUT4_AMPL OUT5_AMPL OUT6_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 39.

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Table 14.79. Register 0x010B, 0x0115, 0x011A, 0x011F, 0x0129, 0x012E, 0x0133, 0x0138 R-Divider Mux

Reg Address	Bit Field	Type	Setting Name	Description
0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x0138	1:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL OUT4_MUX_SEL OUT5_MUX_SEL OUT6_MUX_SEL	Output driver 0 input mux select.This selects the source of the output clock. 0: DSPLL A 1: Reserved 2: DSPLL C 3: DSPLL D
0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x0138	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV OUT4_INV OUT5_INV OUT6_INV	0: CLK and CLK not inverted 1: CLK inverted 2: CLK and CLK inverted 3: CLK inverted These bits have no effect on differential outputs.

Each output can be connected to any of the four DSPLLs using the OUTx_MUX_SEL. The output drivers are all identical.

Table 14.80. Register 0x0115, 0x011A, 0x011F, 0x0129, 0x012E, 0x0133, 0x013D, OUTx VDD Selection and Voltage Setting

Reg Address	Bit Field	Type	Setting Name	Descrption
0x0115	3	R/W	OUT0_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled
0x0115	5:4	R/W	OUT0_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x011A	3	R/W	OUT1_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled
0x011A	5:4	R/W	OUT1_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x011F	3	R/W	OUT2_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled
0x011F	5:4	R/W	OUT2_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0129	3	R/W	OUT3_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled
0x0129	5:4	R/W	OUT3_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x012E	3	R/W	OUT4_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled
0x012E	5:4	R/W	OUT4_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0133	3	R/W	OUT5_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled

Reg Address	Bit Field	Type	Setting Name	Descrption
0x0133	5:4	R/W	OUT5_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x013D	3	R/W	OUT6_VDD_SEL_EN	0: Do not set to 0 1: Standard VDD selection enabled
0x013D	5:4	R/W	OUT6_VDD_SEL	0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved

Table 14.81. Register 0x013F

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	11:0	R/W	OUTX_ALWAYS_ON	Set by CBPro.

Table 14.82. Register 0x0141 OUT_DIS_MSK_

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	0	R/W	OUT_DIS_MSK_PLLA	Set by CBPro.
0x0141	2	R/W	OUT_DIS_MSK_PLLC	Set by CBPro.
0x0141	3	R/W	OUT_DIS_MSK_PLLD	Set by CBPro.
0x0141	5	R/W	OUT_DIS_LOL_MSK	Set by CBPro.
0x0141	6	R/W	OUT_DIS_MSK_LOS-XAXB	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOS-XAXB. 1: All outputs remain enabled during LOSXAXB condition.
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	Set by CBPro.

Table 14.83. Register 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	3:0	R/W	OUT_DIS_MSK_LOL_PLL[D:A]	0: LOL will disable all connected outputs. 1: LOL does not disable any outputs.
0x0142	4	R/W	OUT_DIS_MSK_HOLD_PLLA	Set by CBPro.
0x0142	6	R/W	OUT_DIS_MSK_HOLD_PLLC	Set by CBPro.

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	7	R/W	OUT_DIS_MSK_HOLD_PLLD	Set by CBPro.

- Bit 0 LOL_DSPLL_A mask
- Bit 2 LOL_DSPLL_C mask
- Bit 3 LOL_DSPLL_D mask

Table 14.84. Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Setting Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0: No effect. 1: All drivers powered down.

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Table 14.85. Register 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input. This is valid with external clock sources, not crystals. • 0=pre-scale value 1 • 1=pre-scale value 2 • 2=pre-scale value 4 • 3=pre-scale value 8 Note that changing this register during operation may cause indefinite loss of lock unless the guidelines are followed for changing registers while in operation.

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Changing Registers while Device in Operation are followed.

Table 14.86. Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	Value calculated by CBPro.
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in 4.2 Changing Registers while Device in Operation are followed.

Table 14.87. Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	Values calculated by CBPro.
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in 4.2 Changing Registers while Device in Operation are followed.

Table 14.88. Si5348 P1-P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3_NUM (Reference)	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN (Reference)	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in 4.2 Changing Registers while Device in Operation are followed. Note that P3 corresponds to the Reference divider value.

Table 14.89. Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value. 1: Update P-divider value.
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Table 14.90. Register 0x0231 P0 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 14.91. Register 0x0232 P1 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	4	R/W	P1_FRAC_EN	(IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division

Table 14.92. Register 0x0233 P2 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 14.93. Register 0x0234 P3 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Note that these controls are not needed when following the guidelines in 4.2 Changing Registers while Device in Operation. Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA, SOFT_RST_PLLB, etc., as these do not update the Px_NUM or Px_DEN values. Note that P3 corresponds to the Reference.

Table 14.94. Register 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	Values calculated by CBPro.
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Changing Registers while Device in Operation are followed.

Table 14.95. Register 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	Values calculated by CBPro.
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Changing Registers while Device in Operation are followed.

Table 14.96. 0x023F MXAXB_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 14.97. Register 0x0250-0x0252 R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x0250	7:0	R/W	R0_REG	24-bit Integer output divider divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x0251	15:8	R/W	R0_REG	
0x0252	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1-.R6 dividers follow the same format as the R0 divider described above.

Table 14.98. Si5348 R1-R6 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0253-0x0255	R1_REG	24-bit Integer Number	0x024A-0x024C
0x0256-0x0258	R2_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R3_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R4_REG	24-bit Integer Number	0x024A-0x024C
0x0262-0x0264	R5_REG	24-bit Integer Number	0x024A-0x024C
0x0268-0x026A	R6_REG	24-bit Integer Number	0x024A-0x024C

Table 14.99. Register 0x026B-0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, ULT.1A with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 14.100. Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5348B-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5348B-A12345-GM

Applies to a "custom": OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.

Si5348B-A-GM

Applies to a "base" or "non-custom" OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5348 but **exclude**any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 14.101. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	OPN Revision Number

Table 14.102. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	Part Configuration Identification Code.

Table 14.103. 0x028A-0x028D

Reg Address	Bit Field	Type	Setting Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	The OOF0 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	The OOF1 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	The OOF2 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	The OOF3 trigger threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 14.104. 0x028E-0x0291

Reg Address	Bit Field	Type	Setting Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	The OOF0 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	The OOF1 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	The OOF2 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	The OOF3 clear threshold extension (increases threshold precision from 2 ppm to 0.0625 ppm)

Table 14.105. Register 0x0294 -0x0295 FASTLOCK EXTEND SCL

Reg Address	Bit Field	Type	Setting Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Value calculated in CBPro based on parameter selected
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	Value calculated in CBPro based on parameter selected
0x0295	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLC	Value calculated in CBPro based on parameter selected

Reg Address	Bit Field	Type	Setting Name	Description
0x0295	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLD	Value calculated in CBPro based on parameter selected

Table 14.106. 0x0296 LOL SLW VALWIN SELX PLLx

Reg Address	Bit Field	Type	Setting Name	Description
0x0296	0	R/W	LOL_SLW_VALWIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VALWIN_SELX_PLLB	
0x0296	2	R/W	LOL_SLW_VALWIN_SELX_PLLC	
0x0296	3	R/W	LOL_SLW_VALWIN_SELX_PLLD	

Table 14.107. Register 0x0297 -0x02B1 FASTLOCK_DLY_ONSW

Reg Address	Bit Field	Type	Setting Name	Description
0x0297	0	R/W	FASTLOCK_DLY_ONSW_EN_PLLA	0: Disables FASTLOCK_DLY_ONSW_EN PLLA 1: Enables FASTLOCK_DLY_ONSW_EN PLLA
0x0297	1	R/W	FASTLOCK_DLY_ONSW_EN_PLLB	0: Disables FASTLOCK_DLY_ONSW_EN PLLB 1: Enables FASTLOCK_DLY_ONSW_EN PLLB
0x0297	2	R/W	FASTLOCK_DLY_ONSW_EN_PLLC	0: Disables FASTLOCK_DLY_ONSW_EN PLLC 1: Enables FASTLOCK_DLY_ONSW_EN PLLC
0x0297	3	R/W	FASTLOCK_DLY_ONSW_EN_PLLD	0: Disables FASTLOCK_DLY_ONSW_EN PLLD 1: Enables FASTLOCK_DLY_ONSW_EN PLLD

Table 14.108. Register 0x0299 -0x02A3 FASTLOCK DLY ON

Reg Address	Bit Field	Type	Setting Name	Description
0x0299	0	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLA	0: Disables FASTLOCK_DLY_ON-LOL_PLLA 1: Enables FASTLOCK_DLY_ON-LOL_PLLA
0x0299	1	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLB	0: Disables FASTLOCK_DLY_ON-LOL_PLLB 1: Enables FASTLOCK_DLY_ON-LOL_PLLB
0x0299	2	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLC	0: Disables FASTLOCK_DLY_ON-LOL_PLLC 1: Enables FASTLOCK_DLY_ON-LOL_PLLC
0x0299	3	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLD	0: Disables FASTLOCK_DLY_ON-LOL_PLLD 1: Enables FASTLOCK_DLY_ON-LOL_PLLD
0x029A	19:0	R/W	FASTLOCK_DLY_ON-LOL_PLLA	Value calculated in CBPro based on parameter selected
0x029D	19:0	R/W	FASTLOCK_DLY_ON-LOL_PLLB	Value calculated in CBPro based on parameter selected
0x02A0	19:0	R/W	FASTLOCK_DLY_ON-LOL_PLLC	Value calculated in CBPro based on parameter selected
0x02A3	19:0	R/W	FASTLOCK_DLY_ON-LOL_PLLD	Value calculated in CBPro based on parameter selected
0x02A6	19:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	Value calculated in CBPro based on parameter selected
0x02A9	19:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	Value calculated in CBPro based on parameter selected
0x02AC	19:0	R/W	FAST-LOCK_DLY_ONSW_PLLC	Value calculated in CBPro based on parameter selected
0x02AF	19:0	R/W	FAST-LOCK_DLY_ONSW_PLLD	Value calculated in CBPro based on parameter selected

Table 14.109. Register 0x002B7 LOL_NOSIG_TIME_PLLA, B,C,D

Reg Address	Bit Field	Type	Setting Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	0: 1.7 sec 1: 107 ms 2: 67 ms 3: 417 µs
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	
0x02B7	5:4	R/W	LOL_NO-SIG_TIME_PLLC	
0x02B7	7:6	R/W	LOL_NO-SIG_TIME_PLLD	

Table 14.110. Register 0x002B8 LOL_LOS_REFCLK_PLLA, B,C,D

Reg Address	Bit Field	Type	Setting Name	Description
0x02B8	0	R	LOL__LOS_REFCLK_PLLA	0: No alarm 1: Alarm
0x02B8	1	R	LOL__LOS_REFCLK_PLLB	0: No alarm 1: Alarm
0x02B8	2	R	LOL__LOS_REFCLK_PLLC	0: No alarm 1: Alarm
0x02B8	3	R	LOL__LOS_REFCLK_PLLD	0: No alarm 1: Alarm

Table 14.111. Register 0x002B8 LOL_LOS_REFCLK_PLLA, B,C,D_FLG

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9	0	R/W	LOL__LOS_REFCLK_PLLA _FLG	0: No alarm 1: Alarm
0x02B9	1	R/W	LOL__LOS_REFCLK_PLLB_FLG	0: No alarm 1: Alarm
0x02B9	2	R/W	LOL__LOS_REFCLK_PLLC_FLG	0: No alarm 1: Alarm
0x02B9	3	R/W	LOL__LOS_REFCLK_PLLD_FLG	0: No alarm 1: Alarm

Table 14.112. Register 0x02BC LOS CMOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	1:0	R/W	LOS_CMOS_EN	0: Disable LOS 1: Enable LOS for a clock input

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	5:4	R/W	LOS_CMOS_EN_1HZ	0: Disable LOS for 1Hz input to PLLD, 1: Enable LOS for 1Hz input to PLLD

Note:
1. Bit Field [0] = IN3 and Bit Field [1] = IN4

Table 14.113. Register 0x02BD LOS CMOS VAL TIME

Reg Address	Bit Field	Type	Setting Name	Description
0x02BD	1:0	R/W	LOS_CMOS0_VAL_TIME	Value calculated in CBPro
0x02BD	3:2	R/W	LOS_CMOS1_VAL_TIME	Value calculated in CBPro

Table 14.114. Register 0x02BE - 0x02C1 LOS CMOS TRG_THR

Reg Address	Bit Field	Type	Setting Name	Description
0x02BE	15:0	R/W	LOS_CMOS0_TRG_THR (IN3)	Value calculated in CBPro based on parameter selected
0x02C0	15:0	R/W	LOS_CMOS1_TRG_THR (IN4)	Value calculated in CBPro based on parameter selected

Table 14.115. Register 0x02C2 - 0x02C4 LOS CMOS CLR_THR

Reg Address	Bit Field	Type	Setting Name	Description
0x02C2	15:0	R/W	LOS_CMOS0_CLR_THR (IN3)	Value calculated in CBPro based on parameter selected
0x02C4	15:0	R/W	LOS_CMOS1_CLR_THR (IN4)	Value calculated in CBPro based on parameter selected

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Table 14.116. Register 0x0302-0x0307, 0x030D-0x0312, 0x0318-0x031D, 0x0323-0x0328 Nx Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0302	7:0	R/W	N0_NUM	Value calculated by CBPro based on Frequency Plan.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			
0x030D	7:0	R/W	N1_NUM	Value calculated by CBPro based on Frequency Plan.
0x030E	15:8			
0x030F	23:16			
0x0310	31:24			
0x0311	39:32			
0x0312	43:40			
0x0318	7:0	R/W	N2_NUM	Value calculated by CBPro based on Frequency Plan.
0x0319	15:8			
0x031A	23:16			
0x031B	31:24			
0x031C	39:32			
0x031D	43:40			
0x0323	7:0	R/W	N3_NUM	Value calculated by CBPro based on Frequency Plan.
0x0324	15:8			
0x0325	23:16			
0x0326	31:24			
0x0327	39:32			
0x0328	43:40			

Table 14.117. Register 0x0308-0x030B, 0x0313-0x0316, 0x031E-0x0321, 0x0329-0x032C Nx Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x0308	7:0	R/W	N0_DEN	Value calculated by CBPro based on Frequency Plan.
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

Reg Address	Bit Field	Type	Setting Name	Description
0x0313	7:0	R/W	N1_DEN	Value calculated by CBPro based on Frequency Plan.
0x0314	15:8			
0x0315	23:16			
0x0316	31:24			
0x031E	7:0	R/W	N2_DEN	Value calculated by CBPro based on Frequency Plan.
0x031F	15:8			
0x0320	23:16			
0x0321	31:24			
0x0329	7:0	R/W	N3_DEN	Value calculated by CBPro based on Frequency Plan.
0x032A	15:8			
0x032B	23:16			
0x032C	31:24			

Table 14.118. Registers 0x030C DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to latch the N output divider registers into operation.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.119. Registers 0x0317 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0317	0	S	N1_UPDATE	Set this bit to latch the N output divider registers into operation.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. Because DSPLLB supplies the VCO frequency for all the DSPLLs, changing N1 will have an affect on all the DSPLLs.

Table 14.120. Registers 0x0322 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0322	0	S	N2_UPDATE	Set this bit to latch the N output divider registers into operation.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.121. Registers 0x032D DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x032D	0	S	N3_UPDATE	Set this bit to latch the N output divider registers into operation.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.122. Registers 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

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Table 14.123. Register 0x0407 Active Input Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Current input clock 0: for IN0 1: for IN1 2: for IN2 3: for REF

These bits indicate which input clock DSPLL A is currently selected. 0 for IN0; 1 for IN1; etc.

Table 14.124. Register 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	5:0	R/W	BW0_PLLA	Calculated by CBPro based on value selected.
0x0409	5:0	R/W	BW1_PLLA	
0x040A	5:0	R/W	BW2_PLLA	
0x040B	5:0	R/W	BW3_PLLA	
0x040C	5:0	R/W	BW4_PLLA	
0x040D	5:0	R/W	BW5_PLLA	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 14.125. Register 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	5:0	R/W	FAST-LOCK_BW0_PLLA	Calculated by CBPro based on value selected.
0x040F	5:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	5:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	5:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	5:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	5:0	R/W	FAST_BW5_PLLA	
0x0414	0	S	BW_UPDATE_PLLA	0: No effect. 1: Updates the Normal BW, Fastlock BW, and Exit from Holdover rate.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Table 14.126. Register 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	Values calculated by CBPro.
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.127. Register 0x041C-0x041F MA Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	Values calculated by CBPro.
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan annd are written into these registers.

Table 14.128. Register 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLLA M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.129. Register 0x0421 M Divider Fractional Control and Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	Managed by CBPro
0x0421	4	R/W	M_FRAC_EN_PLLA	0: Interger mode 1: Enable fractional modulator

Table 14.130. Register 0x0422 DSPLL A FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0422	1	R/W	MFSTEPW_DEN_PLLA	0: Modify numerator 1: Modify denominator

Table 14.131. Register 0x0423-0x0429 DSPLLA MA Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0415–0x041F.

Table 14.132. Register 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For REF 4-7: Reserved

This is the input clock selection for manual register-based clock selection.

Table 14.133. Register 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FASTLOCK_MAN_PLLA=0. 0: Disables auto fast lock 1: Enables auto fast lock when PLLA is out of lock.

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	1	R/W	FAST-LOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Table 14.134. DSPLLA Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Descrption
0x042C	0	R/W	HOLD_EN_PLLA	0: Holdover Disabled 1: Holdover Enabled. Standard setting.
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	0: Use Ramp Rate when exiting from Holdover 1: Standard PLL configuration when exiting from Holdover
0x042C	4	R/W	HOLD_EXITBW_SEL1_PLLA	This bit with HOLDEXIT_BW_SEL0_PLLA are set by CBPro to allow the bandwidth when exiting holdover to be set independent of the PLL bandwidth during other times of operation. CBPro sets this bit.
0x042C	7:5	R/W	RAMP_STEP_INTERVAL_PLLA	The ramp rate is selected when using CBPro.

Table 14.135. 0x042D

Reg Address	Bit Field	Type	Setting Name	Description
0x042D	1	R/W	HOLD_RAMP-BYP_NOHIST_PLLA	Set by CBPro.

Table 14.136. Register 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	Calculated by CBPro based on value selected.

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 4.6 Holdover Mode to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 14.137. Register 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	Calculated by CBPro based on value selected.

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 4.6 Holdover Mode to calculate the window length from the register value. time = (2^{DELAY})*268nsec

Table 14.138. 0x0431

Reg Address	Bit Field	Type	Setting Name	Description
0x0431	4:0	R/W	HOLD_REF_COUNT_FRC_PLLA	5- bit value

Table 14.139. 0x0432

Reg Address	Bit Field	Type	Setting Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Value calculated by CBPro
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 14.140. Register 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation. 1: To force holdover.

Table 14.141. Register 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual. 1: Automatic, non-revertive. 2: Automatic, revertive. 3: Reserved.
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off). 1: Hitless switching mode (phase buildout turned on).

Table 14.142. Register 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic. 1: To mask LOS from the clock selection logic.

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

Table 14.143. Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: No priority. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4: For priority 4. 5-7: Reserved.
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: No priority. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4: For priority 4. 5-7: Reserved.

Clock input priorities are used only when the clock switch mode is automatic.

Table 14.144. Register 0x0439 DSPLL A Clock Inputs 2 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: No priority. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4: For priority 4. 5-7: Reserved.

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	6:4	R/W	REF_PRIORITY_PLLA	The priority for REF is: 0: No priority. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4: For priority 4. 5-7: Reserved.

Table 14.145. Register 0x043A Hitless Switching mode for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	0: Reserved. 1: Reserved. 2: Enable hitless switching. 3: Reserved.
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	Hitless switching measurement threshold control.

Table 14.146. Register 0x043B and 0x043C Hitless Switching Phase Threshold for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043B	9:0	R/W	HSW_PHMEAS_THR_PLLA	Calculated by CBPro based on value selected.

Table 14.147. Register 0x043D Hitless Switching Length for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Calculated by CBPro based on value selected.

Table 14.148. Register 0x043E Hitless Switching Delay for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Calculated by CBPro based on value selected.

Table 14.149. Register 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid. 1: Valid.
0x043F	2	R	FASTLOCK_STATUS_PLLA	0: Not in Fastlock. 1: Fastlock active.

Table 14.150. Register 0x0488 Hitless Switching Length, Adjust, for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	Values calculated by CBPro.

Table 14.151. Register 0x0489 and 0x048A PFD Enable Delay for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0489	12:0	R/W	PFD_EN_DLAY_PLLA	Calculated by CBPro based on value selected.

Table 14.152. 0x049B

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	Set by CBPro.
0x049B	4	R/W	HOLD_PRESERVE_HIST_PLLA	Set by CBPro.
0x049B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLA	Set by CBPro.
0x049B	6	R/W	HOLDEXIT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEXIT_STD_BO_PLLA	Set by CBPro.

Table 14.153. 0x049D-0x04A2 DSPLL Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x049D	5:0	R/W	BW0_HO_PLLA	DSPLL A Holdover Bandwidth parameters.
0x049E	5:0	R/W	BW1_HO_PLLA	
0x049F	5:0	R/W	BW2_HO_PLLA	
0x04A0	5:0	R/W	BW3_HO_PLLA	
0x04A1	5:0	R/W	BW4_HO_PLLA	
0x04A2	5:0	R/W	BW5_HO_PLLA	

This group of registers determines the DSPLL A bandwidth used when exiting Holdover Mode. Clock Builder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that the individual SOFT_RST_PLLA (0x001C[1]) does not update these bandwidth parameters.

Table 14.154. DSPLLA Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x04A6	3	R/W	Ramp_Switch_EN_PLLA	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover
0x04A6	2:0	R/W	RAMP_STEP_SIZE_PLLA	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made.

14.2.6 Page 5 Registers Si5348

The page 5 registers are associated with DSPLLB, which is the Reference DSPLL and is responsible for supplying the VCO frequency to the other DSPLLs. Because of this, changes to DSPLLB will have an effect onn all the DSPLLs. This warning applies to all the page 5 registers.

Table 14.155. Register 0x0507-0x050D DSPLL B (Reference) Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	5:0	R/W	BW0_PLLB	Calculated by CBPro based on value selected.
0x0509	5:0	R/W	BW1_PLLB	
0x050A	5:0	R/W	BW2_PLLB	
0x050B	5:0	R/W	BW3_PLLB	
0x050C	5:0	R/W	BW4_PLLB	
0x050D	5:0	R/W	BW5_PLLB	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers. The BW_UPDATE bit (register 0x0514[0] must be set to cause the normal and fast bandwidth parameters to be active.

Table 14.156. Register 0x050E-0x0514 DSPLL B (Reference) Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	5:0	R/W	FAST-LOCK_BW0_PLLB	Calculated by CBPro based on value selected.
0x050F	5:0	R/W	FAST-LOCK_BW1_PLLB	
0x0510	5:0	R/W	FAST-LOCK_BW2_PLLB	
0x0511	5:0	R/W	FAST-LOCK_BW3_PLLB	
0x0512	5:0	R/W	FAST-LOCK_BW4_PLLB	
0x0513	5:0	R/W	FAST-LOCK_BW5_PLLB	
0x0514	0	S	BW_UPDATE_PLLB	0: No effect 1: Updates the Normal BW, Fastlock BW, and Exit from Holdover rate.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLB to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Table 14.157. Register 0x0515-0x051B MB Divider Numerator for DSPLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	Values calculated by CBPro.
0x0516	15:8	R/W	M_NUM_PLLB	
0x0517	23:16	R/W	M_NUM_PLLB	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The MB divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.158. Register 0x051C-0x051F MB Divider Denominator for DSPLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	Values calculated by CBPro.
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MB divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.159. Register 0x0520 M Divider Update Bit for PLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.160. Register 0x0540 Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0540	7:0	S	RESERVED	This register is used in the pre-amble/post-amble write sequence for exporting register values.

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Table 14.161. Register 0x0607 Active Input Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0607	7:6	R	IN_PLLC_ACTV	Current input clock. 0: IN0 1: IN1 2: IN2 3: REF

These bits indicate which input clock DSPLL C is currently selected. 0 for IN0; 1 for IN1; etc.

Table 14.162. Register 0x0608-0x060D DSPLL C Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0608	5:0	R/W	BW0_PLLC	Calculated by CBPro based on value selected.
0x0609	5:0	R/W	BW1_PLLC	
0x060A	5:0	R/W	BW2_PLLC	
0x060B	5:0	R/W	BW3_PLLC	
0x060C	5:0	R/W	BW4_PLLC	
0x060D	5:0	R/W	BW5_PLLC	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 14.163. Register 0x060E-0x0614 DSPLL C Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x060E	5:0	R/W	FAST-LOCK_BW0_PLLC	Calculated by CBPro based on value selected.
0x060F	5:0	R/W	FAST-LOCK_BW1_PLLC	
0x0610	5:0	R/W	FAST-LOCK_BW2_PLLC	
0x0611	5:0	R/W	FAST-LOCK_BW3_PLLC	
0x0612	5:0	R/W	FAST-LOCK_BW4_PLLC	
0x0613	5:0	R/W	FAST-LOCK_BW5_PLLC	
0x0614	0	S	BW_UPDATE_PLLC	0: No effect. 1: Updates the Normal BW, Fastlock BW, and Exit from Holdover rate.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLC to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Table 14.164. Register 0x0615-0x061B MC Divider Numerator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	Values calculated by CBPro.
0x0616	15:8	R/W	M_NUM_PLLC	
0x0617	23:16	R/W	M_NUM_PLLC	
0x0618	31:24	R/W	M_NUM_PLLC	
0x0619	39:32	R/W	M_NUM_PLLC	
0x061A	47:40	R/W	M_NUM_PLLC	
0x061B	55:48	R/W	M_NUM_PLLC	

The MC divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.165. Register 0x061C-0x061F MC Divider Denominator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	Values calculated by CBPro.
0x061D	15:8	R/W	M_DEN_PLLC	
0x061E	23:16	R/W	M_DEN_PLLC	
0x061F	31:24	R/W	M_DEN_PLLC	

The loop MC divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.166. Register 0x0620 M Divider Update Bit for PLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0620	0	S	M_UPDATE_PLLC	Must write a 1 to this bit to cause PLL C M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.167. Register 0x0621 M Divider Fractional Control Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0621	3:0	R/W	M_FRAC_MODE_PLLC	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0621	4	R/W	M_FRAC_EN_PLLC	M divider fractional control and enable. When DSPLL C is in DCO mode, this register should be written to 0x31.

Table 14.168. Register 0x0622 DSPLL C FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	0	R/W	M_FSTEP_MSK_PLLC	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0622	1	R/W	M_FSTEPW_DEN_PLLC	0: Modify numerator 1: Modify denominator

Table 14.169. Register 0x0623-0x0629 DSPLLC MC Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	Values calculated by CBPro.
0x0624	15:8	R/W	M_FSTEPW_PLLC	
0x0625	23:16	R/W	M_FSTEPW_PLLC	
0x0626	31:24	R/W	M_FSTEPW_PLLC	
0x0627	39:32	R/W	M_FSTEPW_PLLC	
0x0628	47:40	R/W	M_FSTEPW_PLLC	
0x0629	55:48	R/W	M_FSTEPW_PLLC	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL C is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0615–0x061F.

Table 14.170. Register 0x062A DSPLL C Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	0: For IN0 1: For IN1 2: For IN2 3-7: Reserved

This is the input clock selection for manual register based clock selection.

Table 14.171. Register 0x062B DSPLL C Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Applies when FASTLOCK_MAN_PLLC=0. 0: Disables auto fast lock 1: Enables auto fast lock when PLLA is out of lock
0x062B	1	R/W	FASTLOCK_MAN_PLLC	0: For normal operation 1: For force fast lock

Table 14.172. Register 0x062C DSPLL C Holdover Control

Reg Address	Bit Field	Type	Setting Name	Descrption
0x062C	0	R/W	HOLD_EN_PLLC	0: Holdover Disabled 1: Holdover Enabled. Standard setting.
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	0: Use Ramp Rate when exiting from Holdover 1: Standard PLL configuration when exiting from Holdover
0x062C	4	R/W	HOLD_EXITBW_SEL1_PLLC	This bit with HOLDEXIT_BW_SEL0_PLLB are set by CBPro to allow the bandwidth when exiting holdover to be set independent of the PLL bandwidth during other times of operation. CBPro sets this bit.
0x062C	7:5	R/W	RAMP_STEP_INTERVAL_PLLC	The ramp rate is selected when using CBPro.

Table 14.173. 0x062D

Reg Address	Bit Field	Type	Setting Name	Description
0x062D	1	R/W	HOLD_RAMPBYP_NOHIST_PLLC	Set by CBPro.

Table 14.174. Register 0x062E DSPLL C Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	Calculated by CBPro based on value selected.

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 4.6 Holdover Mode to calculate the window length from the register value.

time = $((2^{LEN}) – 1)$*268nsec

Table 14.175. Register 0x062F DSPLLC Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	Calculated by CBPro based on value selected.

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushed back into the past. The amount the average window is delayed is the holdover history delay. See 4.6 Holdover Modeto calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 14.176. 0x0631

Reg Address	Bit Field	Type	Setting Name	Description
0x0631	4:0	R/W	HOLD_REF_COUNT_FRC_PLLC	Set by CBPro.

Table 14.177. 0x0632-0x0634

Reg Address	Bit Field	Type	Setting Name	Description
0x0632	7:0	R/W	HOLD_15M_CYC_COUNT_PLLC	Set by CBPro.
0x0633	15:8	R/W	HOLD_15M_CYC_COUNT_PLLC	
0x0634	23:16	R/W	HOLD_15M_CYC_COUNT_PLLC	

Table 14.178. Register 0x0635 DSPLL C Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	0: For normal operation 1: To force holdover

Table 14.179. Register 0x0636 DSPLLC Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 14.180. Register 0x0637 DSPLLC Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0637[0], OOF alarm 0x0637[4]

IN1 Input 1 applies to LOS alarm 0x0637[1], OOF alarm 0x0637[5]

IN0 Input 2 applies to LOS alarm 0x0637[2], OOF alarm 0x0637[6]

Table 14.181. Register 0x0638 DSPLL C Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved

Table 14.182. Register 0x0639 DSPLL C Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	6:4	R/W	REF_PRIORI-TY_PLLC	The priority for clock REF is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Clock input priorities are used only when the clock switch mode is automatic.

Table 14.183. 0x063A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x063A	1:0	R/W	HSW_MODE_PLLC	2:Default setting, do not modify 0,1,3: Reserved
0x063A	3:2	R/W	HSW_PHMEAS_CTRL_PLLC	0: Default setting, do not modify 1,2,3: Reserved

Table 14.184. 0x063B-0x063C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x063B	7:0	R/W	HSW_PHMEAS_THR_PLLC	10-bit value. Set by CBPro.
0x063C	9:8	R/W	HSW_PHMEAS_THR_PLLC	

Table 14.185. Register 0x063D Hitless Switching Length for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x063D	4:0	R/W	HSW_COARSE_PM_LEN_PLLC	Calculated by CBPro based on value selected.

Table 14.186. Register 0x063E Hitless Switching Delay for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x063E	4:0	R/W	HSW_COARSE_PM_DLY_PLLC	Value caclulated in CBPro

Table 14.187. Register 0x063F DSPLL C Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x063F	2	R	FASTLOCK_STATUS_PLLC	1: Indicates the loop is in fastlock.

Table 14.188. Register 0x0688 Hitless Switching Length, Adjust, for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0688	3:0	R/W	HSW_FINE_PM_LEN_PLLC	Values calculated by CBPro.

Table 14.189. Register 0x0689 and 0x068A PFD Enable Delay for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0689	7:0	R/W	PFD_EN_DLY_PLLC	Calculated by CBPro based on value selected.
0x068A	3:0	R/W	PFD_EN_DLY_PLLC	

Table 14.190. Registers 0x069B, Exit from Holdover BW Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x069B	1	R/W	INIT_LP_CLOSE_HO_PLLC	Set by CBPro.
0x069B	4	R/W	HOLD_PRESERVE_HIST	Set by CBPro.
0x069B	5	R/W	HOLD_FRZ_WITH_INT_ONLY	Set by CBPro.
0x069B	6	R/W	HOLDEXIT_BW_EN_PLLC	Set by CBPro. See HOLDEXIT_BW_SEL1_PLLA
0x069B	7	R/W	HOLDEXIT_STD_BO_PLLC	Set by CBPro.

Table 14.191. Registers 0x069D- 0x006A2, Exit from Holdover BW Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x069D	5:0	R/W	HOLDEXIT_BW0_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x069E	5:0	R/W	HOLDEXIT_BW1_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x069F	5:0	R/W	HOLDEXIT_BW2_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x06A0	5:0	R/W	HOLDEXIT_BW3_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x06A1	5:0	R/W	HOLDEXIT_BW4_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x06A2	5:0	R/W	HOLDEXIT_BW5_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Table 14.192. DSPLLC Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x06A6	3	R/W	RAMP_SWITCH_EN_PLLC	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover
0x06A6	2:0	R/W	RAMP_STEP_SIZE_PLLC	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made.

14.2.8 Page 7 Registers Si5348

Note that register addresses for Page 7 DSPLL D Registers 0x0709-0x074D are incremented relative to similar DSPLL A and C addresses on Pages 4 and 6. For example, Register 0x0709 has the equivalent function to Registers 0x0408/0x0608.

Table 14.193. Register 0x0708 Active Input Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0708	2:0	R	IN_PLLD_ACTV	Current input clock 0: IN0 1: IN1 2: IN2 3: REF 4: IN3 5: IN4

These bits indicate which input clock DSPLL D is currently selected. 0 for IN0; 1 for IN1, 2 for IN2, 3 Referene, 4 for CMOS IN3, and 5 for CMOS IN4.

Table 14.194. Register 0x0709-0x070E DSPLL D Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0709	5:0	R/W	BW0_PLLD	Calculated by CBPro based on value selected.
0x070A	5:0	R/W	BW1_PLLD	
0x070B	5:0	R/W	BW2_PLLD	
0x070C	5:0	R/W	BW3_PLLD	
0x070D	5:0	R/W	BW4_PLLD	
0x070E	5:0	R/W	BW5_PLLD	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 14.195. Register 0x070F-0x0715 DSPLL D Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x070F	5:0	R/W	FAST-LOCK_BW0_PLLD	Calculated by CBPro based on value selected.
0x0710	5:0	R/W	FAST-LOCK_BW_1PLLD	
0x0711	5:0	R/W	FAST-LOCK_BW2_PLLD	
0x0712	5:0	R/W	FAST-LOCK_BW3_PLLD	
0x0713	5:0	R/W	FAST-LOCK_BW_4PLLD	
0x0714	5:0	R/W	FAST-LOCK_BW5_PLLD	

Reg Address	Bit Field	Type	Setting Name	Description
0x0715	0	S	BW_UPDATE_PLLD	0: No effect 1: Update both the Normal and Fastlock BWs for PLL D.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers.

Table 14.196. Register 0x0716-0x071C MD Divider Numerator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	Values calculated by CBPro.
0x0717	15:8	R/W	M_NUM_PLLD	
0x0718	23:16	R/W	M_NUM_PLLD	
0x0719	31:24	R/W	M_NUM_PLLD	
0x071A	39:32	R/W	M_NUM_PLLD	
0x071B	47:40	R/W	M_NUM_PLLD	
0x071C	55:48	R/W	M_NUM_PLLD	

The MD divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.197. Register 0x071D-0x0720 MD Divider Denominator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	Values calculated by CBPro.
0x071E	15:8	R/W	M_DEN_PLLD	
0x071F	23:16	R/W	M_DEN_PLLD	
0x0720	31:24	R/W	M_DEN_PLLD	

The loop MD divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.198. Register 0x0721 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0721	0	S	M_UPDATE_PLLD	Must write a 1 to this bit to cause PLL D M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.199. Register 0x0722 M Divider Fractional Control and Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	3:0	R/W	M_FRAC_MODE_PLLD	M feedback divider fractional mode. Must be set to 0xB for proper operation.

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	4	R/W	M_FRAC_EN_PLLD	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.

Table 14.200. Register 0x0723 DSPLL D FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0723	0	R/W	M_FSTEP_MSK_PLLD	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates
0x0723	1	R/W	M_FSTEPW_DEN_PLLD	0: Modify numerator 1: Modify denominator

Table 14.201. Register 0x0724-0x072A DSPLLD MD Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	Values calculated by CBPro.
0x0725	15:8	R/W	M_FSTEPW_PLLD	
0x0726	23:16	R/W	M_FSTEPW_PLLD	
0x0727	31:24	R/W	M_FSTEPW_PLLD	
0x0728	39:32	R/W	M_FSTEPW_PLLD	
0x0729	47:40	R/W	M_FSTEPW_PLLD	
0x072A	55:48	R/W	M_FSTEPW_PLLD	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL D is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0716-0x0720.

Table 14.202. Register 0x072B DSPLL D Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	0: For IN0 1: For IN1 2: For IN2 3: Reference 4: For IN3 5: For IN4 6-7: Reserved

This is the input clock selection for manual register based clock selection. IN3 and IN4 are selected in manual mode only..

Table 14.203. Register 0x072C DSPLL D Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Applies when FASTLOCK_MAN_PLLD=0. 0: Disables auto fast lock 1: Enables auto fast lock when PLLA is out of lock
0x072C	1	R/W	FASTLOCK_MAN_PLLD	0: For normal operation 1: For force fast lock

Table 14.204. Register 0x072 DSPLL D Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	0	R/W	HOLD_EN_PLLD	0: Holdover Disabled 1: Holdover Enabled. Standard setting.
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	0: Use Ramp Rate when exiting from Holdover 1: Standard PLL configuration when exiting from Holdover
0x072D	4	R/W	HOLD_EXITBW_SEL1_PLLD	This bit with HOLDEXITBW_SEL0_PLLA are set by CBPro to allow the bandwidth when exiting holdover to be set independent of the PLL bandwidth during other times of operation. CBPro sets this bit.
0x072D	7:5	R/W	HOLD_RAMP_RATE_PLLD	The ramp rate is selected when using CBPro.

Table 14.205. 0x072E

Reg Address	Bit Field	Type	Setting Name	Description
0x072E	1	R/W	HOLD_RAMPBYP_NOHIST_PLLD	Set by CBPro.

Table 14.206. Register 0x072F DSPLL D Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	Calculated by CBPro based on value selected.

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 4.6 Holdover Mode to calculate the window length from the register value. time = $((2^{LEN}) - 1)$*268nsec

Table 14.207. Register 0x0730 DSPLLD Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0730	4:0	R/W	HOLD_HIST_DELAY_PLLD	Calculated by CBPro based on value selected.

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 4.6 Holdover Mode to calculate the ignore delay time from the register value. time = (2^{DELAY})*268nsec

Table 14.208. 0x0732

Reg Address	Bit Field	Type	Setting Name	Description
0x0732	4:0	R/W	HOLD_REF_COUNT_FRC_PLLD	5- bit value

Table 14.209. 0x0733-0x0735

Reg Address	Bit Field	Type	Setting Name	Description
0x0733	7:0	R/W	HOLD_15M_CYC_COUNT_PLLD	Set by CBPro.
0x0734	15:8	R/W	HOLD_15M_CYC_COUNT_PLLD	
0x0735	23:16	R/W	HOLD_15M_CYC_COUNT_PLLD	

Table 14.210. Register 0x0736 DSPLL D Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	0: For normal operation 1: To force holdover

Table 14.211. Register 0x0737 DSPLLD Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

The only way to use IN3 and IN4 is with manual register based clock selection.

Table 14.212. Register 0x0738 DSPLLD Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applied to LOS alarm 0x0738[0], OOF alarm 0x0738[4]

IN1 Input 1 applied to LOS alarm 0x0738[1], OOF alarm 0x0738[5]

IN2 Input 2 applies to LOS alarm 0x0738[2], OOF alarm 0x0738[6]

Table 14.213. Register 0x0739 DSPLL D Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	The priority for clock input 0 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved
0x0739	6:4	R/W	IN1_PRIORITY_PLLD	The priority for clock input 1 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved

Clock input priorities are used only when the clock switch mode is automatic.

Table 14.214. Register 0x073A DSPLL D Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	2:0	R/W	IN2_PRIORITY_PLLD	The priority for clock input 2 is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved
0x073A	6:4	R/W	REF_PRIORITY_PLLD	The priority for REF is: 0: No priority 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved

Table 14.215. 0x073B Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x073B	1:0	R/W	HSW_MODE_PLLD	2:Default setting, do not modify 0,1,3: Reserved
0x073B	3:2	R/W	HSW_PHMEAS_CTRL_PLLD	0: Default setting, do not modify 1,2,3: Reserved

Table 14.216. 0x073C-0x073D Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x073C	7:0	R/W	HSW_PHMEAS_THR_PLLD	10-bit value. Set by CBPro.
0x073D	9:8	R/W	HSW_PHMEAS_THR_PLLD	

Table 14.217. 0x073E

Reg Address	Bit Field	Type	Setting Name	Description
0x073E	4:0	R/W	HSW_COARSE_PM_LEN_PLLD	Set by CBPro.

Table 14.218. 0x073F

Reg Address	Bit Field	Type	Setting Name	Description
0x073F	4:0	R/W	HSW_COARSE_PM_DLY_PLLD	Set by CBPro.

Table 14.219. Register 0x0740 DSPLL D Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	1	R	HOLD_HIST_VALID_PLLD	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x0740	2	R	FASTLOCK_STATUS_PLLD	0: Not in Fastlock 1: Fastlock active

Table 14.220. Register 0x0788 Hitless Switching Length, Adjust, for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0788	3:0	R/W	HSW_FINE_PM_LEN_PLLD	Values calculated by CBPro.

Table 14.221. Register 0x0789 and 0x078A PFD Enable Delay for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0789	7:0	R/W	PFD_EN_DLY_PLLD	Value caclulated in CBPro.
0x078A	3:0	R/W	PFD_EN_DLY_PLLD	

Table 14.222. 0x079B

Reg Address	Bit Field	Type	Setting Name	Description
0x079B	1	R/W	INIT_LP_CLOSE_HO_PLLD	Set by CBPro.
0x079B	4	R/W	HOLD_PRESERVE_HIST_PLLD	Set by CBPro.
0x079B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLD	Set by CBPro.
0x079B	6	R/W	HOLDEXIT_BW_SEL0_PLLD	Set by CBPro.
0x079B	7	R/W	HOLDEXIT_STD_BO_PLLD	Set by CBPro.

Table 14.223. Registers 0x079D- 0x007A2, Exit from Holdover BW Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x079D	5:0	R/W	HOLDEXIT_BW0_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x079E	5:0	R/W	HOLDEXIT_BW1_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x079F	5:0	R/W	HOLDEXIT_BW2_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x07A0	5:0	R/W	HOLDEXIT_BW3_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x07A1	5:0	R/W	HOLDEXIT_BW4_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x07A2	5:0	R/W	HOLDEXIT_BW5_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Table 14.224. DSPLLD Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x07A6	3	R/W	RAMP_SWITCH_EN_PLLD	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover
0x07A6	2:0	R/W	RAMP_STEP_SIZE_PLLD	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made.

Table 14.225. Register 0x07AA PLLD Clock Input Control

Reg Address	Bit Field	Type	Setting Name	Description
0x07AA	0	R/W	CONFIG3_CMOS_PLLD	0:Normal Selection 1: Replace input selection with CONFIG2_CMOS_PLLD
0x07AA	1	R/W	CONFIG2_CMOS_PLLD	0: IN3 1: IN4
0x07AA	2	R/W	CONFIG1_CMOS_PLLD	0: standard IN0, IN1, IN3 1: Override with value selected in CONFIG2_CMOS_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x07AA	5:4	R/W	CONFIG0_CMOS_PLLD	00: Replace IN0 with IN3/IN4 not selected by CONFIG2_CMOS_PLLD 01: Replace IN1 with IN3/IN4 not selected by CONFIG2_CMOS_PLLD 10:Replace IN2 with IN3/IN4 not selected by ONFIG2_CMOS_PLLD 11: Reserved

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Table 14.226. Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit optimizes the Vil, Vih, Vol, and Voh thresholds to match the VDDS voltage. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I2C or SPI host is operating at 3.3 V and the Si5348 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit high. This will ensure that both the host and the serial interfaces are operating at the optimum voltage thresholds.

Control input pins (I2C_SEL, A1/SDO, SDA/SDIO, SCLK, RSTb, OE0b, OE1b, OE2b, FINC) are controlled by the IO_VDD_SEL and also status output pins (LOL_Cb, LOLDb, INTRb, LOS1b, LOS2b, SDA/SDIO, A1/SDO). It is more than just the communication I2C/SPI interface that is affected by IO_VDD_SEL. The datasheet specifies the voltage limits for these pins based on the VDDIO voltage.

Table 14.227. Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for Ref, IN2, IN1 and IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN2, IN1 and IN0.

When a clock is disabled, it is powered down.

- Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]
- Input 1 corresponds to IN_EN 0x0949[1], IN_PULSED_CMOS_EN 0x0949[5]
- Input 2 corresponds to IN_EN 0x0949[2], IN_PULSED_CMOS_EN 0x0949[6]
- Input 3 (Reference) corresponds to IN_EN 0x0949[3]

Table 14.228. Register 0x094A

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 14.229. Register 0x094E

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro

Table 14.230. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTEGER	0: Integer MXAXB 1: Fractional MXAXB

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Table 14.231. Register 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Setting Name	Description
0x0A03	3:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (D C B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.232. Register 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Setting Name	Description
0x0A04	3:0	R/W	N_PIBYP	Bypass the fractional part of the internal divider for PLLs (D C B A). Set to a 1 when the value is integer, as this may give slightly lower phase noise. May be set to 0 when the value is either fractional or integer. Changes made to 0x0A04 requires a SOFT_RST or a SYNC. N_PIBYP should be cleared for all FOTF and DCO applications.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.233. Register 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Setting Name	Description
0x0A05	3:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (D C B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

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Table 14.234. Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 4.2 Changing Registers while Device in Operation for more information.

Table 14.235. Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 4.2 Changing Registers while Device in Operation for more information.

Table 14.236. 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	6	R/W	FRACN_CLK_DIS_PLLC	Clock disable for the fractional divide of the M divider in PLLC. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Reg Address	Bit Field	Type	Name	Description
0x0B44	7	R/W	FRACN_CLK_DIS_PLLD	Clock disable for the fractional divide of the M divider in PLLD. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

When a DSPLL is in DCO mode, its corresponding clock disable bit should be cleared.

If DSPLLA is in DCO mode, 0x0B44[4] should be zero.

If DSPLLC is in DCO mode, 0x0B44[6] should be zero.

If DSPLLD is in DCO mode, 0x0B44[7] should be zero.

Table 14.237. 0x0B45 LOL Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	1: Clock disabled.
0x0B45	1	R/W	CLK_DIS_PLLB	1: Clock disabled.
0x0B45	2	R/W	CLK_DIS_PLLC	1: Clock disabled.
0x0B45	3	R/W	CLK_DIS_PLLD	1: Clock disabled.

Table 14.238. Register 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS for (REF, IN2, IN1, IN0). Must be set to 0 to enable the LOS function of the respective inputs.
0x0B46	5:4	R/W	LOS_CMOS_CLK_DIS_PLLD	Disables LOS for the CMOS clocks IN3 and IN4. Must be set to 0 to enable the LOS function of the respective inputs.

Table 14.239. Register 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set to 0 for normal operation. Digital OOF Bits 3:0 are for IN3,2,1,0, Bit 4 is for OOF for the XAXB input.

Table 14.240. Register 0x0B48

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set to 0 for normal operation. Digital OOF divider clock user disable. Bits 3:0 are for IN3,2,1,0, Bit 4 is for OOF for the XAXB input.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed whhen changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.241. Register 0x0B49 Calibration Bits

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.242. Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	3:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (D C B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.243. Register 0x0B57 VCO Reset Calcode

Reg Address	Bit Field	Type	Setting Name	Description
0x0B57	7:0	R/W	VCO_RESET_CAL-CODE	Value caclulated in CBPro
0x0B58	3:0	R/W	VCO_RESET_CAL-CODE	

15. Custom Differential Amplitude Controls

In some applications, it may be desirable to drive larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings generated by ClockBuilder Pro. For example, "CML" format is sometimes desired for an application, but CML is not a defined standard, and hence, the input amplitude of CML signals may differ between receivers. In these cases, the following information describes how to implement non-standard differential amplitudes.

The differential output driver has two basic modes of operation as well as variable output amplitude capability. The Normal mode has an internal impedance of ~100 ohms differential, while the Low Power mode has an internal impedance of >500 ohms differential. In both cases, when properly terminated with 100 ohms differential externally, the amplitudes listed in the table below result.

Table 15.1. Differential Output Amplitude Typical Values

OUTx_AMPL	Normal Mode OUTx_FORMAT = 1 (Vpp-SE mV - Typical)	Low Power Mode OUTx_FORMAT = 2 (Vpp SE mV - Typical)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[1]
7	920	1600[1]

Note:
1. In low power mode with VDDOx = 1.8 V, OUTx_AMPL may not be set to 6 or 7.
2. These amplitudes are based upon 100 Ω differential termination

For applications using a custom differential output amplitude the common mode voltage should be selected as shown in the table below. These settings, along iwth the settings given in Table 21, have been verified to give good signal integrity. Some extreme combinations of amplitude and common mode may have impaired signal integrity.

Also, in cases where the receiver is dc-biased either internally or through an external network, the outputs of this device must be ac-coupled. Output driver performance is not guaranteed when dc-coupled to a biased-input receiver.

Table 15.2. Differential Output Common Mode Voltage Settings

VDDOx (V)	Differential Format	OUTx_FORMAT (dec)	Common Mode Voltage (V)	OUTx_CM (dec)
3.3	Normal	1	2.05	11
3.3	Low Power	2	1.65	7
2.5	Normal	1	1.35	12
2.5	Low Power	2	1.15	10
1.8	Normal	1	0.80	13
1.8	Low Power	2	0.80	13

See also (xref) for additional information on the OUTx_FORMAT, OUTx_AMPL, and OUTx_CM controls.

16. Accessing Design and Support Collateral

The Si5348 is currently available to restricted customers only. To access the support documentation, contact Skyworks Support.

17. Revision History

Revision 1.4

October, 2018

- Updated input, reference, and output termination diagrams.

Revision 1.3

February, 2018

- Updated register descriptions to include all reported registers from CBPro.
- Updated block diagrams to include the reference input selectable to DSPLL A, C, and D.
- Added 5.3.6 Rise Time Considerations.

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