

Si5346-D EVALUATION BOARD USER'S GUIDE

Description

The Si5346-D-EVB is used for evaluating the Si5346 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5346-D-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

EVB Features

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows standalone or holdover mode of operation on the Si5346.
- ClockBuilder[®] Pro (CBPro) GUI programmable V_{DD} supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable V_{DDO} supplies allow each of the 4 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI allows control and measurement of voltage, current, and power of V_{DD} and all 4 V_{DDO} supplies.
- Status LEDs for power supplies and control/status signals of Si5346.
- SMA connectors for input clocks, output clocks, and optional external timing reference clock.

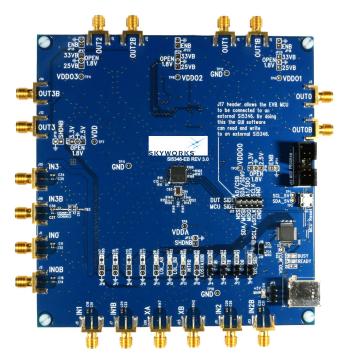


Figure 1. Si5346-D Evaluation Board

1. Si5346-D-EB Functional Block Diagram

Below is a functional block diagram of the Si5346-D-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See section "3. Quick Start" or section "9. Installing ClockBuilder Pro Desktop Software" for more information.

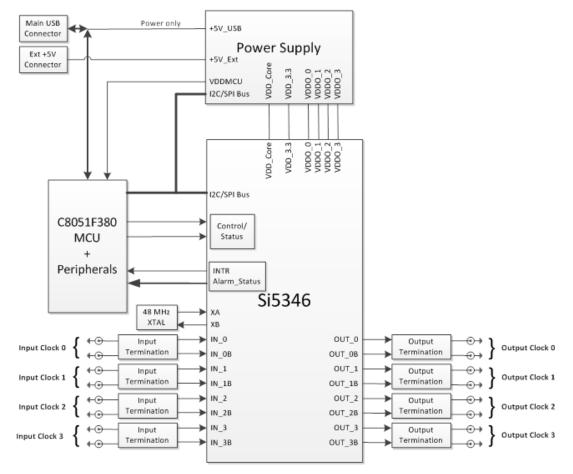


Figure 2. Si5346-D-EB Functional Block Diagram

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2. Si5346-D-EVB Support Documentation and ClockBuilder Pro Software

All Si5346-D-EVB schematics, BOMs, User's Guides, and software can be found online at the following link: www.skyworksinc.com/support-ia

3. Quick Start

- 1. Install ClockBuilder Pro desktop software from www.skyworksinc.com/en/application-pages/clockbuilder-pro-software.
- 2. Connect a USB cable from Si5346-D-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 1.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5346-D-EB.
- 6. For the Si5346 data sheet, go to www.skyworksinc.com/en/Products/Timing.

Si5346-D-EVB

4. Jumper Defaults

Location	Туре	I = Installed 0 = Open	Location	Туре	l = Installed 0 = Open
JP1	2 pin	I			
JP2	2 pin	I			
JP3	2 pin	0			
JP4	2 pin	Ι			
JP5	3 pin	1 to 2 (USB)			
			J17	5 x 2 Hdr	All 5 installed
Note: Refer to	o the Si534	16-D-EB schematics	for the functionality	associated wit	th each jumper.

Table 1. Si5346-D-EB Jumper Defaults

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D5	LOS_XAXBB	Blue	XA/XB Loss of Signal indicator
D6	INTRB	Blue	MCU INTR (Interrupt) active
D7	LOL_BB	Blue	DSPLL A Loss of Lock indicator
D8	LOL_AB	Blue	DSPLL B Loss of Lock indicator
D11	+5V MAIN	Green	Main USB +5V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

Table 2. Si5346-D- EB Status LEDs

D5, D6, D7, and D8 are status LEDs indicating the device alarms currently asserted. D11 is illuminated when USB +5 V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.

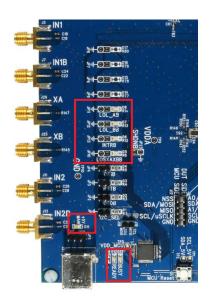
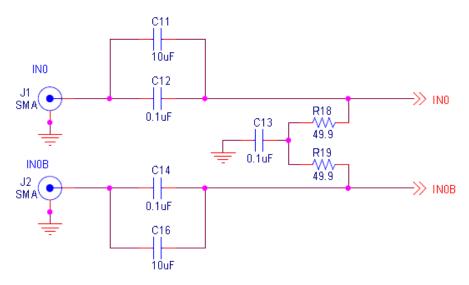
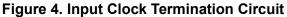


Figure 3. Status LEDs

6. Clock Input Circuits (INx/INxB)

The Si5346-D-EB has eight SMA connectors (IN0/IN0B–IN3/IN3B) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5346 data sheet. Typically a 0.1 μ F dc block is sufficient, however, 10 μ F may be needed for lower input frequencies. Note that the EVB is populated with both dc block capacitor values.





7. Clock Output Circuits (OUTx/OUTxB)

Each of the eight output drivers (four differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5346-D-EB provides an L-network at OUT0/OUT0B output pins for optional output termination resistors. Note that components with schematic "**NI**" designation are not normally populated.

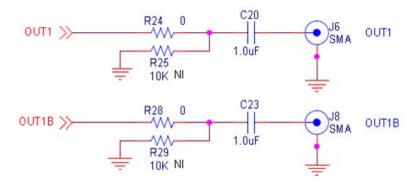


Figure 5. Output Clock Termination Circuit

8. External Reference Clock Input Circuit (XA/XB)

The Si5346-D-EB supports either XTAL or external reference clock on XA/XB. By default, the XTAL is populated. If a reference clock is required for testing, remove Y1 and place C93/C94. A low-jitter reference clock can then be applied to J25/J26. Note that XA/XB is the jitter reference for the device. Jitter performance at the output of the Si5346 will depend on the jitter performance of the reference clock at XA/XB.

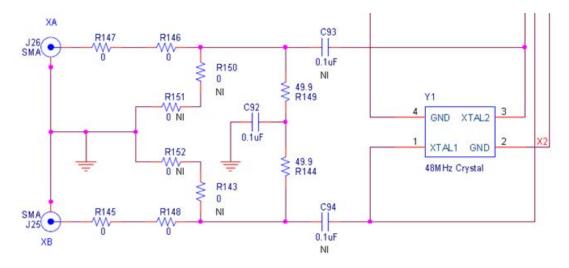


Figure 6. External Reference Clock Termination Circuit

9. Installing ClockBuilder Pro Desktop Software

To install the CBOPro software on any Windows 7 (or above) PC:

Go to www.skyworksinc.com/en/application-pages/clockbuilder-pro-software

and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Please follow the instructions as indicated.

10. Using the Si5346-D-EVB

10.1. Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown below.

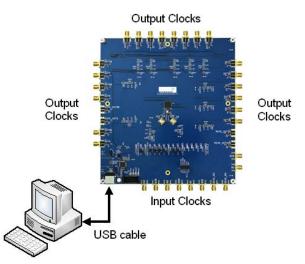


Figure 7. EVB Connection Diagram

10.2. Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is **not** needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5346-D-EB schematic for details.

10.3. Overview of ClockBuilder Pro Applications

The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilder Pro installer will install **two** main applications:

CB ClockBuilder Pro Wizard - Skyworks	– 🗆 X
O ClockBuilder Pro Wizard Q We Make Timing Simple	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions Knowledge Base
🖶 <u>Open Project</u>	Custom Part Number Lookup
<u>Convert Existing Project/NVM File</u>	Applications Documentation 10/40/100G Line Card Whitepaper
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance
SI5346A Rev D EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements
	ClockBuilder Pro Documentation
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes
o,	Version 4.1 Built on 9/22/2021

Figure 8. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

CB Si	5346A Rev D	EVB - Cloo	kBuilder Pro)						
File	Help									
Info	DUT SPI	DUT Set	ings Editor	DUT Reg	ister Editor	Regulators	All Voltages	GPIO	Status Registers	
					Voltage	Curren	it Powe	r		
	VD	D 1.80V		On	V)	Δ	w	Read	
	VDD	A 3.30V		On	V)	Δ	w	Read	
	VDDO	0 1.80		Off	V)	Δ	w	Read	
	VDDO	1.80		Off	V)	Δ	w	Read	
	VDDO	2 1.80V		Off	V)	۹	w	Read	
	VDDO	3 1.80V		Off	v)	а	w	Read	
A	ll Output	Selec	t Voltage		Total	,	Α	w	Read All	
	Supplies	Powe	r On P	ower Off	Co	mpare Desig	n Estimates to	o Measu	rements	

Figure 9. Application #2: EVB GUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5346)
- Control the EVB's regulators
- Monitor voltage, current, power on the EVB

10.4. Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5346-D-EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Skyworks-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

10.5. Workflow Scenario #1: Testing a Skyworks-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows. Once the PC and EVB are connected, launch **ClockBuilder Pro** by clicking on this icon on your PC's desktop.



Figure 10. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

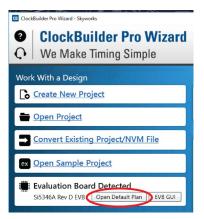


Figure 11. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.



Select "Yes" to write the default plan to the Si5346 device mounted on your EVB. This ensures the device is completely reconfigured per the Skyworks default plan for the DUT type mounted on the EVB.

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Writing Si5346 Design to EVB	
Address 0x0429	

Figure 13. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.

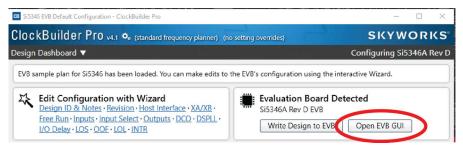


Figure 14. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device's default CBPro project file created by Skyworks, as shown below.

			_										
CB Si5346A Rev D	D EVE	3 - ClockBu	uilder Pro										
ile Help													
Info DUT SPI	D	UT Setting	s Editor	DUT Reg	ister Editor	Regulators	All Volta	iges	GPIO	Status Registe	ers		
					Voltage	Curren	t P	ower					
V	סכ	1.80V		On 🛛	1.796 V	113 r	nA	203 r	nW [Read			
VDI	DA	3.30V		On	3.282 V	120 r	nA	394 n	nW [Read			
VDD	00	1.80V		Off	0.005 V	0 r	nA	0 n	nW [Read			
VDD	01	1.80V		On 📃	1.789 V	0 r	nA	0 n	nW [Read			
VDD	02	1.80V		On	1.784 V	0 r	nA	0 n	nW [Read			
VDD	03	1.80V		On	1.800 V	0 r	nA	0 n	nW [Read			
All Output	Г	Select Vo	oltage	V	Total	233 1	mA 0.	597 \	N [Read All			
Supplies	1	Power C	n Po	ower Off	Co	mpare Desig	n Estimat	tes to	Measu	rements			

Figure 15. EVB GUI Window

10.5.1. Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Skyworks-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":

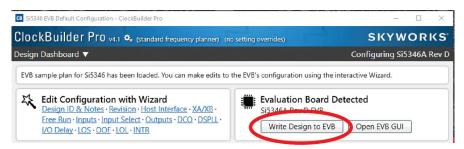


Figure 16. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

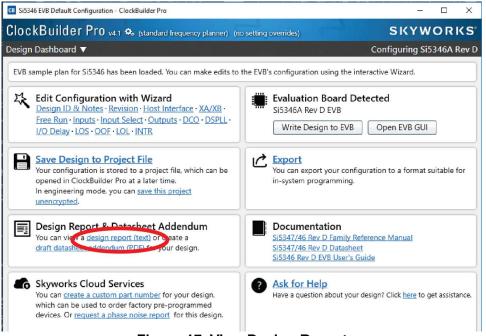


Figure 17. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

Si5346 Design Report		-)
esign Report			
* Engineering Mo	de Design Report **		
verview			
art:	Si5346A Rev D		
esign ID: reated By:	5346EVB3 ClockBuilder Pro v4.1 [2021-09-22]		
imestamp:	2021-11-12 12:16:41 GMT-05:00		
1.			
esign Rule Check			
rrors:			
No errors			
arnings: No warnings			
evice Grade			
	equency: 672.1640625 MHz		
requency Synthes requency Plan Gra	is Mode: Fractional ade: A		
inimum Base OPN:			
evice Outpu	t Clock		
	ency Range Typical Jitter		
	z to 720 MHz < 150 fs z to 350 MHz "		
	alculated frequency plan, a Si5346A grade device is design. See the datasheet Ordering Guide for more		
esign			
ost Interface:	Ive VPD (Come)		
I/O Power Supp SPI Mode: 4-Wi			
	nge: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins)		
A/XB:			
48 MHz (XTAL -	Crystal)		
nputs:			
ING 25 MHz			
Standard			
DSPLL A,	B		
IN1: 25 MHz			
Standard			
DSPLL A,	8		
IN2: 10 MHz			
Standard			
DSPLL A, IN3: 10 MHz			
Standard			
DSPLL A,			
utputs:			
0070 161.1328	125 MHz		

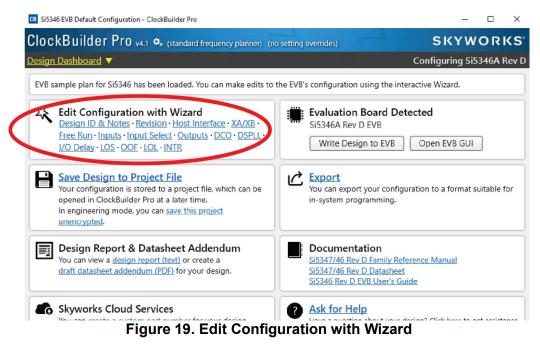
Figure 18. Design Report Window

10.5.2. Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

10.6. Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard:



You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

look Ruild	or Pro	SIZV	NOR	1Z
	er Pro v4.1 🍫 (standard frequency planner) (no setting overrides)			
ep 1 of 15 - De	sign ID & Notes ▼	Configuring:	5i5346A	Re
D esign ID The device has 8 r	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/rev	sion identifier.		
Design ID:	5346EVB3 (optional; max 8 characters)			
	The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_ID	7.		
Padding Mode:	NULL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padde character).	Configuring S15346A Rev D gn/configuration/revision identifier, 0 through DESIGN_ID7, GN_IDx will be padded with 0x00 bytes (aka NULL		
	 Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padde character). 	d with 0x20 bytes	(space	
	ord wrapped in reports, you can use newlines to start a new paragraph.	otasine otasine	et suberio	

Figure 20. Design Wizard

Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

Figure 21. Writing Design Status

10.7. Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

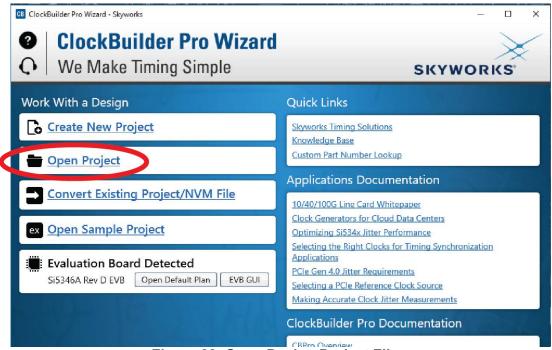


Figure 22. Open Design Project File

Si5346-D-EVB

Image: market with the second sec	CB Open CBPro Projec	ct File				×
Arme Date modified Type Size Desktop Documents Downloads Pictures Si3344 Si3343 Si3343 Si3343 This PC Network	$\leftrightarrow \rightarrow \checkmark \uparrow$	« Jui_Tharwal > User_Guide_Images_Rebranding	> Si5346 🗸 🤇	Search Si5346		٩
✓ Quick access Desktop ☑ Documents ✓ Downloads ✓ Pictures ✓ F\ ✓ Si5344 ✓ Si5344 ✓ Si5348 ☑ This PC ✓ Network	Organize 🔻 Nev	w folder			= 🔹 🛄	?
File name: Skyworks Timing Project V	 Desktop Documents Downloads Pictures F:\ Si5344 Si5346 Si5347 Si5348 This PC 	Name Si5346-RevD-5346EVB3-Project				
		File name:		 Skyworks Timing 	Project	~

Locate your CBPro design file in the Windows file browser.

Figure 23. Browse to Project File

Select Yes when the WRITE DESIGN to EVB popup appears:



Figure 24. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.8. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:



You can now write your device's complete configuration to file formats suitable for in-system programming.

About Regis	Register File	Settings File	Multi-Project Register,	Jettings	Regmap				
5				-	5 1				
This export	ster Export								
configuratio		e registers that	t need to be written to	the Si534	46 to achiev	e your de	sign/		
	l line version o rompt to learr		vailable. Type CBProPro	ojectRegi	stersExport	help fr	om a		
Options									
Export Type	:								
and d	ata fields. le Header File		lata pair in hexadecima						
The re			ressed in C code via ar	n array of	address, dat	ta pairs. T	his can	be	
If checke	by the # chara	tional header v	will be included at the der will contain some t						
Certain of This ens the dow	ures the devic	rs must be wri e is stable duri	egister writes tten before and after v ing configuration down urn inclusion of this se	nload and	resumes n	ormal ope	eration	after	J
🗌 I am tar	geting pre-pro	oduction samp	les 😮						

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5346 using Clock-Builder Pro on the Si5346-D-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5346 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

12. Si5346-D-EB Schematic and Bill of Materials (BOM)

The Si5346-D-EB Schematic and Bill of Materials (BOM) can be found online at

www.skyworksinc.com/support-ia

Note: Please be aware that the Si5346-D-EB schematic is in OrCad Capture *hierarchical format* and not in a typical "flat" schematic format.

SKYWORKS

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

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