TIMING AND SYNCHRONIZATION IN BROADCAST VIDEO

1. Introduction

Digitization of video signals has been common practice in broadcast video for many years. Early digital video was commonly encoded on a 10-bit parallel bus, but as higher processing speeds became practical, a serial form of the digitized video signal called the Serial Digital Interface (SDI) was developed and standardized. Serialization of the digital video stream greatly facilitates its distribution within a professional broadcast studio.

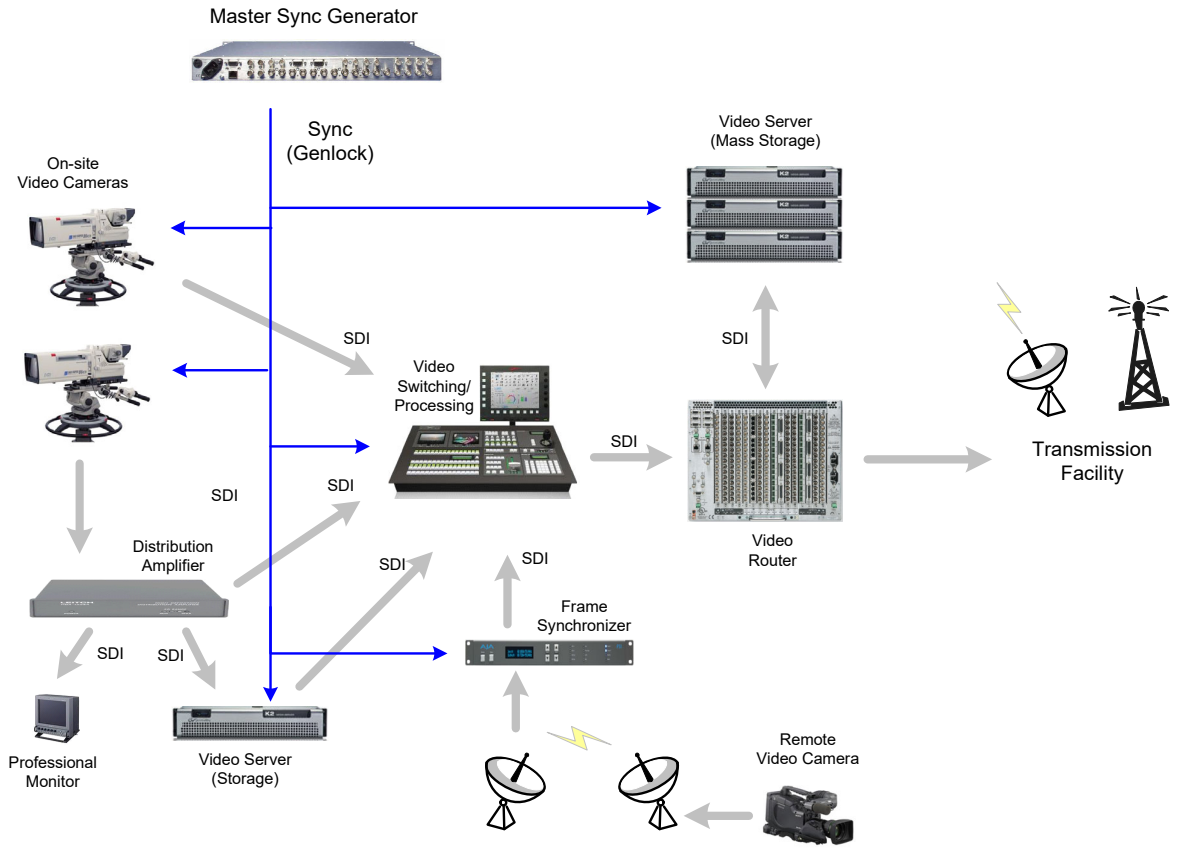


Figure 1. Typical Example of a Professional Broadcast Video

In a studio with multiple cameras, it is important that video signals coming from multiple sources are frame aligned or synchronized to allow seamless switching between video sources. For this reason, a synchronization signal is often distributed to all video sources using a master synchronization generator as shown in Figure 1. This allows video switching equipment to select between multiple sources without having to buffer and re-synchronize all of its input video signals. In this application note, we will take a closer look at the various components that make up a broadcast video system and how each of the components play a role in the synchronization chain.

2. Digitizing the Video Signal

A video camera uses sensors to capture and convert light to electrical signals that represent the three primary colors– red, green, and blue (RGB). Horizontal, vertical, and field synchronization (HVF) information is added to the signals so that the receiver can identify the top and the edge of the picture. The resulting RGB signals are converted to luma (Y) and color difference signals (PbPr) using a linear matrix to help reduce the transmitted data rate. Analog-to-Digital (A/D) converters digitize the band-limited YPbPr signals using a sampling rate determined by the timing generator.

The sample rate needed to capture video depends on its resolution. Table 1 lists the various sampling rates for common video formats. Note that the color difference (PbPr) signals are sampled at half the rate of the luma (Y) signal since human vision is more sensitive to changes in light intensity than changes in color. The three 10-bit luma and color difference video data streams are multiplexed to form a single higher rate 10-bit YCbCr stream, which is then serialized and encoded to meet SMPTE standards. Since the resultant SDI datastream is sampled using the timing generator, it becomes synchronous with the studio's master sync generator. This is referred to as genlocking in the video world.

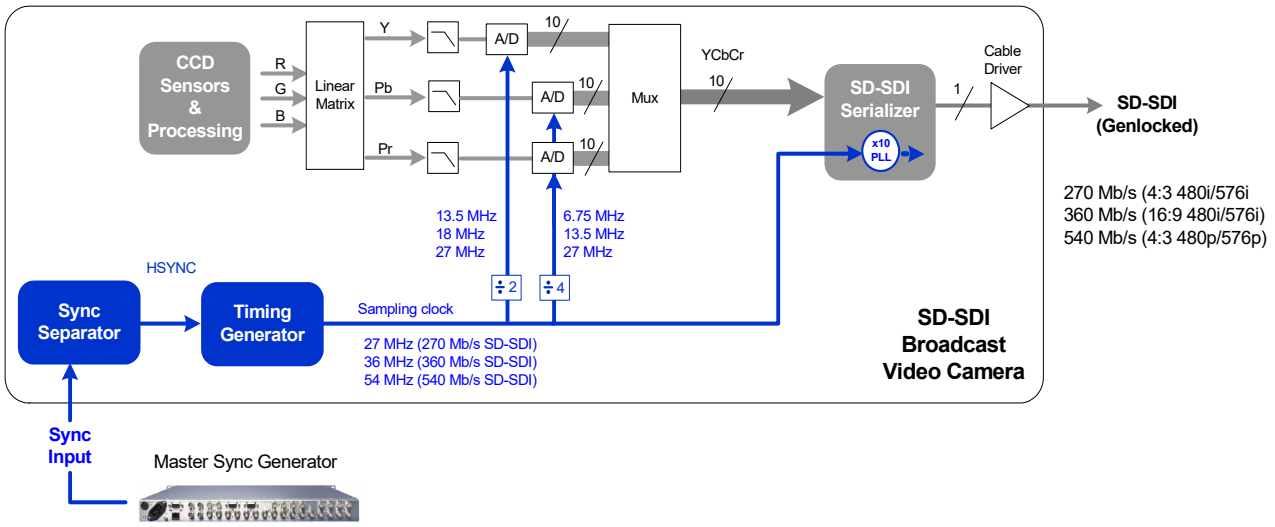


Figure 2. SD-SDI Professional Video Camera Supporting SMPTE 259M and 344M

Because of the higher resolution of an HD video signal, multiplexing of the YCbCr data is carried over two 10-bit buses instead of one. This is shown in Figure 3. The resulting 20-bit video stream is serialized using a 1.485 Gb/s HD-SDI link (SMPTE 292M) for 720p and 1080i video formats, and over two 1.485 Gb/s HD-SDI links (SMPTE 372M Dual Link SDI) or one 3G-SDI 2.97 Gb/s (SMPTE 424M/425M) link for support of the higher resolution 1080p video format. 3G-SDI has since replaced Dual Link SDI because it can be distributed over a a single cable. "Appendix A—Common SDI Standards" on page 17 provides a list of relevant SD and HD-SDI standards used in the video broadcasting industry.

Table 1. Common Video Formats and their Associated Sampling Rates*

Video Format	Aspect Ratio	NTSC/ PAL/HDTV	Frame Rate* (Hz)	Y Sample Rate (MHz)	PbPr Sample Rate (MHz)	YCbCr Tx Rate (MHz)	YCbCr Bus Width	SDI Tx Rate	SMPTE Standard
720x480i	4:3	NTSC	30/ 1.001	**13.5**	**6.75**	**27**	10-bit	270 Mb/s	259M-C SD-SDI
960x480i	16:9	NTSC	30/ 1.001	**18**	**9**	**36**	10-bit	360 Mb/s	259M-D SD-SDI
720x480p	4:3	NTSC	60/ 1.001	**27**	**13.5**	**54**	10-bit	540 Mb/s	344M/347M
720x576i	4:3	PAL	25	**13.5**	**6.75**	**27**	10-bit	270 Mb/s	259M-C SD-SDI
960x576i	16:9	PAL	25	**18**	**9**	**36**	10-bit	360 Mb/s	259M-D SD-SDI
720x576p	4:3	PAL	50	**27**	**13.5**	**54**	10-bit	540 Mb/s	344M/347M
960x720p	16:9	HDTV	60	**74.25**	**37.125**	**74.25**	20-bit	1.485 Gb/s	292M HD-SDI
1280x720p	16:9	HDTV	60/ 1.001	**74.25/ 1.001**	**37.125/ 1.001**	**74.25/ 1.001**	20-bit	1.485/1.001 Gb/s	292M HD-SDI
1280x720p	16:9	HDTV	50	**74.25**	**37.125**	**74.25**	20-bit	1.485 Gb/s	292M HD-SDI
1920x1080i	16:9	HDTV	30	**74.25**	**37.125**	**74.25**	20-bit	1.485 Gb/s	292M HD-SDI
1920x1080i	16:9	HDTV	30/ 1.001	**74.25/ 1.001**	**37.125/ 1.001**	**74.25/ 1.001**	20-bit	1.485/1.001 Gb/s	292M HD-SDI
1920x1080i	16:9	HDTV	25	**74.25**	**37.125**	**74.25**	20-bit	1.485 Gb/s	292M HD-SDI
1920x1080p	16:9	HDTV	60	**148.5**	**74.25**	**148.5**	2x 10-bit 1x 20-bit	2.97 Gb/s	372M Dual Link SDI 424M/425M 3G-SDI
1920x1080p	16:9	HDTV	60/ 1.001	**148.5/ 1.001**	**74.25/ 1.001**	**148.5/ 1.001**	2x 10-bit 1x 20-bit	2.97/1.001 Gb/s	372M Dual Link SDI 424M/425M 3G-SDI
1920x1080p	16:9	HDTV	50	**148.5**	**74.25**	**148.5**	2x 10-bit 1x 20-bit	2.97 Gb/s	372M Dual Link SDI 424M/425M 3G-SDI

Notes:

1. In North America, the dominant broadcast HDTV standards are 720p60 and 1080i/30. In Europe, 720p50 and 1080i/25 have been adopted.
2. Non-integer frame rates were introduced when color was incorporated into the NTSC monochrome signal in the early 1950s. This new frame rate is obtained by dividing the even frame rate by 1.001.

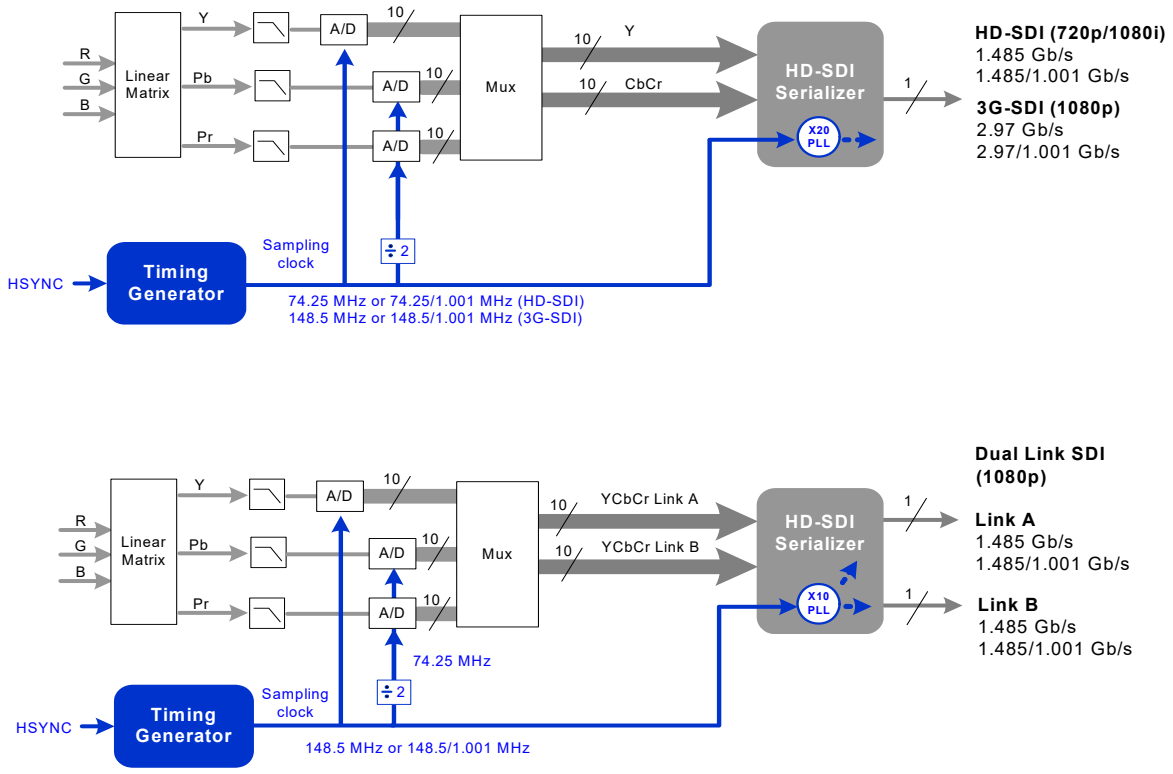


Figure 3. Multiplexing HD Video (SMPTE 292M HD-SDI, 424M 3G-SDI, 372M Dual Link SDI)

3. Genlocking - Synchronization of Video Equipment

In a studio with multiple cameras, it is desirable to synchronize all video sources to facilitate downstream video processing such as switching, editing, keying, fading, etc. This process is known as genlocking the video equipment and is achieved by synchronizing all of the video sources to a common synchronization signal. As illustrated in Figure 1, the master sync generator provides a common synchronization reference to all equipment that generates a video source.

A common signal used in professional studios for genlocking video equipment is known as black burst or color black. This is essentially an analog composite video signal without the video information. The process of extracting timing from the black burst signal is shown in Figure 4.

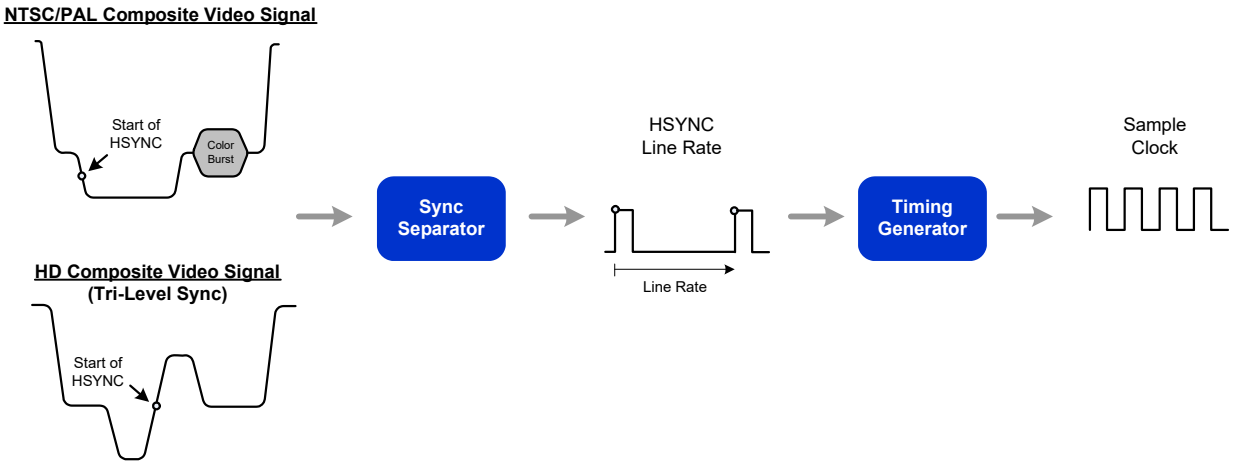


Figure 4. Extracting HSYNC from an Analog Composite Video Signal

A sync separator removes the unwanted portions of the composite video signal and leaves the timing portion of the signal, which can be locked to by a timing generator. The horizontal sync pulse (HSYNC) is commonly used as a timing reference since it occurs as a repetitive and accurate rate. The timing generator locks to the HSYNC signal, filters jitter, and generates the video sampling clock. A list of common HSYNC rates and sample rates is shown in Table 2.

Table 2. Common Video Formats and their HSYNC and Sampling Rates

Video Format	Aspect Ratio	NTSC/ PAL/HDTV	Frame Rate (Hz)	Pixels per line	HSYNC Line Rate (kHz)	Sample Clock (MHz)
720x480i	4:3	NTSC	30/ 1.001	858	**15.75/ 1.001**	**13.5**
960x480i	16:9	NTSC	30/ 1.001	1144	**15.75/ 1.001**	**18**
720x480p	4:3	NTSC	60/ 1.001	858	**31.5/ 1.001**	**27**
720x576i	4:3	PAL	25	864	**15.625**	**13.5**
960x480p	16:9	NTSC	60/1.001	1144	**31.5/ 1.001**	**36**
960x576i	16:9	PAL	25	1152	**15.625**	**18**
960x576p	16:9	PAL	50	1152	**31.25**	**36**
720x576p	4:3	PAL	50	1152	**31.25**	**27**
1280x720p	16:9	HDTV	60	1650	**45**	**74.25**
1280x720p	16:9	HDTV	60/ 1.001	1650	**45/ 1.001**	**74.25/ 1.001**
1280x720p	16:9	HDTV	50	1980	**37.5**	**74.25**
1280x720p	16:9	HDTV	30	3300	**22.5**	**74.25**
1280x720p	16:9	HDTV	30/ 1.001	3300	**22.5/ 1.001**	**74.25/ 1.001**
1280x720p	16:9	HDTV	25	3960	**18.75**	**74.25**

Table 2. Common Video Formats and their HSYNC and Sampling Rates

Video Format	Aspect Ratio	NTSC/ PAL/HDTV	Frame Rate (Hz)	Pixels per line	HSYNC Line Rate (kHz)	Sample Clock (MHz)
1280x720p	16:9	HDTV	24	4125	**18**	**74.25**
1280x720p	16:9	HDTV	24/ 1.001	4125	**18/ 1.001**	**74.25/ 1.001**
1920x1080i	16:9	HDTV	30	2200	**33.75**	**74.25**
1920x1080i	16:9	HDTV	30/ 1.001	2200	**33.75/ 1.001**	**74.25/ 1.001**
1920x1080i	16:9	HDTV	25	2640	**28.125**	**74.25**
1920x1080p	16:9	HDTV	60	2200	**67.5**	**148.5**
1920x1080p	16:9	HDTV	60/ 1.001	2200	**67.5/ 1.001**	**148.5/ 1.001**
1920x1080p	16:9	HDTV	50	2640	**56.25**	**148.5**
1920x1080p	16:9	HDTV	30	2200	**33.75**	**74.25**
1920x1080p	16:9	HDTV	30/ 1.001	2200	**33.75/ 1.001**	**74.25/ 1.001**
1920x1080p	16:9	HDTV	25	2640	**28.125**	**74.25**
1920x1080p	16:9	HDTV	24	2750	**27**	**74.25**
1920x1080p	16:9	HDTV	24/ 1.001	2750	**27/ 1.001**	**74.25/ 1.001**

4. The Need for Synchronization within Video Network Components

Many components are involved in the production of the final broadcast video signal. Video switchers accept video sources from multiple sources such as cameras and video storage devices. Distribution amplifiers send video signals around the studio and perform the job of a repeater to help clean up the signals they distribute. Timing generators and frame synchronizers ensure that all video sources are synchronized making the process of switching, keying, and editing possible. Video routers provide a single point for switching and routing video signals to and from other studios. Complicating the process further, many of these components also must support the multiple standard definition and high definition video formats that are available today. In this section, we will take a closer look at the various components that make up a video network and investigate their timing and synchronization requirements.

4.1. Frame Synchronizer

There are times when an asynchronous video signal needs to be synchronized to the studio's genlocked reference. A good example of this is when a studio receives a video signal from a remote camera that does not have access to the studio's master genlock synchronization signal. The frame synchronizer resolves the issue by buffering the un-synchronized video signal and re-timing it to the master synchronization source. This produces a synchronized (genlocked) copy of the video signal that can then be used by other video equipment in the studio. A block diagram of a frame synchronizer is shown in Figure 5.

The task of re-synchronizing the video frames requires that the video is buffered frame-by-frame and transmitted using the studio's genlock clock reference. In order for this to happen, the video must be de-serialized to its parallel 10-bit or 20-bit YCbCr component video format, buffered, and re-clocked out using the genlock reference provided by the timing generator. The parallel YCbCr component video is then serialized and output through the cable driver. The result is a genlocked SDI video signal that is synchronous with other video equipment in the studio.

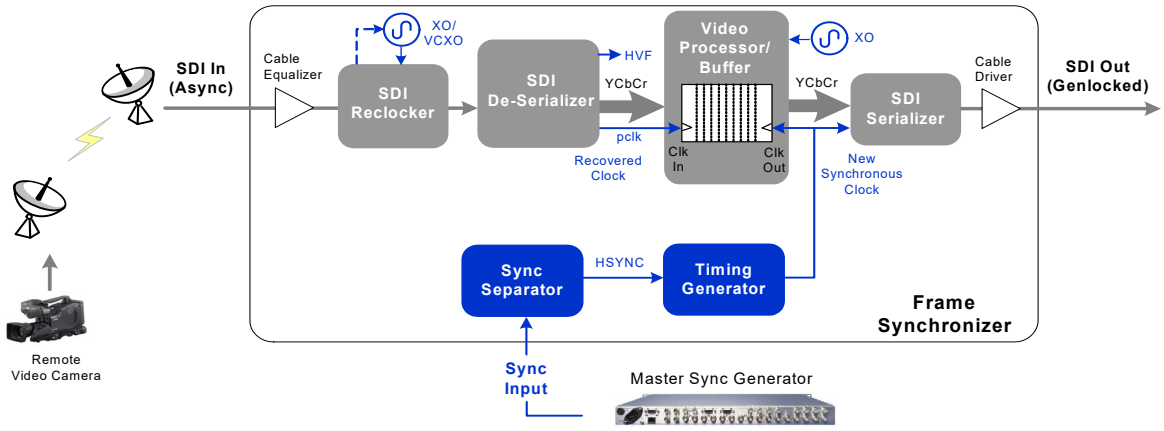


Figure 5. Block Diagram of a Framer Synchronizer

The SDI re-clocker helps remove alignment jitter from the SDI data stream using phase-locked loop circuitry, which usually requires an external reference from a crystal oscillator (XO) or voltage controlled oscillator (VCXO). Cable drivers are used to buffer the video signal to multiple sources.

4.2. Distribution Amplifier

Broadcast studios often use multiple video signals for production and some of these signals need to reach long distances. Distribution amplifiers are used to help extend the distance that the video signal can reach or to distribute a video signal to multiple sources. For example, a video signal from a camera might need to connect directly to a production switcher, a monitor, and a video storage device like a VTR or a video server. A block diagram of a distribution amplifier is shown in Figure 6.

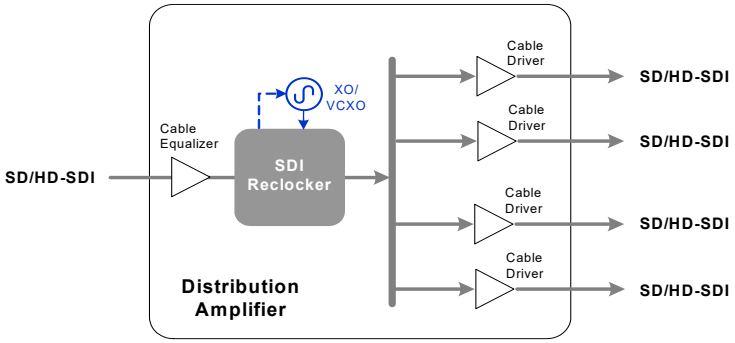


Figure 6. Block Diagram of a Distribution Amplifier

Distribution amplifiers use a cable equalizer to compensate for the inherent low pass characteristics of coaxial cables that carry the SDI video signals. The cable equalizer effectively extends the reach of the SDI cables to over 140 meters for HD signals and 300 meters for SD signals. More than one distribution amplifier can be used in the signal path to further extend its reach, but they should be used sparingly to maintain the best possible signal integrity. One of the issues with using long cables and multiple distribution amplifiers is jitter accumulation in the video signal.

4.3. Professional Video Monitor

At some point along the video path, we need to monitor its signal. Because of the multiple video formats available today, professional monitors used in broadcast studios usually accept SD and HD signals in both analog and digital formats. Before we can view a digital video signal, we need to reconstruct the video frames that we worked so hard to digitize and serialize. A block diagram of a professional video monitor is shown in Figure 7.

Similar to the frame synchronizer, the SDI signal needs to be equalized, reclocked, and de-serialized. An image processor re-organizes and scales the digital video component signal (YCbCr) to fit the particular display (CRT, LCD, or Plasma). Analog signals such as component YPbPr or RGB are usually digitized and processed similar to its digital counterpart before reaching the display.

Since the monitor is situated at the end of the video path, there is usually no need for re-synchronization of the video signal. The de-serializer recovers a clock and synchronization signals (HVF) from the serial datastream and passes them on to the image processor so that it knows how to “frame” the video pictures. The processor itself usually requires a clock of its own to run its processing engine, but this clock is typically asynchronous or unrelated to the video clock that it is processing.

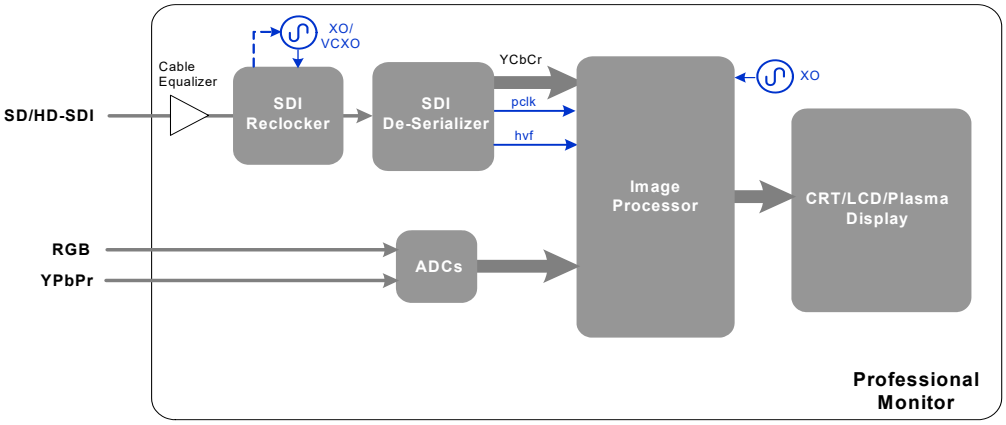


Figure 7. Block Diagram of a Professional Monitor

4.4. Video Switcher

The video switcher provides a meeting point for all video signals in the studio. This is where an operator monitors multiple video sources and switches between them to produce the final production video signal. Switching between video signals is not a trivial task, and without synchronization (or genlocking) it would be almost impossible. A block diagram of the video switcher is shown in Figure 8.

Before switching between two or more video sources, the individual video signals must be de-serialized, reconstructed frame-by-frame, and buffered. Precise alignment between video frames is necessary when combining video from different sources. Genlocking the video sources reduces the amount of buffering needed to keep the video frames aligned and ready for switching. After the video has been combined, it is serialized and re-timed to the master sync generator so that the video that it produces is synchronous with the rest of the studio’s equipment.

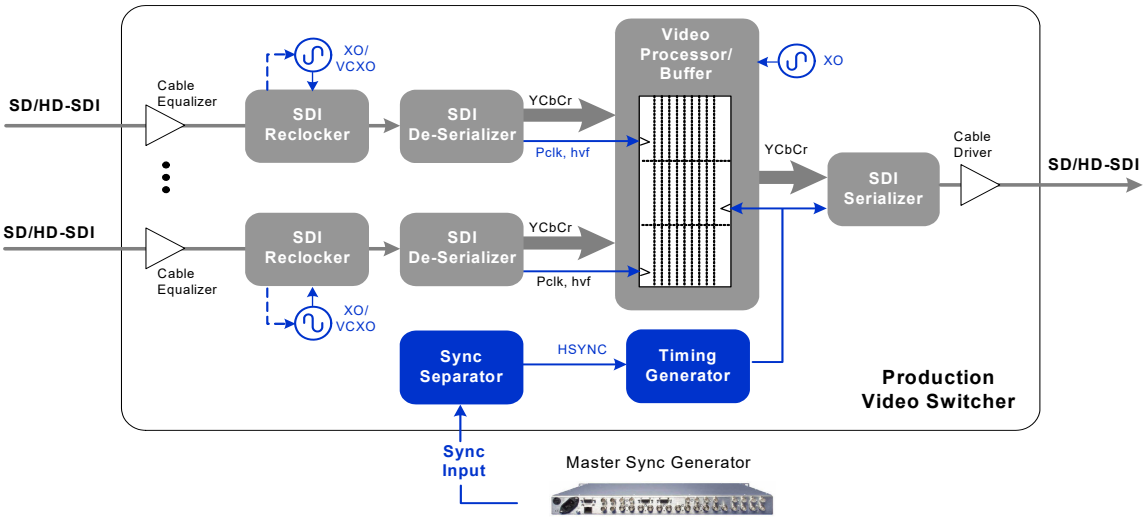


Figure 8. Block Diagram of a Video Switcher

4.5. Video Router

The video router acts like a switchboard for video signals. It routes video signals from one place to another. Video signals are switched through a cross-point matrix, re-clocked (or de-jittered), and sent to its destination. The video signal is processed as a serial stream from input to output. A block diagram of a video router is shown in Figure 9.

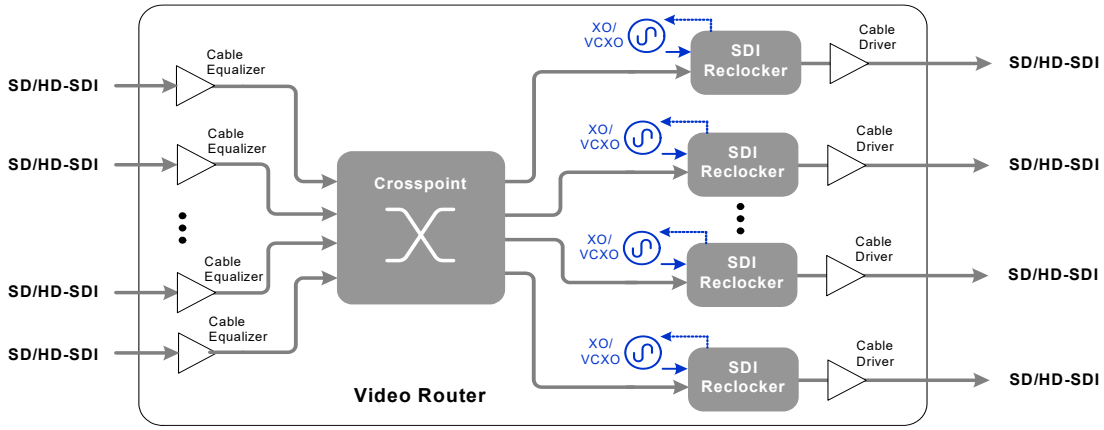


Figure 9. Block Diagram of a Video Router

4.6. Video Server (Storage)

Producing the final video stream requires mixing of live and pre-recorded material. The video server allows storage of live video so that it can be transmitted at a later time or mixed-in with live video from another source.

The SDI video signal is usually stored in a compressed digital form after going through equalization, jitter clean-up, and de-serialization. The process is reversed when the video is retrieved. Since synchronization of the video signal is lost during storage, it must be re-synchronized to the studio's master sync generator before moving on to downstream equipment. A block diagram of a video server is shown in Figure 10.

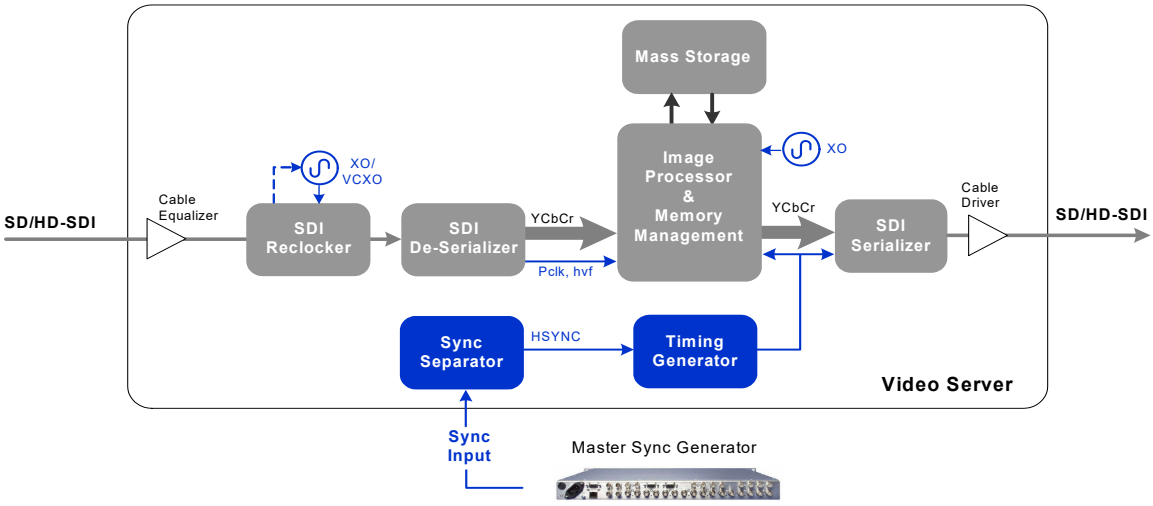


Figure 10. Block Diagram of a Video Server

4.7. Video Multi-format Converter

Because of the multiple video formats and resolutions available today, it is often necessary to convert video from one format to another. The de-serialization process extracts the component video (YCbCr) and timing signals (HVF) from the serial datastream so that a processor can convert the image to a different format. The resulting image is re-serialized and re-timed to the genlock synchronization signal.

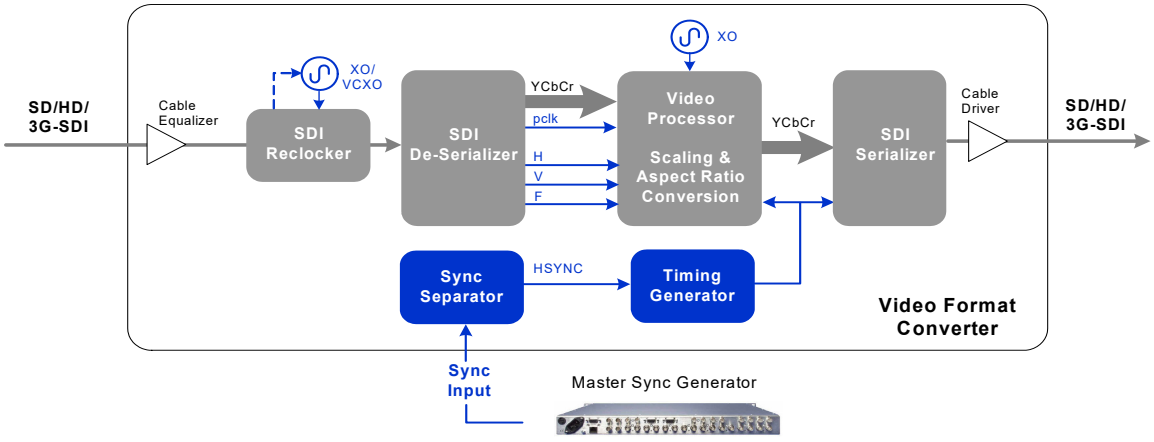


Figure 11. Block Diagram of a Video Format Converter

5. Jitter Requirements for Video Clocks

As the video signal travels through the interconnecting wires and the components that make up the video network, the digitized signal will accumulate jitter. If jitter becomes excessive, the video signal will deteriorate to the point where it is no longer usable or recoverable. For this reason, jitter reduction circuitry is included at several points throughout the video path to maintain signal integrity.

The process of recovering video from the SDI signal requires extracting both the data and a sampling clock from the datastream. This is known as clock and data recovery (CDR). Since the clock is recovered from the SDI datastream itself, it will track its jitter but only within the loop bandwidth of the phase-locked loop (PLL) based CDR circuitry. Jitter that occurs above this loop bandwidth will not be tracked; it will be filtered. Although recovering a jitter filtered clock sounds like a good idea, it can cause decoding errors if there is still excessive jitter present on the data. For this reason, SMPTE has specified limits on the jitter content of SDI signals.

SMPTE defines two types of jitter: timing jitter and alignment jitter. Timing jitter covers the entire jitter frequency spectrum starting at 10 Hz. Alignment jitter focuses on the jitter frequency spectrum that CDR circuits cannot track. Therefore, alignment jitter has a much more powerful impact on system performance and as a result has tighter limits. Figures 12 and 13 provide a summary of the jitter bandpass and jitter limits for both SD-SDI and HD-SDI.

		Timing Jitter		Alignment Jitter	
		Bandpass		Bandpass	
SMPTE Standards	Serial Data Rate	Lower Limit (f_1)	Upper Limit (f_4)	Lower Limit (f_3)	Upper Limit (f_4)
259M-C	270 Mb/s	10 Hz	>27 MHz	1 kHz	>27 MHz
259M-D	360 Mb/s	10 Hz	>36 MHz	1 kHz	>36 MHz
344M	540 Mb/s	10 Hz	>54 MHz	1 kHz	>54 MHz
292M	1.485 Gb/s	10 Hz	>148 MHz	100 kHz	>148 MHz
424M	2.97 Gb/s	10 Hz	>297 MHz	100 kHz	>297 MHz

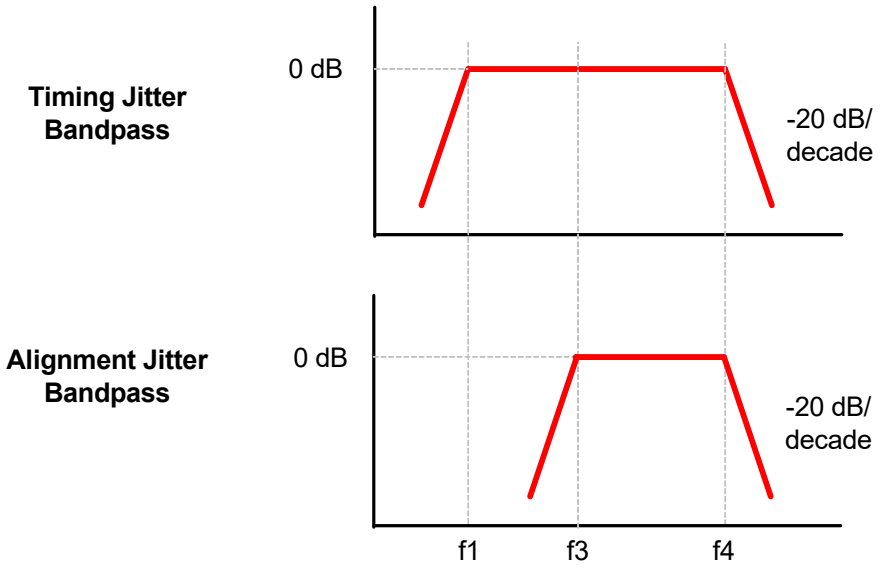


Figure 12. Jitter Measurement Bandpass

		Timing Jitter				Alignment Jitter			
		Bandpass		Jitter Limit pk-pk (A1)		Bandpass		Jitter Limit pk-pk (A2)	
SMPTE Standards	Serial Data Rate	Lower Limit (f_1)	Upper Limit (f_4)			Lower Limit (f_3)	Upper Limit (f_4)		
259M-C	270 Mb/s	10 Hz	>27 MHz	1.0 UI	3.70 ns	1 kHz	>27 MHz	0.2 UI	740 ps
259M-D	360 Mb/s	10 Hz	>36 MHz	1.0 UI	2.78 ns	1 kHz	>36 MHz	0.2 UI	555 ps
344M	540 Mb/s	10 Hz	>54 MHz	1.0 UI	1.85 ns	1 kHz	>54 MHz	0.2 UI	370 ps
292M	1.485 Gb/s	10 Hz	>148 MHz	1.0 UI	673 ps	100 kHz	>148 MHz	0.2 UI	134 ps
424M	2.97 Gb/s	10 Hz	>297 MHz	2.0 UI	673 ps	100 kHz	>297 MHz	0.2 UI	67 ps

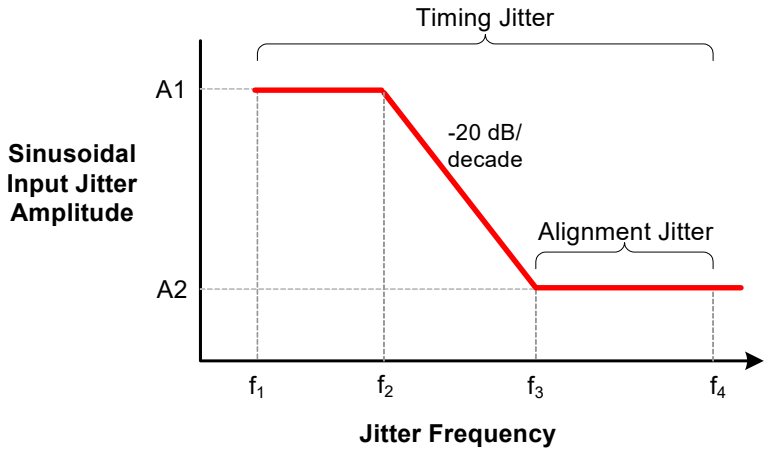


Figure 13. Output Jitter Limits for SDI Clocks

5.1. Jitter Filtering

The SDI re-clocker is very effective at filtering alignment jitter because the alignment jitter frequency content is beyond the bandwidth of the CDR circuits, so it cannot be tracked. As a result, the re-sampled SDI signal becomes free of alignment jitter. It is important that alignment jitter is kept under control in the SDI datastream, otherwise decoding errors will occur.

Lower frequency timing jitter is easily tracked by the CDR circuits, so timing jitter can easily accumulate as the video signal propagates through the video path. PLLs with loop bandwidths closer to the 10 Hz level are needed to filter timing jitter. This is a function that is commonly performed in the timing generator.

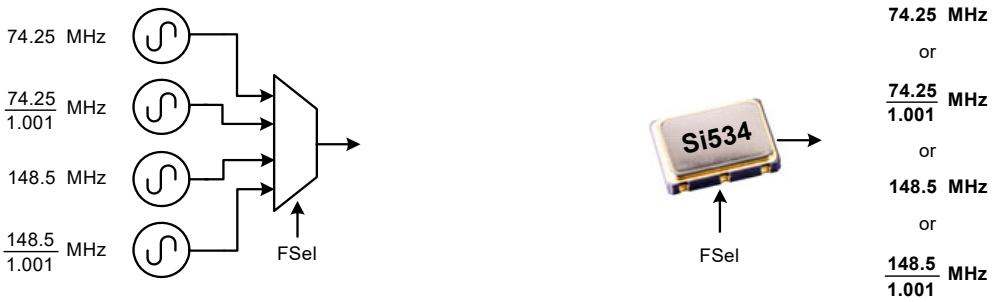
6. Simplifying Timing and Synchronization in Video Networks

There is no doubt that timing and synchronization plays a critical role in successful processing and distribution of the video signal within a studio. Because of the multiple standardized video formats available today, both the asynchronous oscillators (XOs) and the phase-locked loops (PLLs) that make up the timing path need to be flexible enough to support multiple clock rates and frequencies. Often PLLs need to translate (or convert) between non-integer related frequencies as in the case of a timing generator that needs to synchronize to an NTSC HSYNC rate and generate an HD-SDI sample clock for an SDI serializer (e.g., locking to 15.75/1.001 kHz to generate 74.25/1.001 MHz requires a multiplication ratio of 4719000/1001 or 4.71428571428571).

An ideal solution would support all of the video clock rates and conversions in a single programmable device. In this section, we will take a look at a few products that help to simplify the design of timing and synchronization of multi-format video equipment.

6.1. Asynchronous Clocks

As explained in Section 4, some of the timing references required in video components are asynchronous. A good example of this is with devices like the SDI Re-Clocker, which usually requires an external crystal oscillator (XO) as a reference clock for its internal clock and data recovery (CDR) circuitry. Depending on SDI data rate, this clock reference could be any of the clock rates shown in Figure 14. The traditional approach to generating these clock frequencies has been to use multiple discrete XOs and a mux for selection. The Si534 Quad Frequency Crystal Oscillator simplifies this process by generating up to four different clock frequencies from a single industry standard 5 x 7 mm package. Frequency selection pins (FSel) are used to determine the frequency of the output clock. Other devices in the Si53x family support single and dual frequency options.



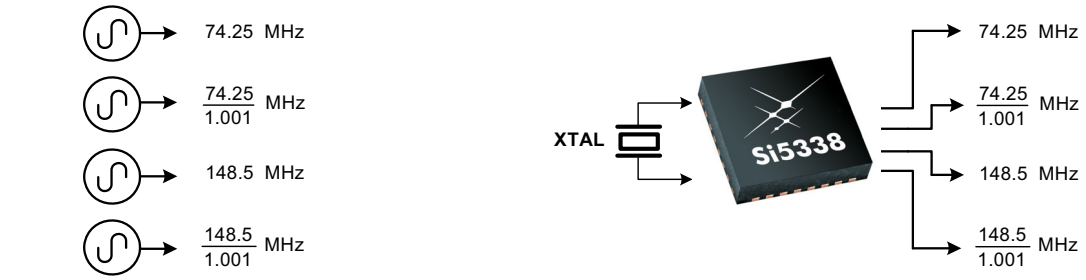
Traditional Method of Selecting and Generating Video Frequencies

Simplifying the Generation and Selection of Video Frequencies

Figure 14. Simplifying Clock Generation and Selection Using the Si534

Video processors and FPGAs often need several asynchronous clocks to operate their digital functions. As shown in Figure 15, the Si5338 I^2C Programmable Any-Rate, Any-Output Quad Clock Generator synthesizes four simultaneous and independent clock rates from a low cost crystal (XTAL).* This device is ideally suited for replacing discrete clock oscillators, and since it is fully programmable, it can generate all the frequencies needed to accommodate multiple video rates and processor speeds.

***Note:** The Si5338 can also synchronize to an external timing reference instead of an XTAL



Traditional Method of Generating Multiple Video Clock frequencies

Simplifying Multiple Clock Generation

Figure 15. Simplifying Clock Generation of Multiple Clocks Using the Si5338

6.2. Frequency Controlled Clocks

For applications that need a synchronous clock, the Si554 Quad Frequency Voltage Controlled Crystal Oscillator (VCXO) provides the same frequency selectability as the Si534 XOs, but adds a voltage control input. This allows designers to implement their own FPGA-based phase-locked loop solutions to support multiple video data rates using a single VCXO. A typical application of this is shown in Figure 16.

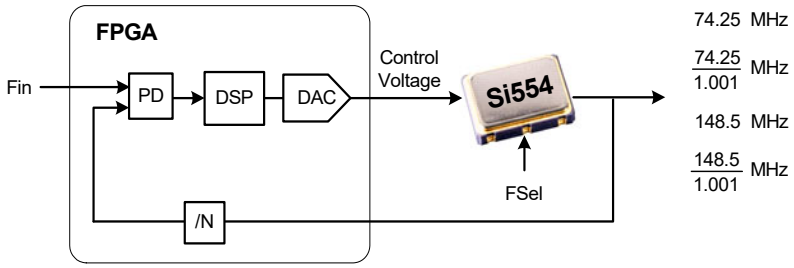


Figure 16. FPGA-Based VCXO PLL Supporting Multiple Video Standards

An alternative implementation of an FPGA-based PLL using a digitally controlled crystal oscillator (DCXO) is also shown in Figure 17. In this case, the FPGA controls the output frequency digitally using an Si570 Any-Rate I^2C Programmable XO/VCXO instead of an analog control voltage. This eliminates the need for the digital-to-analog conversion process that inherently contributes to added output jitter.

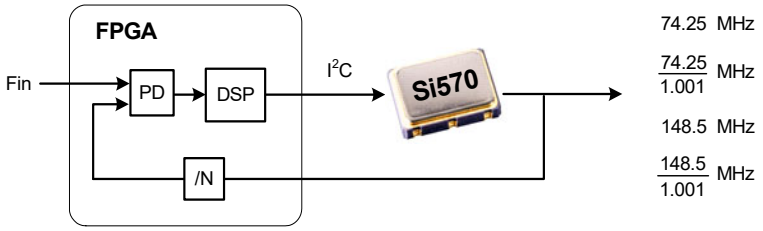


Figure 17. FPGA-Based DCXO PLL Supporting Multiple Video Standards

6.3. Synchronous Clocks

An even simpler method of implementing a multi-format video phase-locked loop is to use an integrated PLL device like the Si5324 Any-Rate Precision Clock Multiplier/Jitter Attenuator. Because of its highly programmable frequency conversion rates, sub 10 Hz loop bandwidth, and excellent intrinsic jitter performance, the Si5324 makes an ideal PLL for genlock applications in equipment like professional cameras, production switchers, frame synchronizers, video servers, format converters, etc. A typical application is shown in Figure 18.

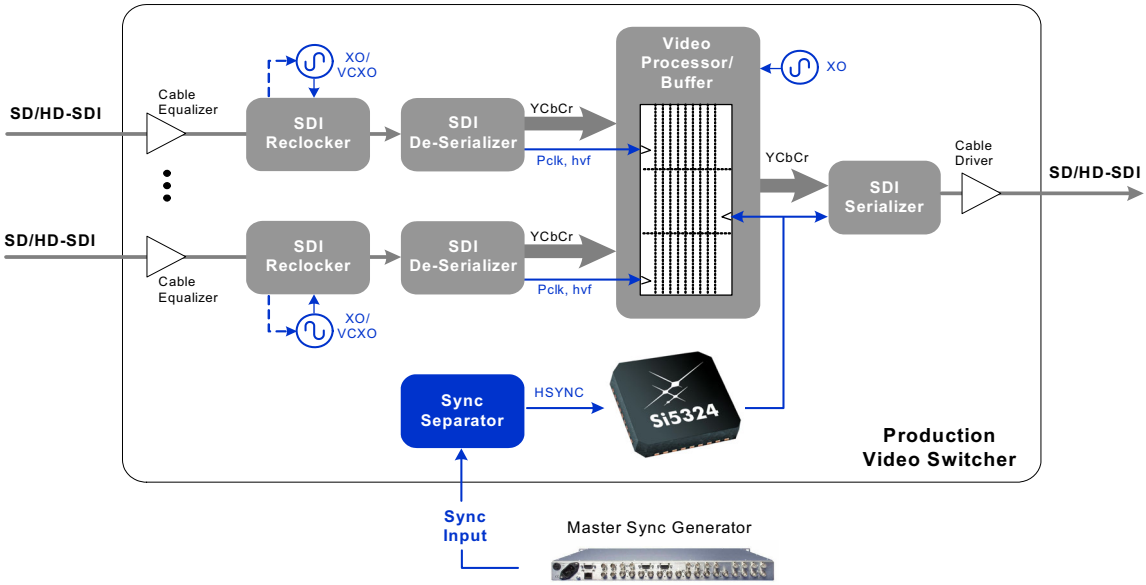


Figure 18. Simplifying Genlock Applications Using the Si5324

7. Conclusion

We have seen that synchronization plays a critical role in the broadcast studio. Not only is it necessary within the video signal itself so that the receiver knows how to frame the pictures that it receives, but it is also necessary at the physical level to ensure proper serialization and de-serialization of the video signal. The oscillators and phase-locked loops that make synchronization possible in these video systems need to provide multiple frequencies to support today's variety of standard definition and high definition resolutions. Not only is flexible frequency conversion important, but controlling jitter with properly placed jitter filters is critical in successful recovery of the video signal as it propagates through the video equipment within a studio.

Because of its long history of providing ultra low jitter and highly configurable frequency oscillators and phase-locked loops, Skyworks Solutions provides the perfect solution for bridging the frequency gap between today's multiple video standards.

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APPENDIX A—COMMON SDI STANDARDS

SMPTE Standard	Serial Format	Title and Description
SMPTE 259M	SD-SDI	Serial Digital Interface at 143Mb/s, 177Mb/s, 270Mb/s, 360Mb/s ■ 259M-C specifies 270 Mb/s for 480i and 576i 4:3 standard definition ■ 259M-D specifies 360 Mb/s for 480i and 576i 16:9 standard definition ■ 259M-A and 259M-B (143 Mb/s and 177 Mb/s) interfaces have since become obsolete
SMPTE 344M	SD-SDI	540 Mb/s Serial Digital Interface ■ Expands on SMPTE 259M allowing for data rates of 540 Mb/s for extended definition TV (EDTV) resolutions of 480p and 576p ■ Defines the physical interface
SMPTE 347M	SD-SDI	540 Mb/s Serial Digital Interface-Source Image Format Mapping ■ 347M defines YCbCr mapping
SMPTE 292M	HD-SDI	1.5 Gb/s Signal/Data Serial Interface ■ 1.485 Gb/s and 1.485/1.001 Gb/s data rates supporting 720p60, 720p59.94, 720p50, 1080i30, 1080i29.97, 1080i25
SMPTE 372M	Dual Link SDI	Dual Link 292M Interface for 1920 x 1080 Picture Raster ■ Defines a 3 Gb/s link carried over two 1.485 Gb/s or 1.485/1.001 Gb/s links supporting 1080p
SMPTE 424M	3G-SDI	3 Gb/s Signal/Data Serial Interface ■ 2.97 Gb/s and 2.97/1.001 Gb/s data rates over a single cable supporting 1080p60, 1080p59.94, 1080p50 ■ 3G-SDI has recently replaced the Dual Link SDI interface (372M). ■ Defines the physical interface
SMPTE 425M	3G-SDI	3 Gb/s Signal/Data Serial Interface - Source Image Formatting ■ 425M defines the YCbCr mapping
SMPTE RP 184		Specification of Jitter in Bit-Serial Digital System ■ Provides definition of jitter for SDI systems

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