TERMINATION OPTIONS FOR ANY-FREQUENCY, ANY-OUTPUT CLOCK GENERATORS AND CLOCK BUFFERS

1. Introduction

This application note provides termination recommendations for connecting input and output clock signals to the Si533x and Si5356/55 family of timing ICs and is not applicable to any other Skyworks Solutions devices.

The Si533x and Si5356/55 family of any-frequency, any-output clock generators and clock buffers greatly simplifies the task of interfacing between many of today's common signal types. Both the inputs and the outputs are compatible with single-ended (LVTTL, CMOS, HSTL, SSTL) and/or differential signals (LVPECL, LVDS, HCSL, CML) and support multiple supply voltage levels (3.3, 2.5, 1.8, or 1.5 V). All of the inputs and outputs are configured on a per-port basis offering unprecedented flexibility. Block diagrams of the devices are shown in Figures 1 and 2. The Si5338 and Si5356 are I^2C-configured devices that lock to a crystal or external clock and generate up to four independent output frequencies. The Si5338 is compatible with both single-ended and differential clock formats, whereas the Si5356 is limited to single-ended clocks. The Si5334 is a pin-controlled version of the Si5338 that does not have an I^2C interface. Similarly, the Si5355 is a pin-controlled version of the Si5356. The Si5330 is a non-PLL clock buffer device that provides low jitter clock distribution and level translation.

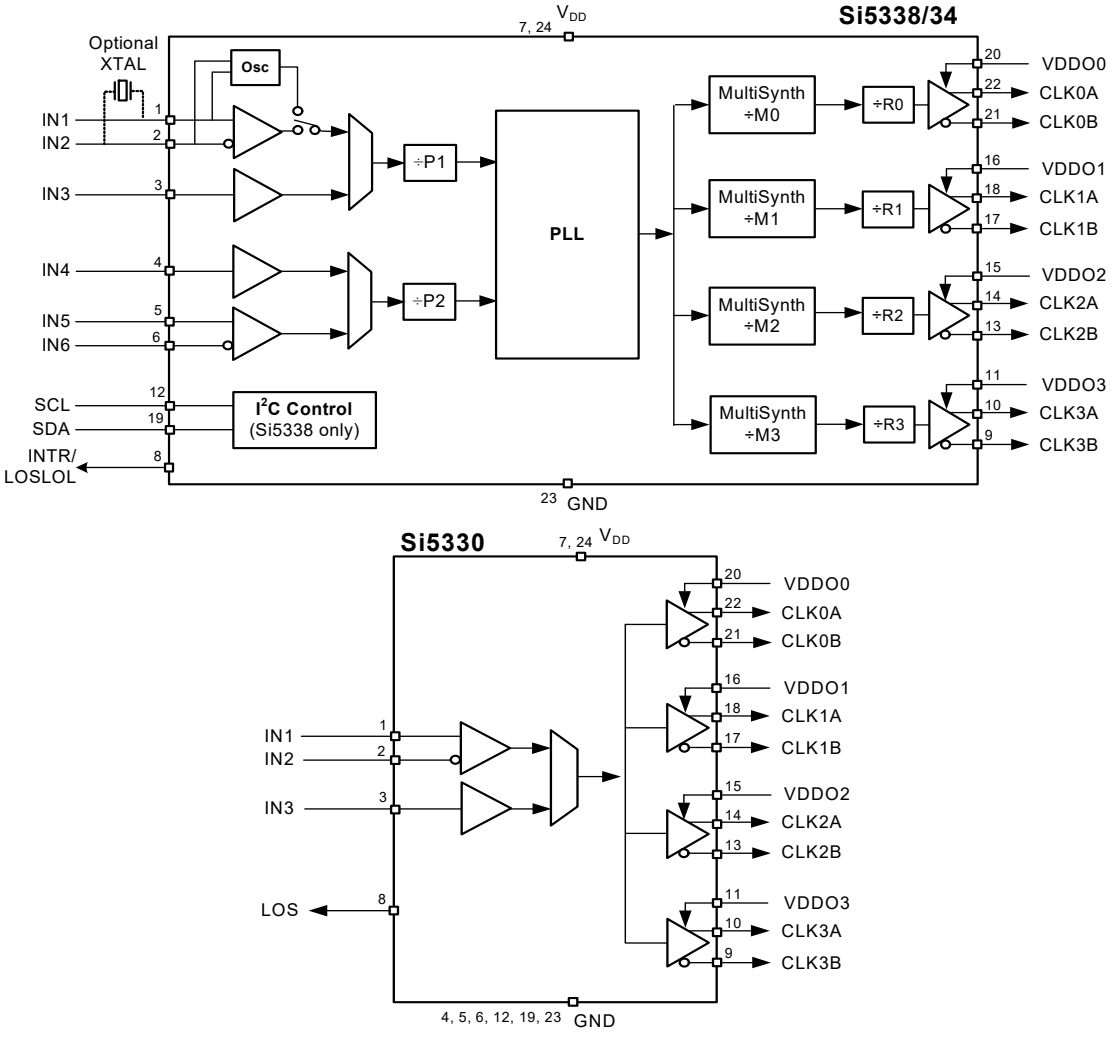


Figure 1. Si5338/34 and Si5330 Block Diagrams

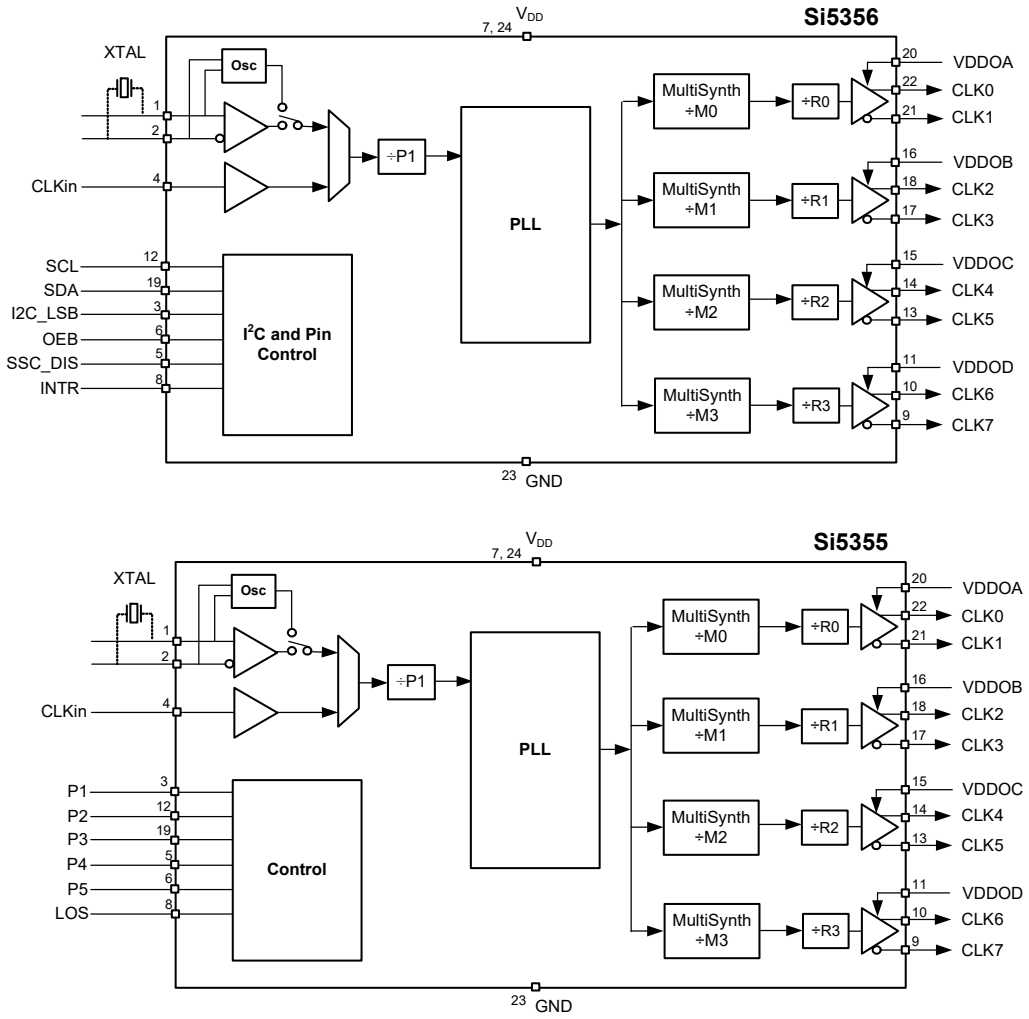


Figure 2. Si5356 and Si5355 Block Diagrams

2. Inputs

The Si533x and Si5356/55 families support both single-ended and differential inputs. The device supports up to two single-ended inputs (Pins 3 and 4) and two differential inputs (Pins 1,2, and 5,6). On the Si5338/34 and Si5356/55 devices, a crystal can be connected to Pins 1 and 2 instead of an input clock. Refer to “AN360: Crystal Selection Guide for Any-Frequency Devices” for more information on using the crystal input option.

2.1. Single-Ended Inputs

The multi-format single-ended clock inputs of the Si533x and Si5356/55 are ac-coupled internally to remove any dc bias from the signal. This allows the device to trigger on a signal swing threshold instead of a specific voltage level (normally specified as V_{IH} and V_{IL}). The receiver accepts any signal with a minimum voltage swing of 800 mV_{PP} and a maximum of 3.73 V_{PP} regardless of the core V_{DD} supply. For best performance, the slew rate at input Pins 3 and 4 must be greater than 1 V/ns. This makes the inputs 3.3 V-tolerant even when the core voltage is powered with 1.8 V. An Si5338/34/56/55 should have an input duty cycle no worse than 40/60%. An Si5330 should have an input duty cycle no worse than 45/55%.

2.1.1. LVTTL/CMOS Inputs

The only termination necessary when interfacing a CMOS driver to the Si533x and Si5356/55 is a source resistor (Rs) placed near the driver to help match its output impedance to the transmission line impedance. In some cases, the value for this series resistor may be zero as it depends upon the CMOS driver characteristics. The CMOS drivers in the Si533x and Si5356/55 are designed to work optimally into a 50 Ω transmission line without an external source resistor. A typical CMOS signal connection is illustrated in Figure 3. Using this configuration, the receiver is capable of interfacing to 3.3, 2.5, or 1.8 V CMOS clock signals.

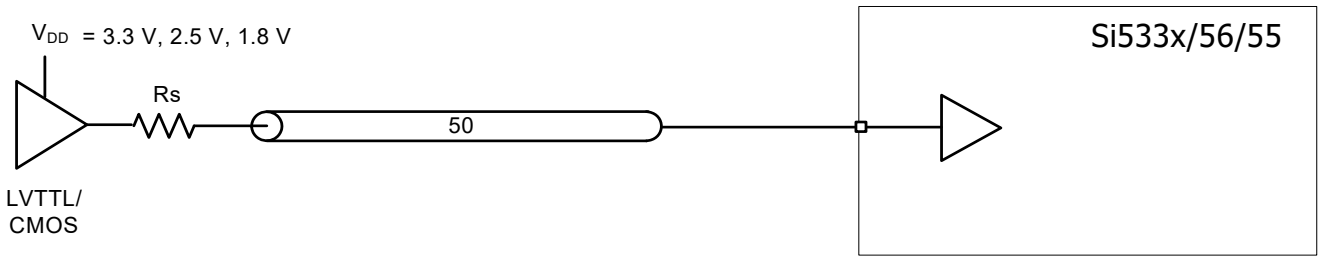


Figure 3. Interfacing to an LVTTL/CMOS Input Signal

2.1.2. Single-Ended SSTL and HSTL Inputs

HSTL and SSTL single-ended clock inputs should be input to the differential inputs, pins 1 and 2, of the Si533x with the circuit shown in Figure 4.

Some drivers may require a series 25 Ω resistor. If the SSTL/HSTL input is being driven by another Si533x device, the 25 Ω series resistor is not required as this is integrated on-chip. The maximum recommended input frequency in this case is 350 MHz.

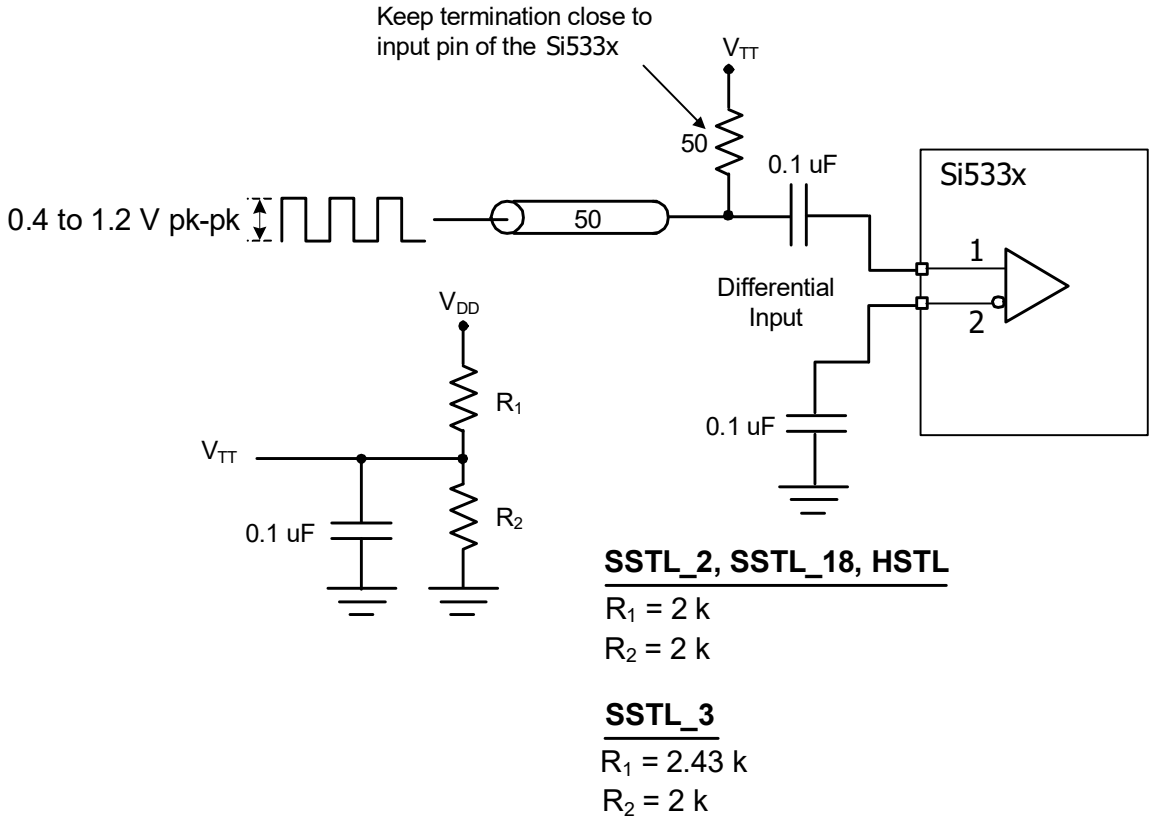


Figure 4. Single-Ended SSTL/HSTL Input to Pins 1 and 2

2.1.3. Applying a Single-Ended Signal to a Differential Input

It is possible to interface any single-ended signal to the differential input pins (IN1/IN2 or IN5/IN6). The recommended interface for a signal that requires a 50 Ω load is shown in Figure 5. On these inputs, it is important that the signal level be less than 1.2 V_{PP} SE and greater than 0.4 V_{PP} SE. The maximum recommended input frequency in this case is 350 MHz.

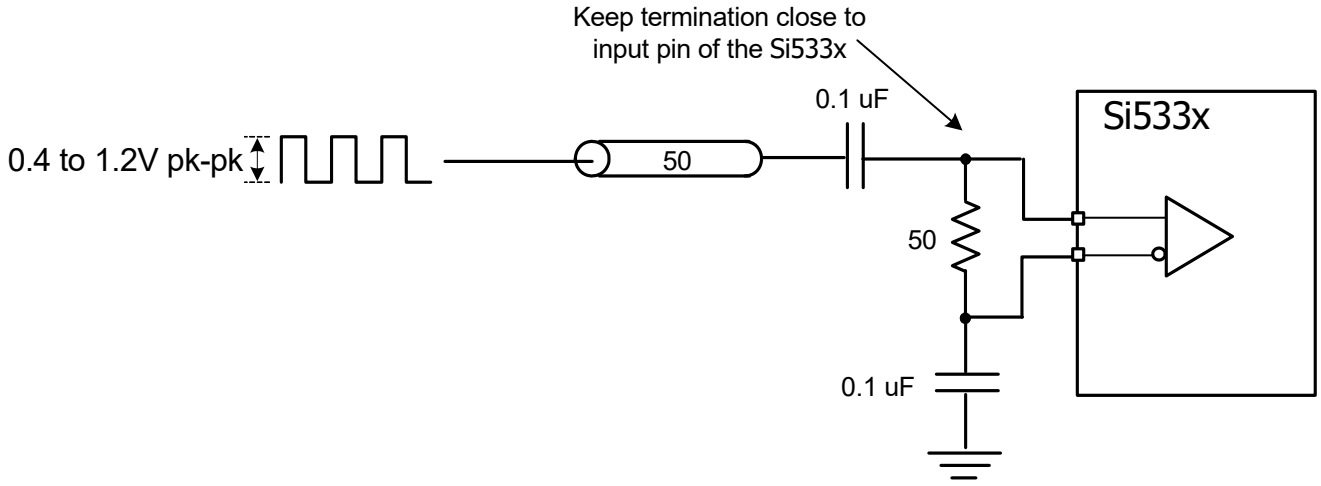


Figure 5. Single-Ended Input Signal with 50 Ω Termination

2.2. Differential Inputs

The multi-format differential clock inputs of the Si533x will interface with today's most common differential signals, such as LVDS, LVPECL, CML, and HCSL. The differential inputs are internally self-biased *and must be ac-coupled externally with a 0.1 µF capacitor*. The receiver will accept a signal with a voltage swing between 400 mV and 2.4 V_{PP} differential. Each half of the differential signal must not exceed 1.2 V_{PP} at the input to the Si533x or else the 1.3 V dc voltage limit may be exceeded.

2.2.1. LVDS Inputs

When interfacing the Si533x device to an LVDS signal, a 100 Ω termination is required at the input along with the required dc blocking capacitors as shown in Figure 6.

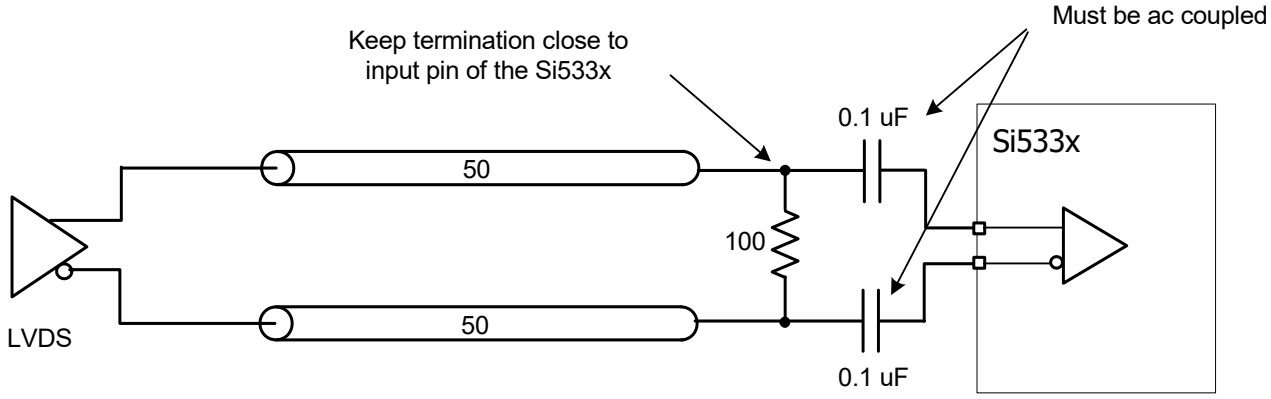
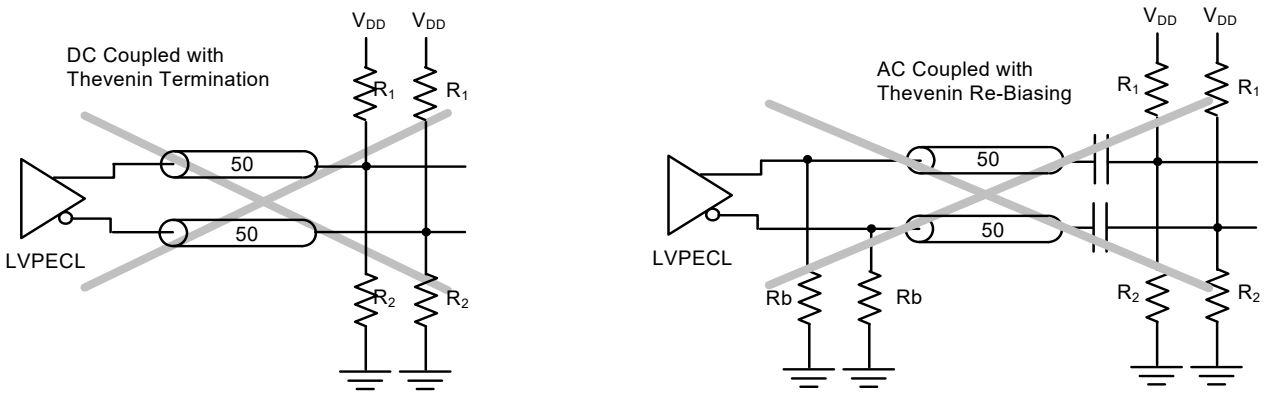


Figure 6. LVDS Input Signal

2.2.2. LVPECL Inputs

Since the differential receiver of the Si533x is internally self biased, an LVPECL signal may not be dc-coupled to the device. Figure 7 shows some common LVPECL connections that should not be used because of the dc levels they present at the receiver's input.



Not Recommended

Figure 7. Common LVPECL Connections that May be Destructive to the Si533x Input

Recommended configurations for interfacing an LVPECL input signal to the Si533x are shown in Figure 8. Typical values for the bias resistors (Rb) range between 120 and 200 Ω depending on the LVPECL driver. The 100 Ω resistor provides line termination. Because the receiver is internally self-biased, no additional external bias is required.

Another solution is to terminate the LVPECL driver with a Thevenin configuration as shown in Figure 8b. The values for R_1 and R_2 are calculated to provide a 50Ω termination to V_{DD}-2V. Given this, the recommended resistor values are R_1 = 127 Ω and R_2 = 82.5 Ω for V_{DD} = 3.3 V, and R_1 = 250 Ω and R_2 = 62.5 Ω for V_{DD} = 2.5 V.

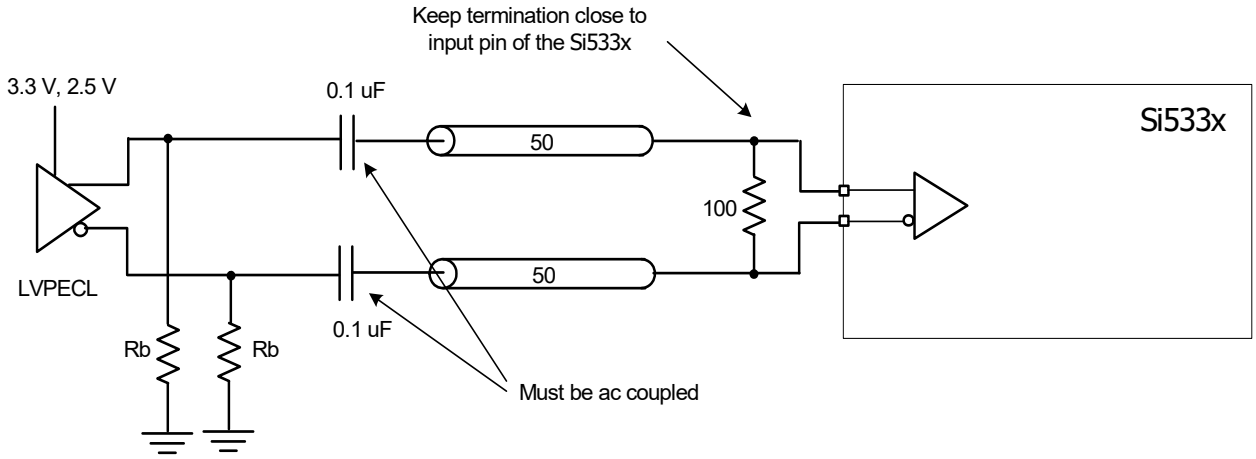


Figure 8a—LVPECL Input Signal with Source Biasing Option

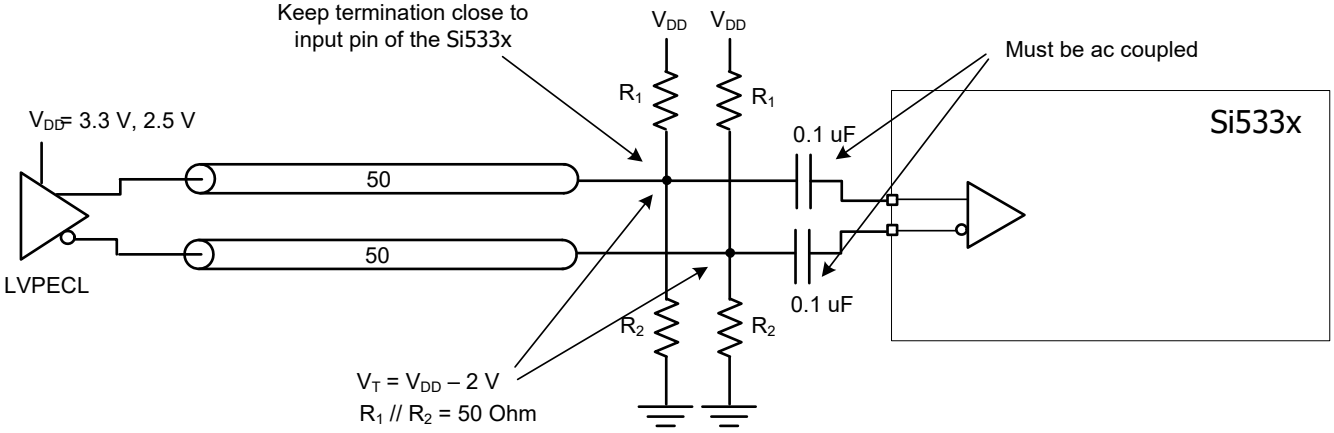


Figure 8b—LVPECL Input Signal with Load Biasing Option

Figure 8. Recommended Options for Interfacing to an LVPECL Signal

2.2.3. CML Inputs

CML signals may be applied to the differential inputs of the Si533x. Since the Si533x differential inputs are internally self-biased, a CML signal may not be dc-coupled to the device.

The recommended configurations for interfacing a CML input signal to the Si533x are shown in Figure 9. The 100 Ω resistor provides line termination, and, since the receiver is internally-biased, no additional external biasing components are required.

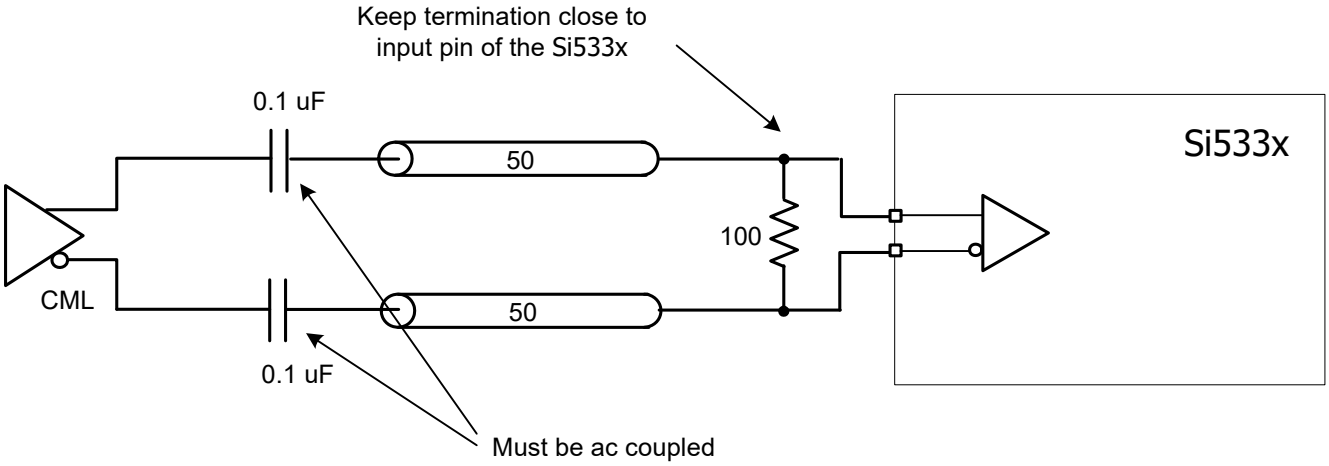


Figure 9. CML Input Signal

2.2.4. Applying CMOS Level Signal to Differential Inputs

Note that the maximum voltage level on the differential input pins on all Si533x must not exceed 1.3 V. To apply a CMOS signal to any of these pins, use the circuit shown in Figure 10. For a CMOS signal applied to these differential inputs, the maximum recommended frequency is 200 MHz.

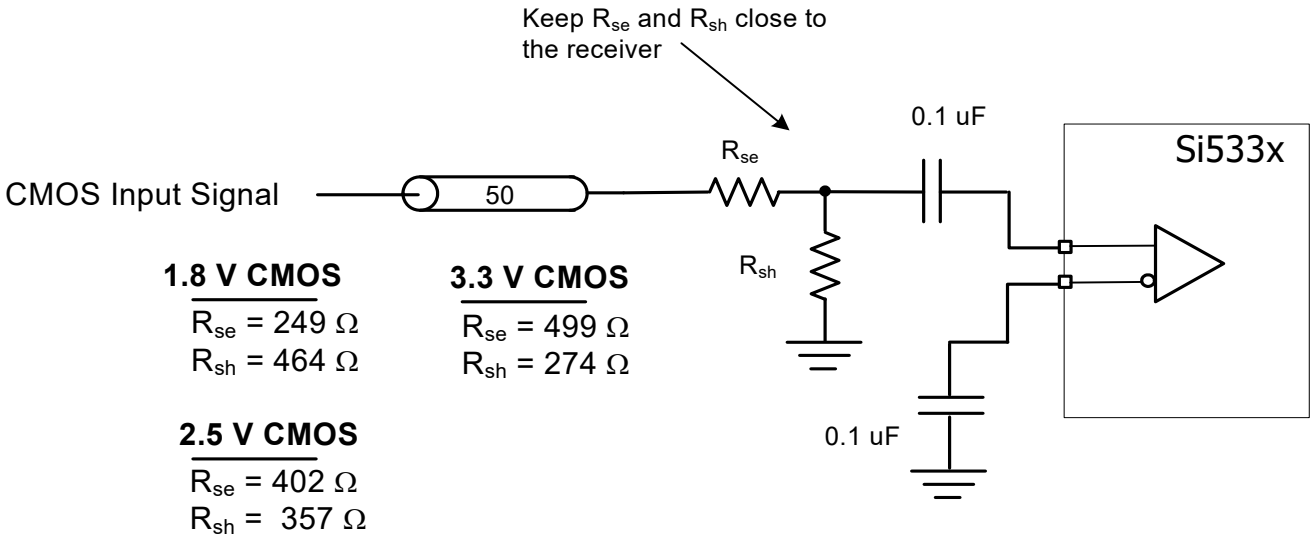


Figure 10. Applying a CMOS Level Signal to the Differential Inputs

2.2.5. HCSL Inputs

A typical HCSL driver has an open source output, which requires an external series resistor and a resistor to ground. The values of these resistors depend on the driver but are typically equal to 33 Ω (Rs) and 50 Ω (Rt). Note that the HCSL driver in the Si533x requires neither Rs nor Rt resistors. Other than two ac-coupling capacitors, no additional external components are necessary when interfacing an HCSL signal to the Si533x.

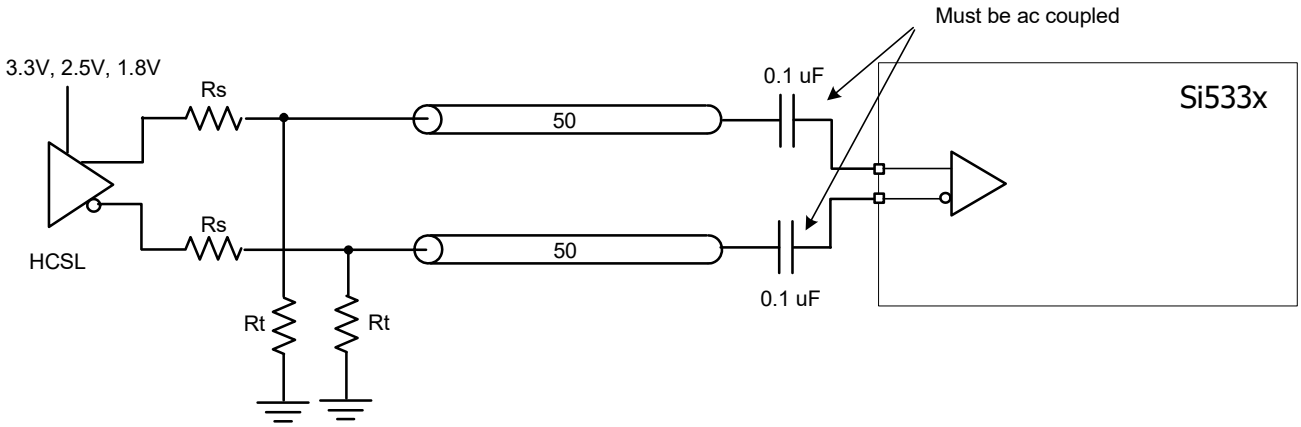


Figure 11. HCSL Input Signal to Si533x

3. Outputs

The Si533x devices provide four outputs that can be differential or single-ended. The Si5356/55 devices only have CMOS outputs. When configured as single-ended, the driver generates two signals that can be configured as in-phase or complimentary. Each of the outputs has its own output supply pin, allowing the device to be used in mixed supply applications without the need for external level translators. Each output driver is configurable to support the following signal types: CMOS/LVTTL, SSTL, HSTL, LVPECL, LVDS, and HCSL. The Si5338 also supports a CML output driver.

3.1. CMOS/LVTTL Outputs

The CMOS output driver has a controlled impedance of about 50 Ω, which includes an internal series resistor of approximately 22 Ω. For this reason, an external Rs series resistor is not recommended when driving 50 Ω traces. If the trace impedance is higher than 50 Ω, a series resistor, Rs, should be used. A typical configuration is shown in Figure 12. By default, the CMOS outputs of the driver are in-phase and can be used to drive two receivers. They can also be configured as complimentary outputs. The output supports 3.3, 2.5, and 1.8 V CMOS signal levels when the appropriate voltage is supplied to the external VDDO pin and the device is configured accordingly.

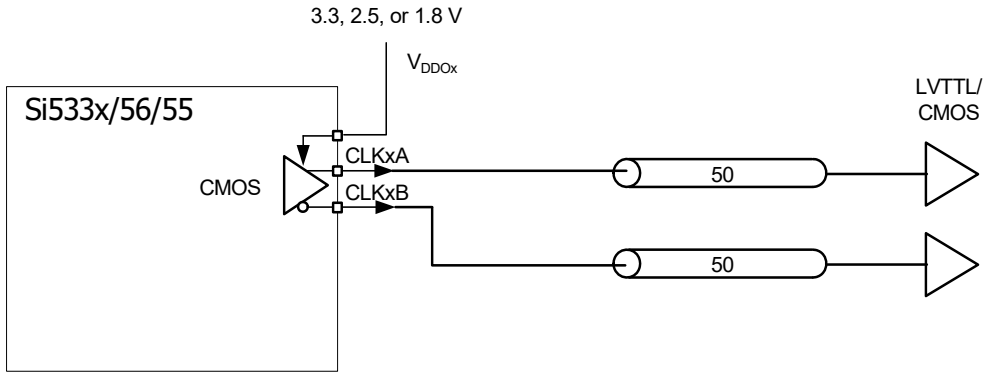


Figure 12. Interfacing to a CMOS Receiver

3.1.1. 1.5 and 1.2 V CMOS Outputs

The Si533x/55/56 output drivers natively support 3.3, 2.5, and 1.8 V CMOS. However, 1.5 and 1.2 V CMOS signals can be obtained using a two-resistor network as shown in Figure 13 and Table 1 below. Place R1 and R2 as close to the device output as possible.

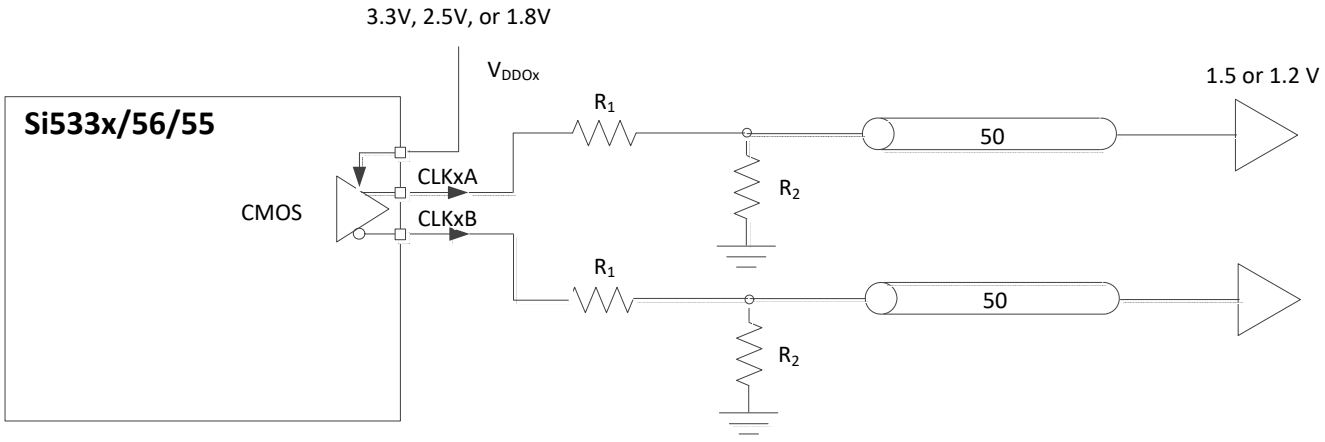


Figure 13. Interfacing to a 1.5 or 1.2 V CMOS Receiver

Table 1. Resistor Values for Interfacing to 1.5 and 1.2 V Receivers

	1.2 V CMOS Output		1.5 V CMOS Output	
VDDOx	**R1**	**R2**	**R1**	**R2**
1.8 V	25 Ω	150 Ω	10 Ω	300 Ω
2.5 V	55 Ω	100 Ω	33 Ω	125 Ω
3.3 V	90 Ω	80 Ω	60 Ω	90 Ω

The resistor values in Table 1 were selected to maintain signal integrity, specifically rise/fall time, at the cost of current consumption. The increase in current consumption is expected to be on the order of 2 to 8 mA per output depending on VDDOx, 4 mA max with VDDOx of 1.8 V.

3.2. SSTL and HSTL Outputs

The Si533x supports both SSTL and HSTL outputs, which can be single-ended or differential. The recommended termination scheme for SSTL is shown in Figure 14. The V_{TT} supply can be generated using a simple voltage divider as shown below.

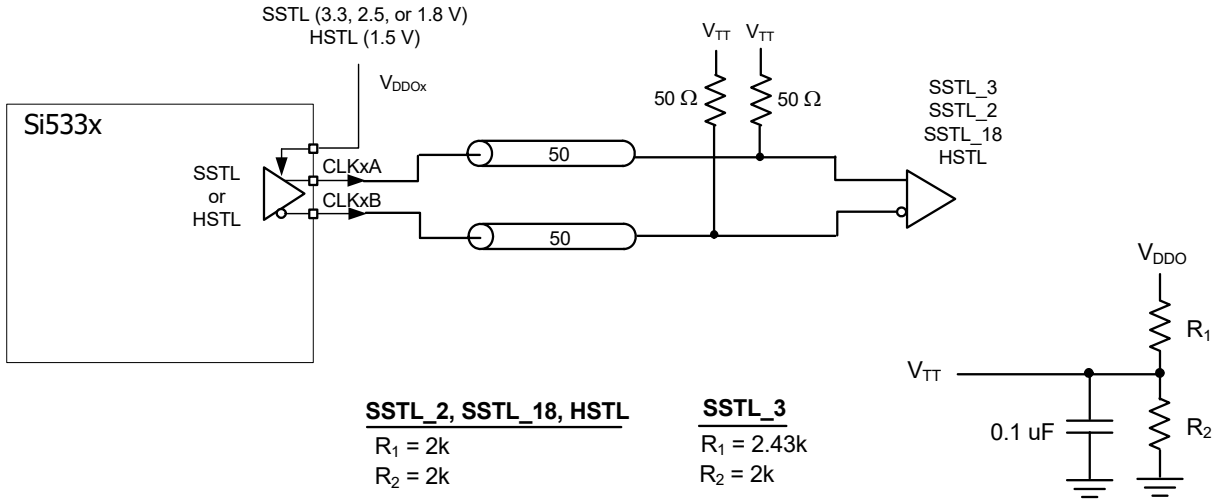


Figure 14. Interfacing the Si533x to an SSTL or HSTL Receiver

3.3. LVPECL Outputs

The LVPECL driver is configurable in both 3.3 V or 2.5 V standard LVPECL modes. The output driver can be ac-coupled or dc-coupled to the receiver.

3.3.1. DC-Coupled LVPECL Outputs

The standard LVPECL driver supports two commonly used dc-coupled configurations. Both of these are shown in Figure 15. LVPECL drivers were designed to be terminated with 50 Ω to VDD–2 V, which is illustrated in Figure 15a. V_{TT} can be supplied with a simple voltage divider as shown in Figure 15.

An alternative method of terminating LVPECL is shown in Figure 15b, which is the Thevenin equivalent to the termination in Figure 15a. It provides a 50 Ω load terminated to V_{DD}–2.0 V. For 3.3 V LVPECL, use R_1 = 127 Ω and R_2 = 82.5 Ω; for 2.5 V LVPECL, use R_1 = 250 Ω and R_2 = 62.5 Ω. The only disadvantage to this type of termination is that the Thevenin circuit consumes additional power from the V_{DDO} supply.

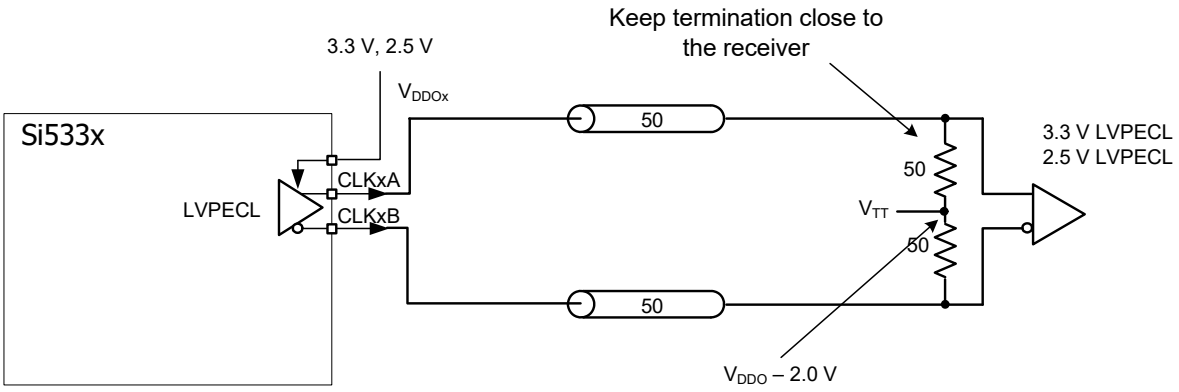


Figure 14a—DC Coupled Termination of 50 Ohms to V_{DD} – 2.0 V

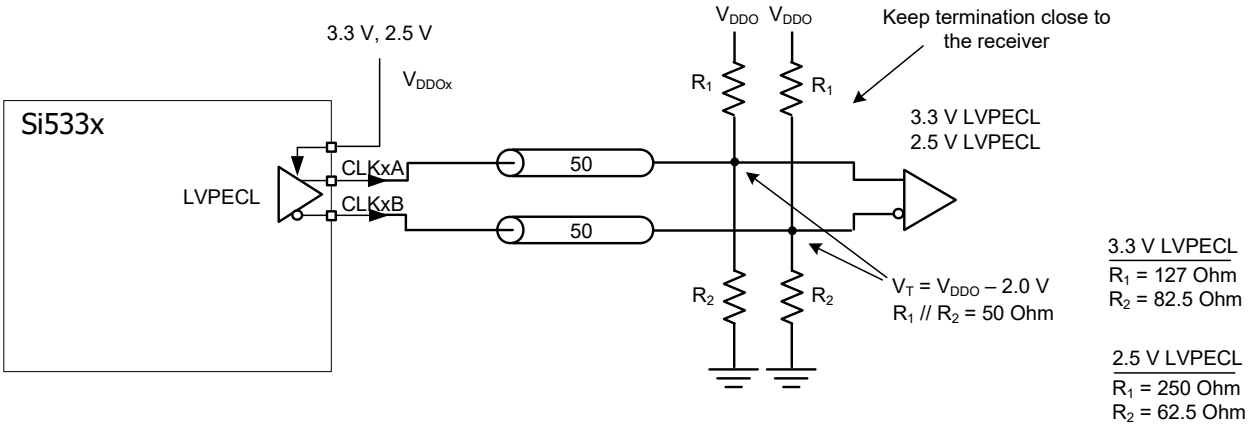


Figure 14b—DC Coupled with Thevenin Termination

Figure 15. Interfacing the Si533x to an LVPECL Receiver Using DC Coupling

3.3.2. AC Coupled LVPECL Outputs

AC coupling is necessary when a receiver and a driver have compatible voltage swings but different common-mode voltages. AC coupling works well for dc-balanced signals, such as for 50% duty cycle clocks. Figure 16 describes two methods for ac coupling the standard LVPECL driver. The Thevenin termination shown in Figure 16a is a convenient and common approach when a V_{BB} (V_{DD} – 1.3 V) supply is not available; however, it does consume additional power. The termination method shown in Figure 16b consumes less power. A V_{BB} supply can be generated from a simple voltage divider circuit as shown in Figure 16.

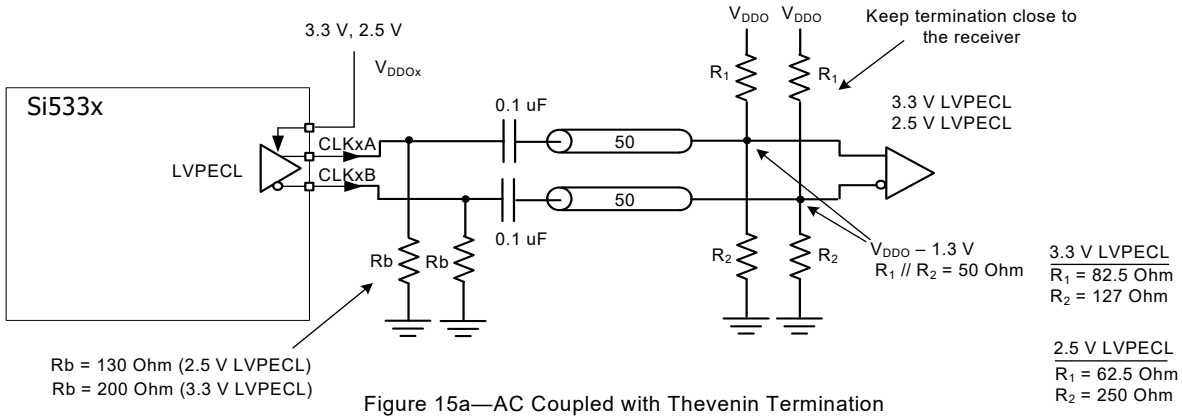


Figure 15a—AC Coupled with Thevenin Termination

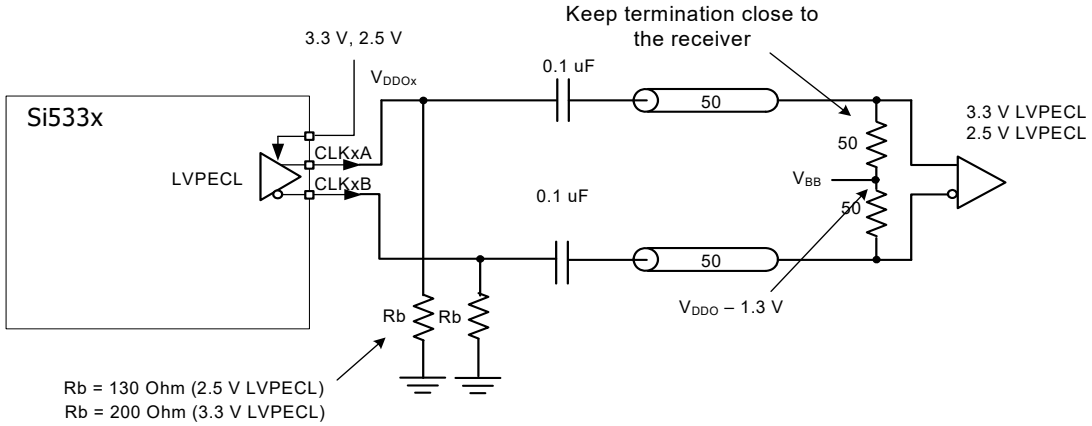


Figure 15b—AC Coupled with 100 Ohm Termination

Figure 16. Interfacing to an LVPECL Receiver Using AC Coupling

3.4. LVDS Outputs

The LVDS output option provides a very simple and power-efficient interface that requires no external biasing when connected to an LVDS receiver. An ac-coupled LVDS driver is often useful as a CML driver. The LVDS driver may be dc-coupled or ac-coupled to the receiver in 3.3 V or 2.5 V output mode.

3.4.1. AC-Coupled LVDS Outputs

The Si5338/34 LVDS output can drive an ac-coupled load. The Si5330 LVDS output can only drive an ac-coupled load if the input to the Si5330 has a very well-controlled duty cycle like any Skyworks Solutions PLL clock products. The ac coupling capacitors may be placed at either the driver or receiver end, as long as they are placed prior to the 100 Ω termination resistor. Keep the 100 Ω termination resistor as close to the receiver as possible, as shown in Figure 17. When a 1.8 V output supply voltage is used, the LVDS output of the Si533x produces a common-mode voltage of ~0.875 V, which does not support the LVDS standard. In this case, it is best to ac-couple the output to the load.

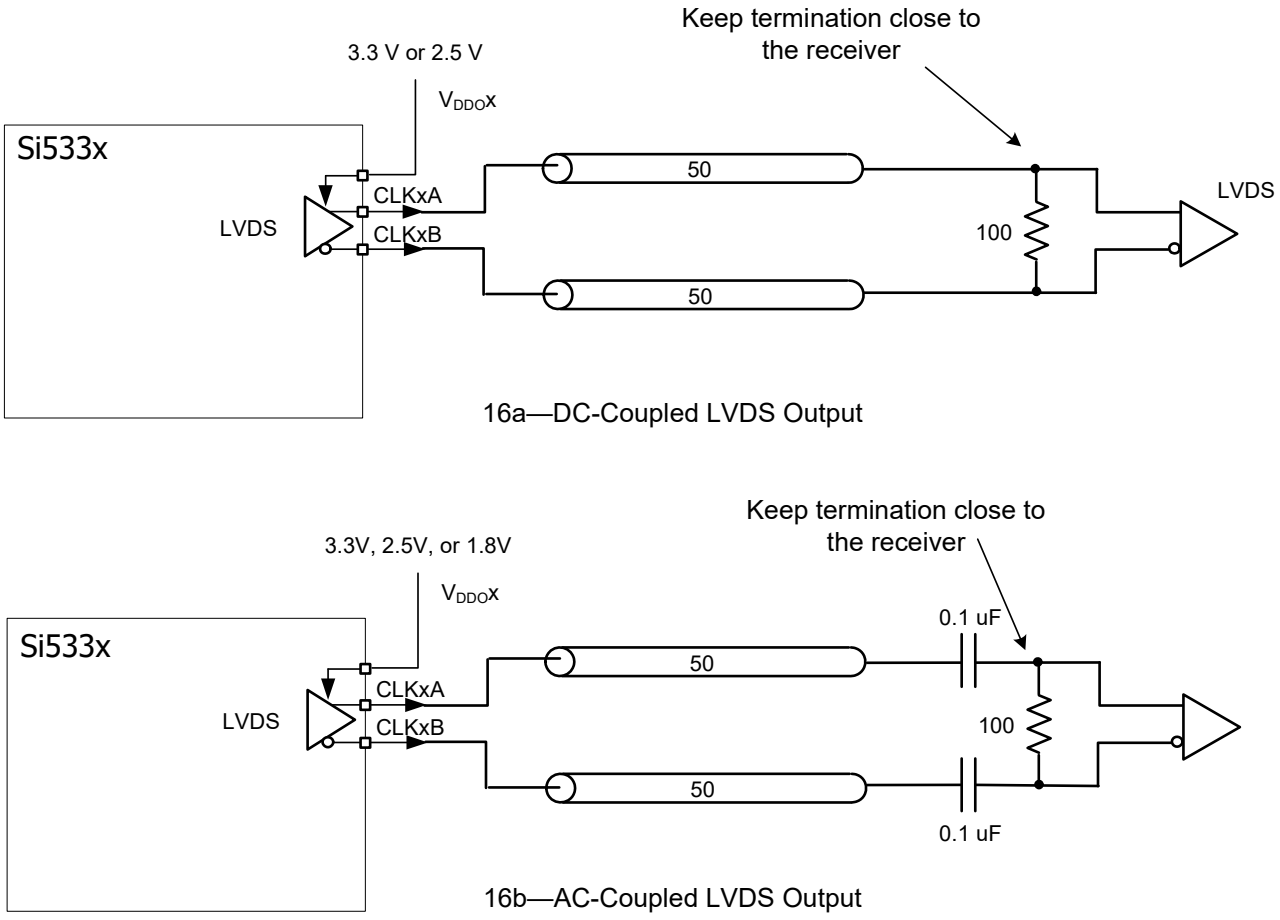


Figure 17. Interfacing to an LVDS Receiver

3.5. HCSL Outputs

Host clock signal level (HCSL) outputs are commonly used in PCI Express applications. A typical HCSL driver has an open source output that requires an external series resistor and a resistor to ground. The Si533x HCSL driver has integrated these resistors to simplify the interface to an HCSL receiver. No external components are necessary when connecting the Si533x HCSL driver to an HCSL receiver.

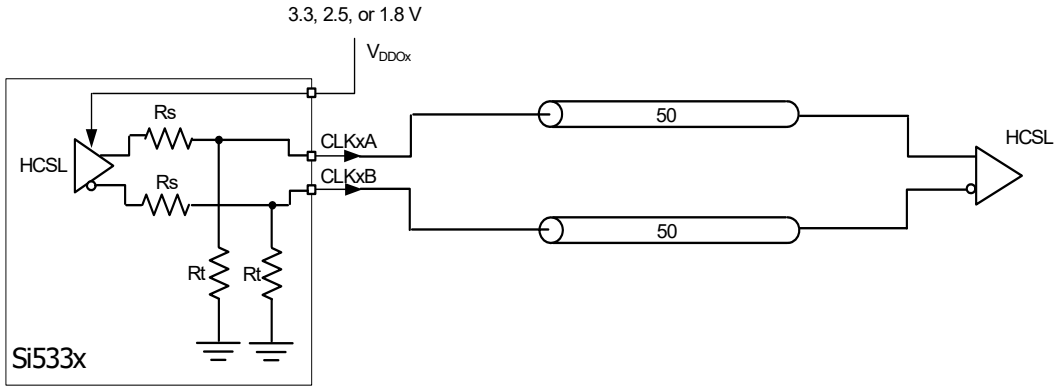


Figure 18. Interfacing the Si533x to an HCSL Receiver

3.6. CML Outputs

The Si5338 has a CML driver option. This driver can be used to replace an LVPECL driver in ac-coupled applications and save ~15 mA for each output driver in the process. When using the CML driver, no external bias resistors from the CML outputs to ground or Vtt should be connected. The CML driver is compliant with LVPECL peak-peak output levels; however, the common-mode output voltage is not compliant to LVPECL specs. The CML driver is individually available for all four differential outputs. See Section 9 of the Si5338 Reference Manual for information on selecting the CML Driver option. The CML output driver option should only be used when the output clock signal comes from an internal MultiSynth.

The Si5338 CML output driver can be used as long as the following conditions are met:

1. Both pins of the differential output pair are ac coupled to the load.
2. The load at the receiver is effectively 100 Ω differential.
3. The Si5338 PLL is not bypassed.
4. The VDDOx supply for the CML driver voltage is 3.3 V or 2.5 V.

The CML driver has the same specified output voltage swing as the LVPECL driver.

1. Max Vsepp = .95 V
2. Min Vsepp = .55 V
3. Typ Vsepp = .8 V

Figure 19 shows the normal connection for the Si5338 CML Driver format. Figure 20 shows the expected termination for the Si5338 CML driver. This termination is most often within a CML receiver.

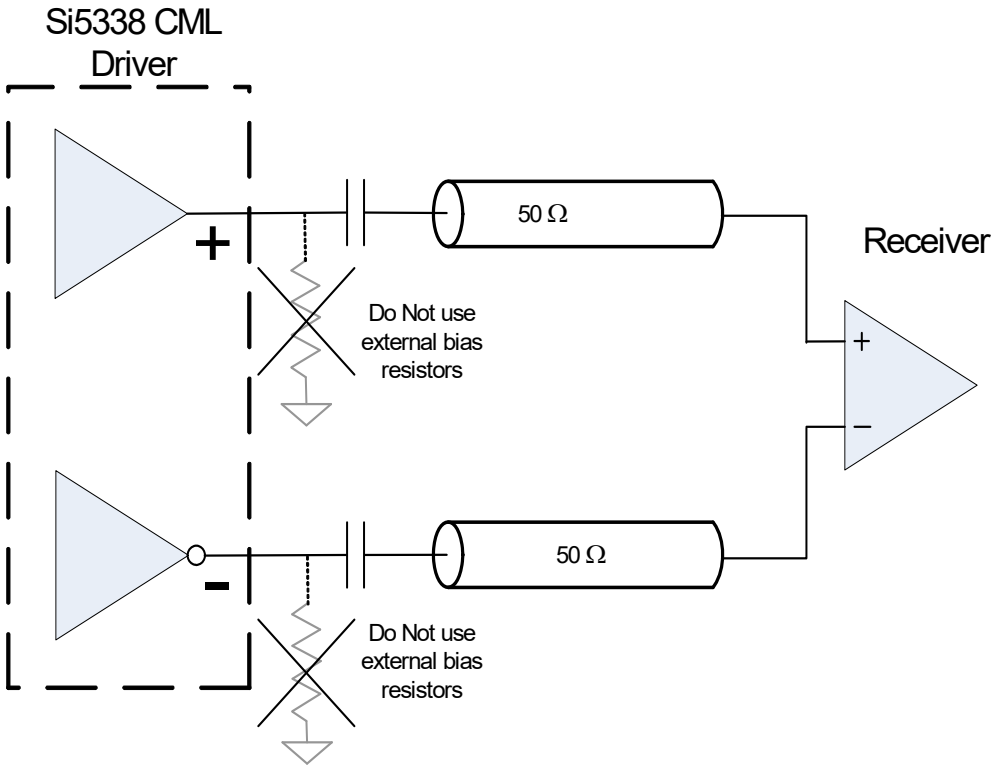


Figure 19. CML Driver Connection

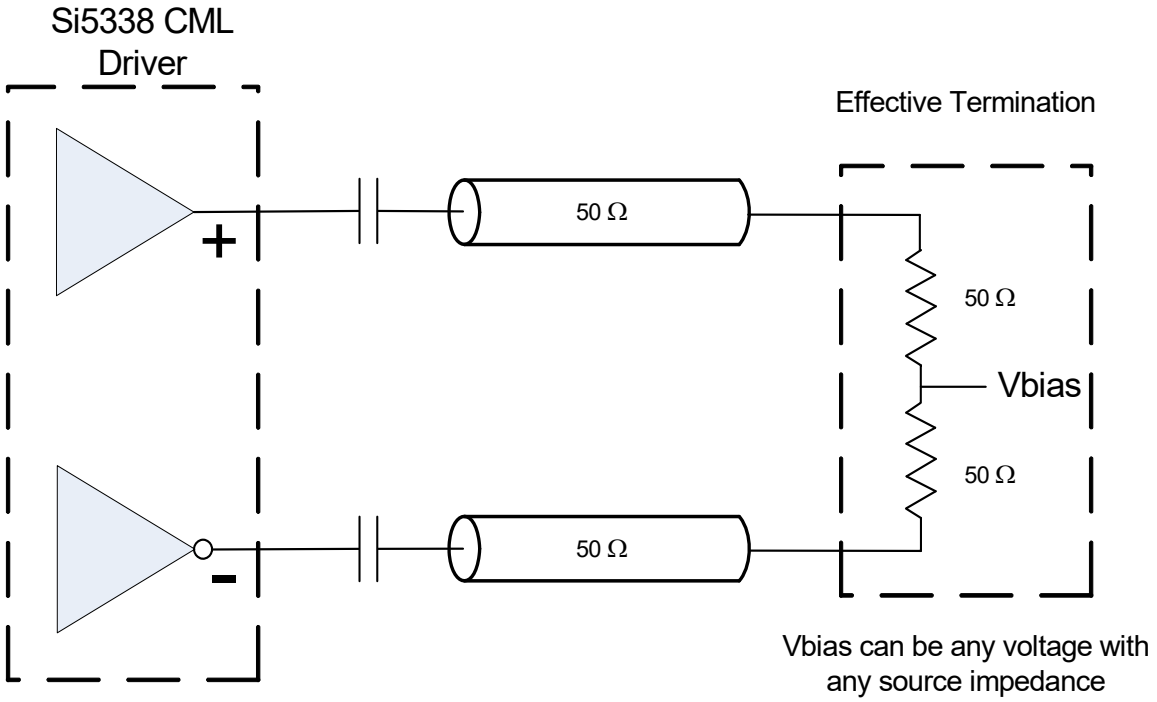
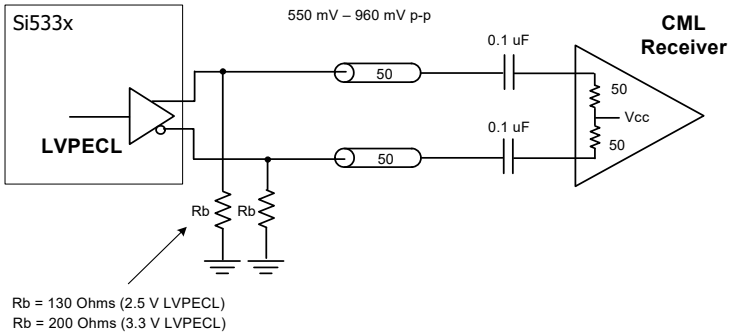


Figure 20. Terminations for Si5338 CML Driver

3.7. Interfacing the Si533x LVDS/LVPECL to a CML Receiver

Current mode logic (CML) is transmitted differentially and terminated to 50 Ω to Vcc as shown in Figure 21. A CML receiver can be driven with either an LVPECL or an LVDS output depending on the signal swing required by the receiver. A single-ended output swing from 550 mV to 960 mV is achieved when driving a CML receiver with an LVPECL output. For a reduced output swing, LVDS mode is recommended for producing a single-ended swing between 250 mV and 450 mV.

Driving a CML Receiver Using the LVPECL Output



Driving a CML Receiver Using the LVDS Output

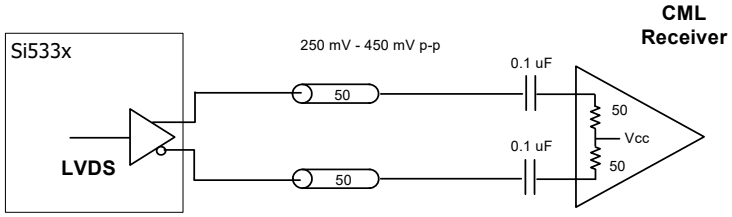


Figure 21. Terminating an LVPECL or an LVDS Output to a CML Receiver

Revision History

Revision 0.6

March, 2020

- Fixed R1 typo in "2.1.2. Single-Ended SSTL and HSTL Inputs" on page 4.
- Updated reference to Si5338 reference manual in "3.6. CML Outputs" on page 15.

Revision 0.5

October, 2013

- Updated Figure 10 on page 8.
  - Updated resistor values.
- Updated "2.2.4. Applying CMOS Level Signal to Differential Inputs" on page 8.
  - Added text to recommend max CMOS input frequency into a differential input.
- Updated "2.1.2. Single-Ended SSTL and HSTL Inputs" on page 4 and "2.1.3. Applying a Single-Ended Signal to a Differential Input" on page 5 to specify a max input frequency of 350 MHz.
- Removed R1 and R2 and 0.1 µf cap from Figures 15 and 16.
- Added maximum input frequency of 350 MHz to "2.1.2. Single-Ended SSTL and HSTL Inputs" on page 4 and "2.1.3. Applying a Single-Ended Signal to a Differential Input" on page 5.
- Added "3.6. CML Outputs" on page 15.
- Added "3.1.1. 1.5 and 1.2 V CMOS Outputs" on page 10.

Revision 0.4

November, 2010

- Updated "3.5. HCSL Outputs" on page 15.

Revision 0.3

July, 2010

- Moved Section “2.2.4 Applying a Single-Ended Signal to a Differential Input” to Section 2.1.3.
- Modified LVPECL circuit in Figure 16.
- Added "2.2.3. CML Inputs" on page 8.
- Added "2.2.4. Applying CMOS Level Signal to Differential Inputs" on page 8.

Revision 0.2

January, 2010

- Added "2.2.2. LVPECL Inputs" on page 5.
- Removed “3.4. Low Power LVPECL Output Driver—AC Coupled”.
- Added "3.7. Interfacing the Si533x LVDS/LVPECL to a CML Receiver" on page 17.

Revision 0.1

October, 2008

- Initial release.

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