

AN1362: Si828x XM3 Gate Driver Test Report

This report documents testing performed at Skyworks with support from Wolfspeed's XM3 module team and provides details on the operation of Skyworks Si828x isolated gate drivers and the Wolfspeed Half-Bridge Silicon Carbide (SiC) Field Effect Transistor (FET) XM3 module. The Si828x's robust short-circuit protection feature and the rugged SiC XM3 module, which enable the system to survive and operate well under extreme short-circuit conditions, are described. This test report also details Si828x-XM3 performance in switching loss, crosstalk, and common-mode immunity (CMTI) tests in a half-bridge configuration.

KEY FEATURES

- Robust short-circuit protection and common-mode transient immunity
- High current handling capability and rugged reliability
- Complete modular design in a half-bridge configuration

The test platform consisted of a Skyworks Si828x-AW-GDB half-bridge gate driver evaluation board (Daughter Card) and a Wolfspeed CIL XM3 Evaluation Board (Motherboard). The XM3 SiC FET module was mounted under Wolfspeed's XM3 Motherboard. The XM3 Motherboard has holes that lined up with the XM3 module's terminals and allowed the Skyworks Si828x-AW-GDB board on top to be plugged directly into the XM3 module on the bottom. This design provided optimum interconnection between the Si828x gate drivers and the XM3 module to minimize parasitic inductance in the gate driver circuits.

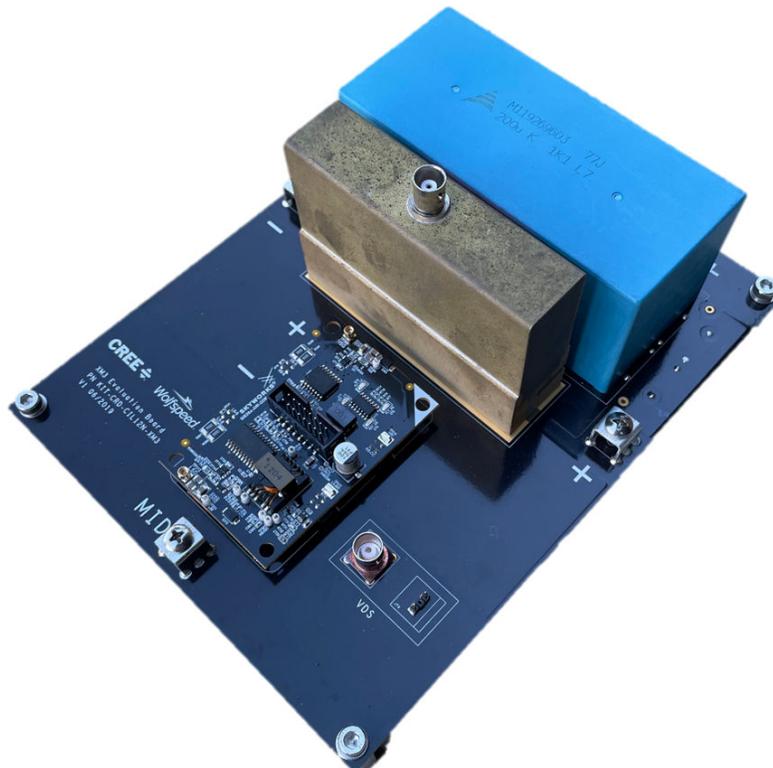


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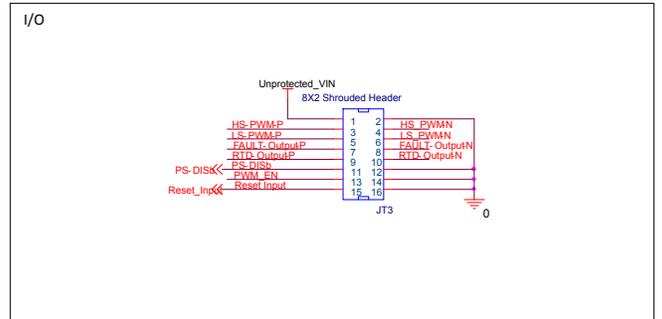
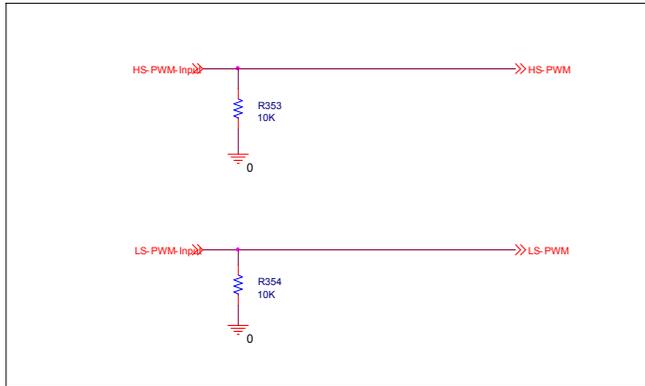
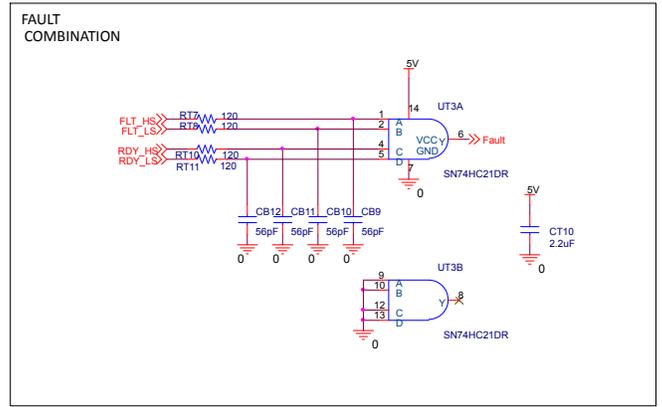
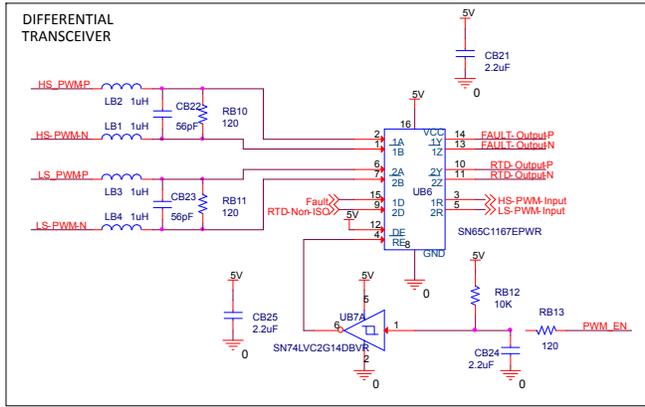


Figure 1.2. Low-Voltage Signals and I/O

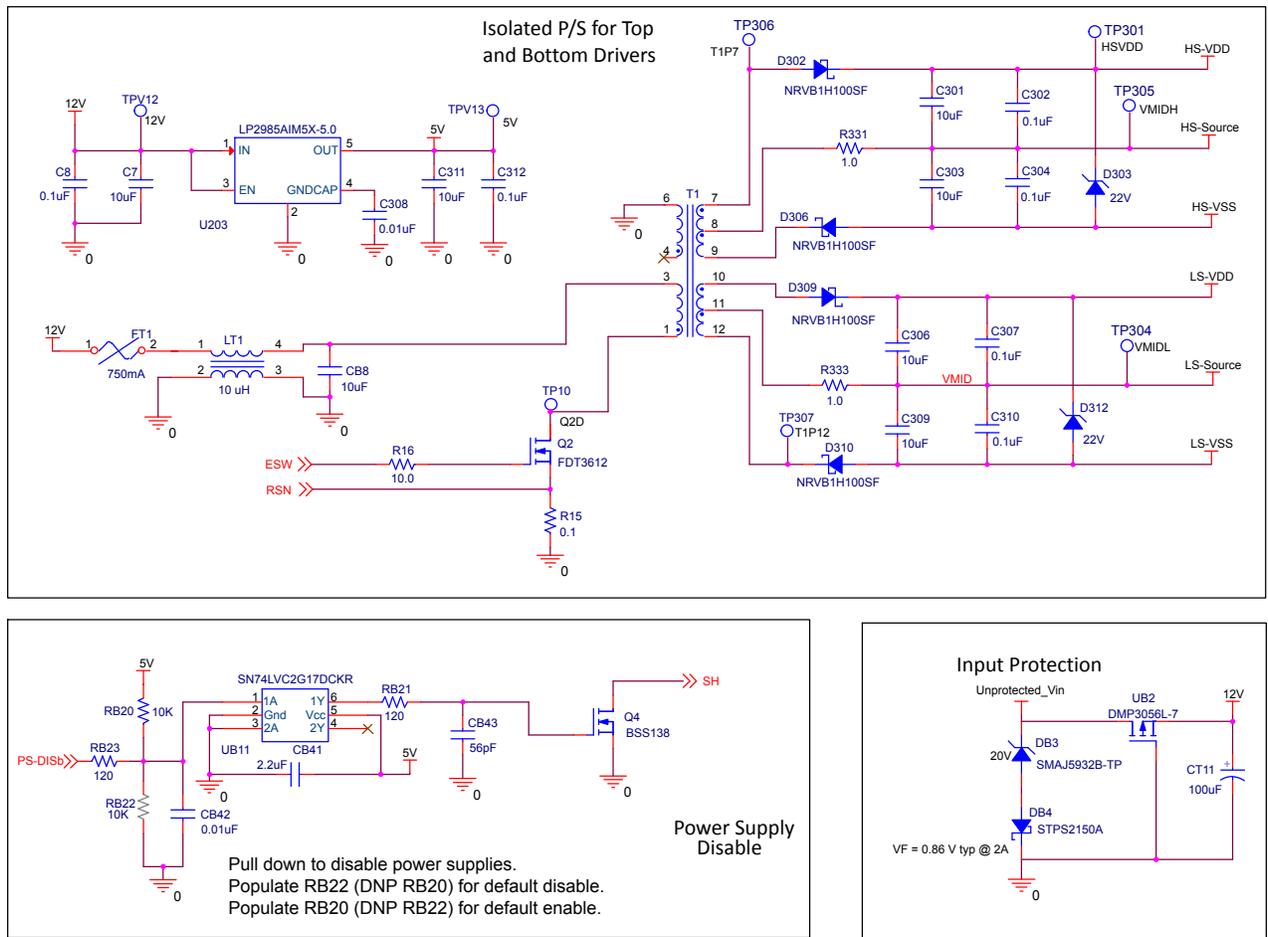
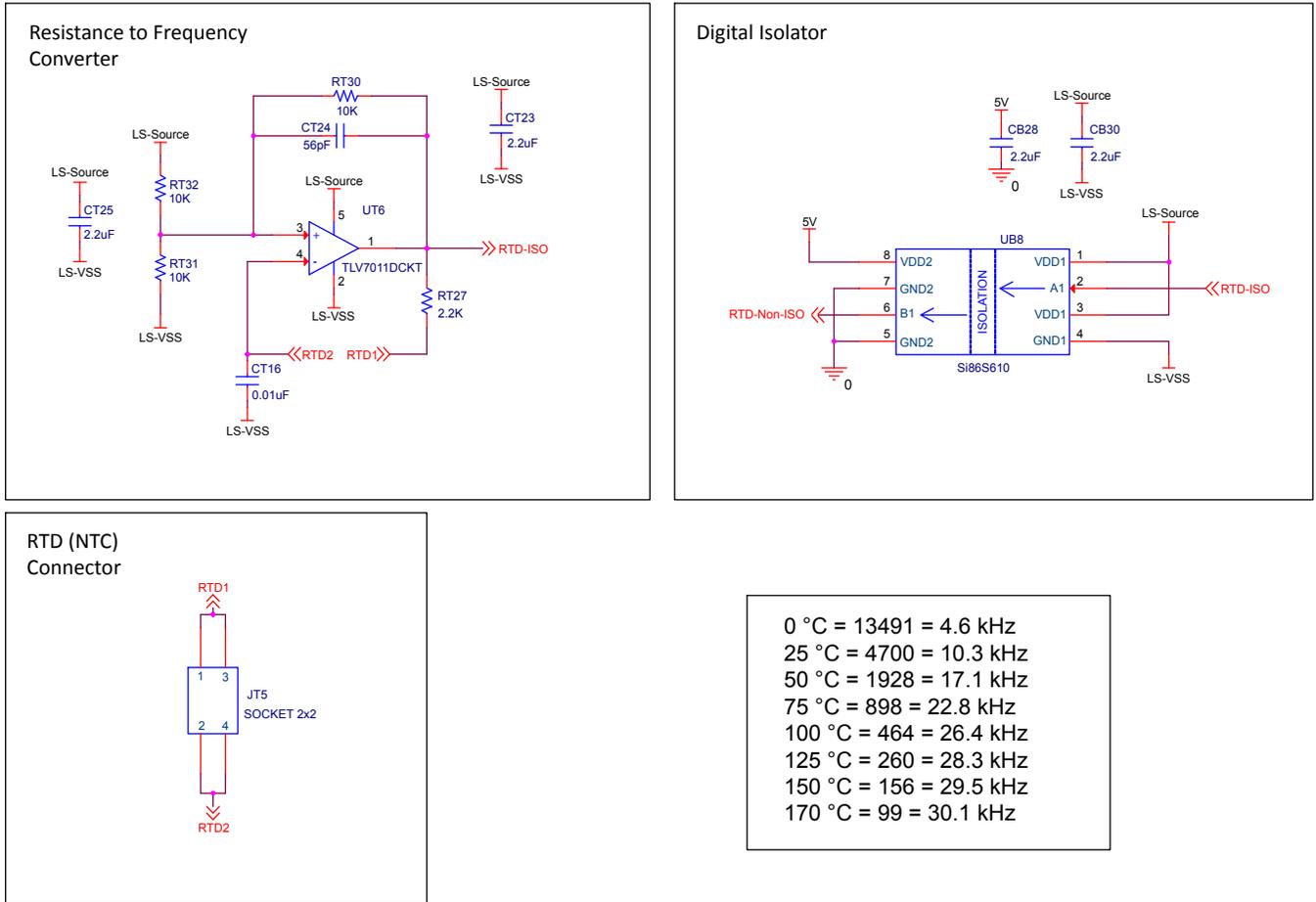


Figure 1.3. Power Supplies and Input Protection



0 °C	= 13491	= 4.6 kHz
25 °C	= 4700	= 10.3 kHz
50 °C	= 1928	= 17.1 kHz
75 °C	= 898	= 22.8 kHz
100 °C	= 464	= 26.4 kHz
125 °C	= 260	= 28.3 kHz
150 °C	= 156	= 29.5 kHz
170 °C	= 99	= 30.1 kHz

Figure 1.4. NTC Resistance to Frequency Converter

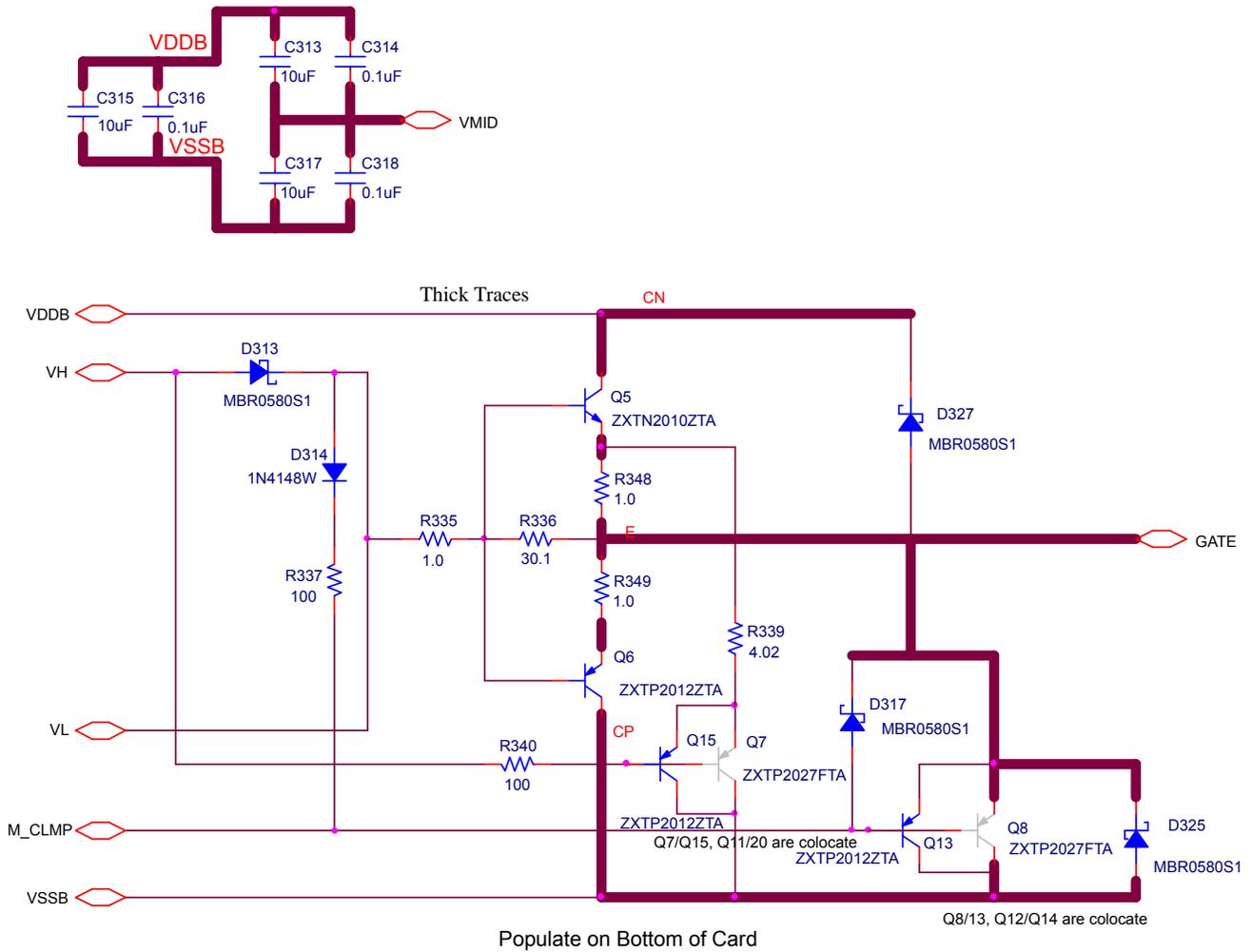


Figure 1.5. High-Side Current Booster Circuit

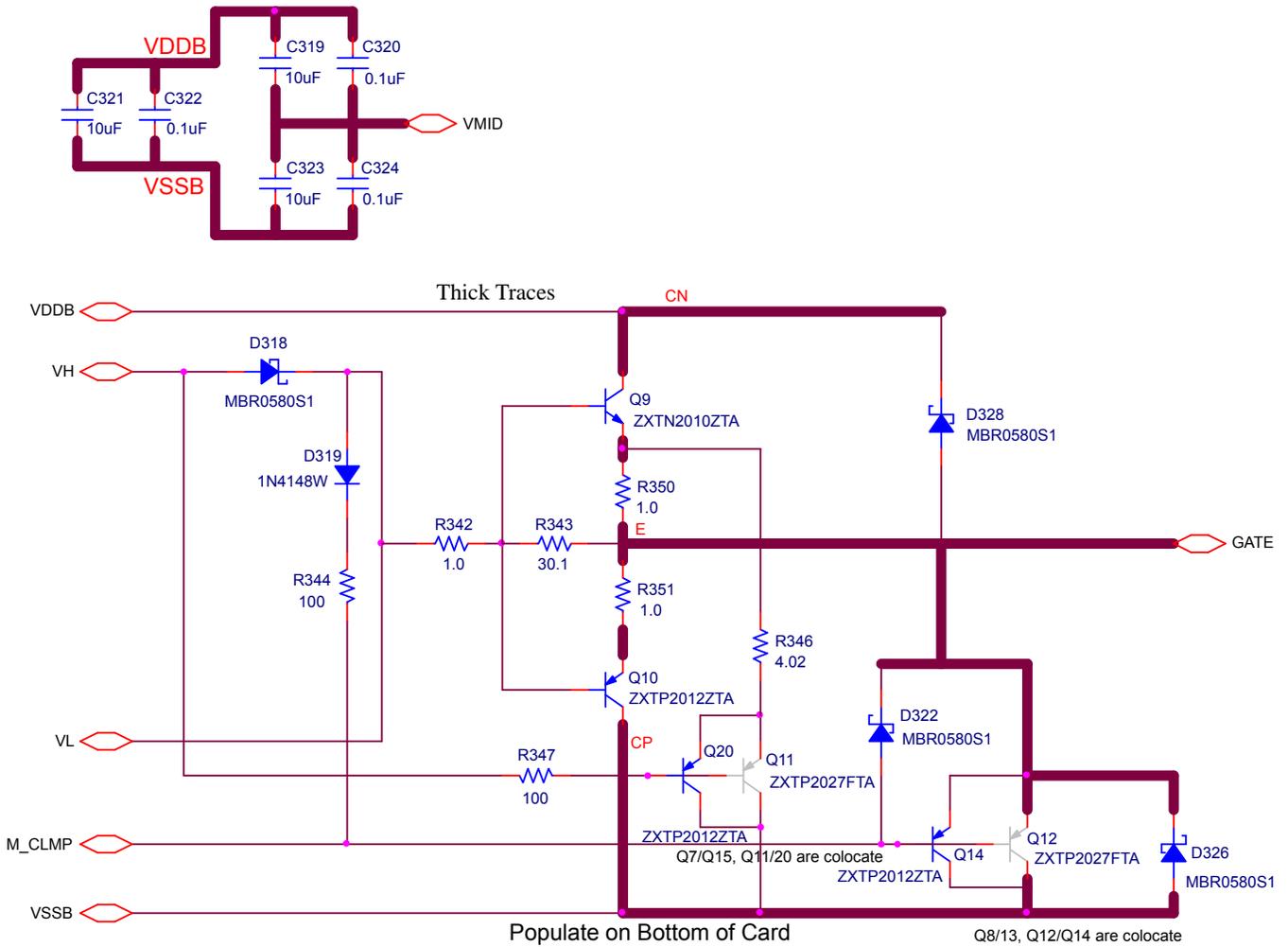


Figure 1.6. Low-Side Current Booster Circuit

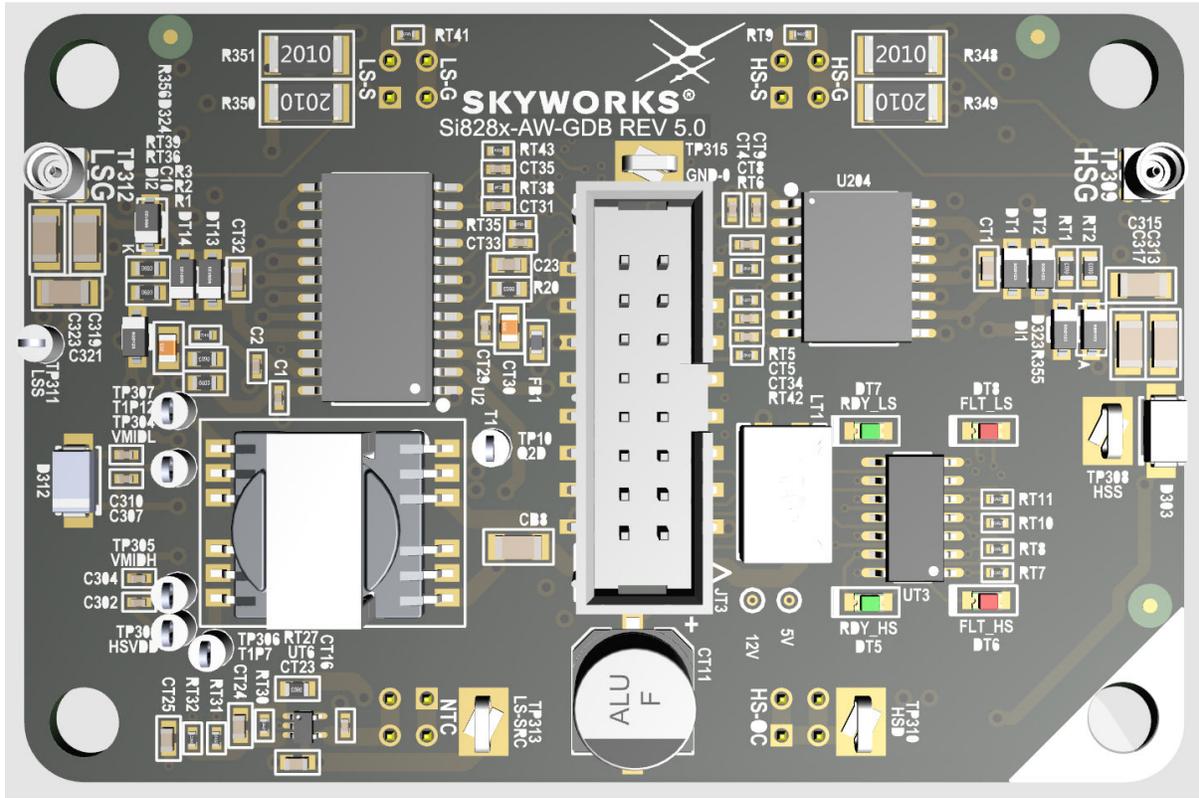


Figure 1.7. Si828x-AW-GDB Evaluation Board

For more information on the Si828x's advanced gate drive capabilities, see "[AN1288: Si828x External Enhancement Circuits](#)".

1.2 XM3 Module

Wolfspeed's CAB450M12XM3 half-bridge SiC module was evaluated in this test and exhibited the following electrical rating: $R_{ds-on} = 2.6 \text{ m}\Omega$ (typical); $V_{DS} = 1.2 \text{ kV}$, and $I_{DS} = 450 \text{ A}$. For more details about this module, go to the Wolfspeed XM3 Half-Bridge Power Module Family web page at <https://www.wolfspeed.com/xm3-power-module-family/>.



Figure 1.8. Wolfspeed's CAB450M12XM3 Half-Bridge SiC Module

1.3 Wolfspeeds CIL XM3 Evaluation Board Motherboard

The figure below shows a simplified schematic of Wolfspeed's [KIT-CRD-CIL12N-XM3](#) evaluation board. The board's layout is optimized for low parasitic inductance (Figure 8) with minimum interconnect trace distances between the bulk capacitors, the high-frequency bypass capacitors, and the high bandwidth current measurement via current viewing resistor (CVR). Finally, the board has a Kelvin high-frequency V_{DS} voltage measurement point BCN connector to simplify the V_{DS} oscilloscope probe connection and connection points for the inductor, L_O .

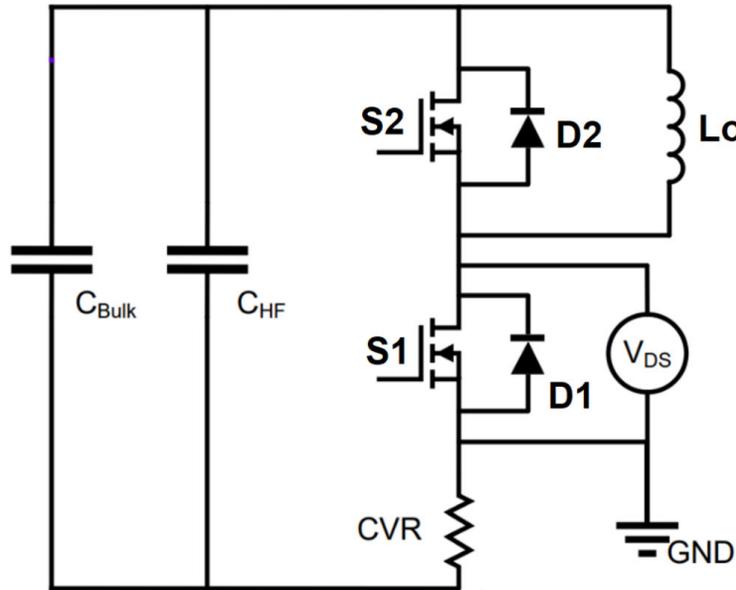


Figure 1.9. Wolfspeed's KIT-CRD-CIL12N-XM3 Simplified Schematic

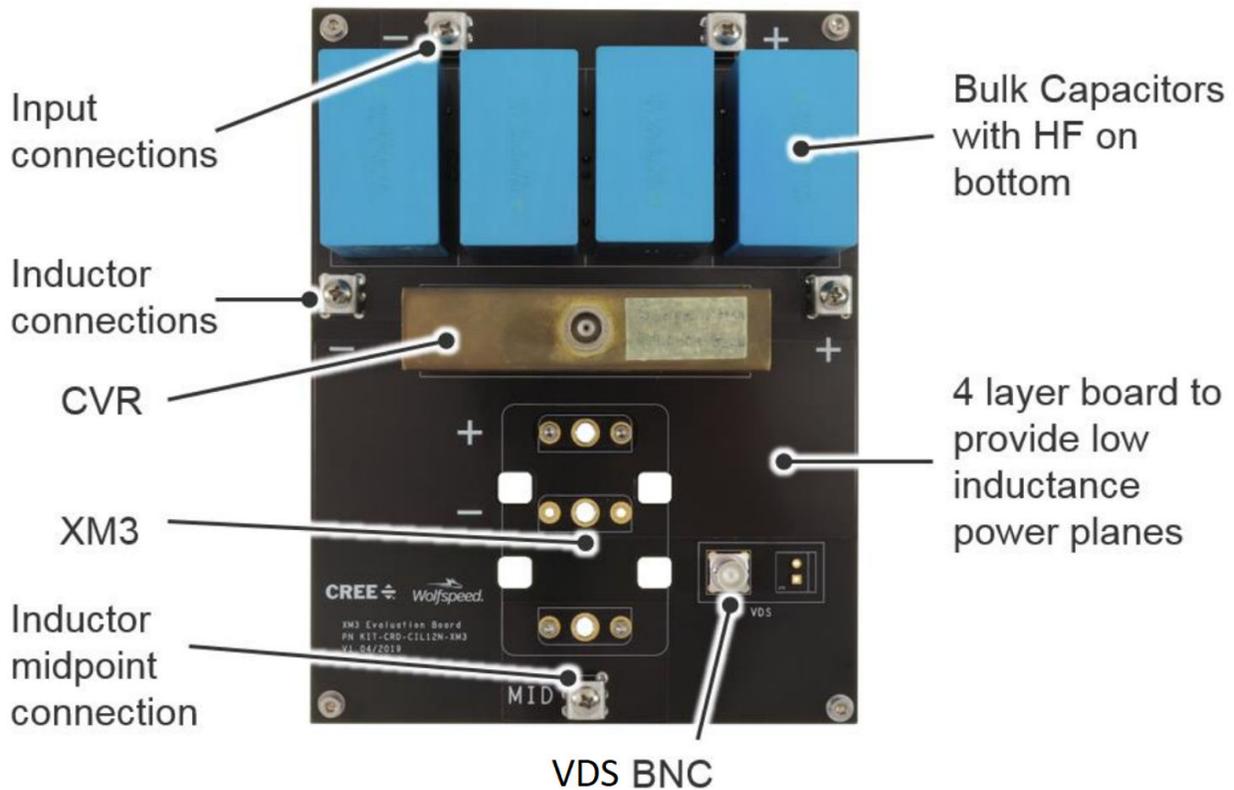


Figure 1.10. Wolfspeed's KIT-CRD-CIL12N-XM3 CIL Evaluation Board

For more information on Wolfspeed's KIT-CRD-CIL12N-XM3 CIL Evaluation Board and the test apparatus, see the [CIL CPWR-AN31 User Guide](#).

2. Short Circuit Testing

Short circuit testing was performed by creating a low-impedance connection across the low-side XM3 half-bridge SiC FET module, as shown in the figures below. This simulated a washer short condition, in which a piece of electrically conducting wire or a washer falls between the V⁻ and VMID terminals of the XM3 module. A physical washer short across the high-side SiC (V⁺ to MID terminals) is not feasible due to the XM3's terminal arrangement; therefore, testing on the high-side short condition was not conducted.

2.1 Test Setup

Due to the XM3's sizable gate charge characteristics, the Si828x circuits have some external components to increase the current drive and provide control to the XM3 SiC FET gates. Below are short descriptions of the external components:

1. Q1 and Q2: Increase current drive
2. RI: sets DESAT detection timing
3. RSS: set soft shutdown timing
4. RH: sets turn-on switching speed
5. RL: set turn-off switching speed

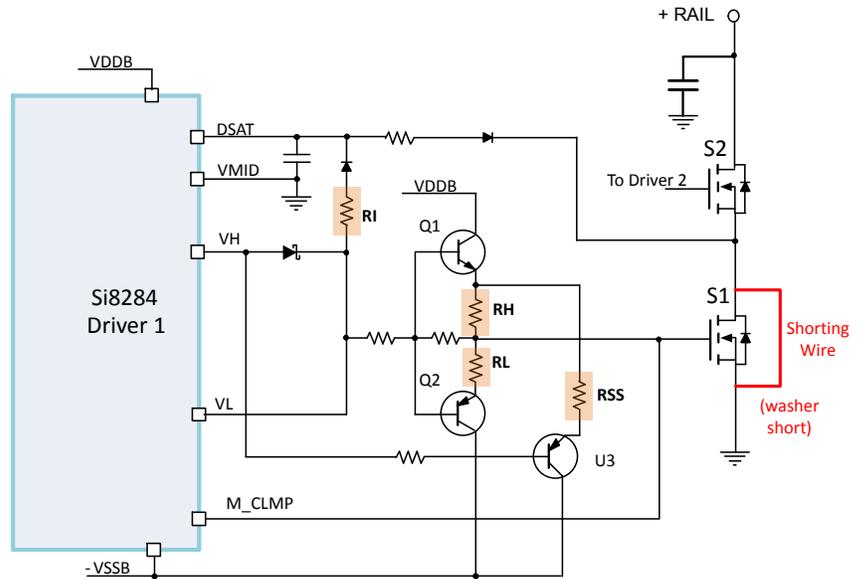


Figure 2.1. Simplified Schematic of the Driver Circuit and a Shorted Upper SiC MOSFET

Cooper bus short across the low-side XM3 half-bridge SiC FET module (Half-Bridge - to MID terminals)



Figure 2.2. Low-Side Short Circuit Setup with Large Copper Bus Bar

The Si828x gate driver circuits can be tuned to provide robust protection against short-circuit conditions. The tuning process requires selecting the component described in the simplified driver circuit schematic above to achieve a DESAT response time of less than 1 μ s (from the time the I_{DS} current goes above 0 A and back to 0 A) while ensuring that the I_{DS} peak current and the V_{DS} voltage spike levels stay below the XM3's rating. This tuning process is documented in [AN1288: Si828x External Enhancement Circuits](#).

2.2 Short Circuit Test Results

Table 2.1 DESAT Test Results on page 13 and the following scope plots summarize three data points for consideration. Notice from the data in the table that the values of RI control the Si828x detection time directly. Additionally, since the I_{DS} peak current is directly proportional to the detection time, I_{DS} peak current is also affected by the value of RI. The RSS value controls the SSD duration (Soft Shutdown duration) and the V_{DS} voltage spike. The RSS value has some effect on the I_{DS} peak current as well.

Due to the optimized layout of the KIT-CRD-CIL12N-XM3 CIL evaluation board plus the XM3 module's internal low parasitic inductance, the V_{DS} voltage spike is insignificant in all tests cases. This low-voltage spike allows short circuit tests at 1 kV dc rail. Bear in mind that application circuits with larger parasitic inductance induce higher voltage spikes; therefore, larger RSS or reduced operating dc rail may be required to ensure that the V_{DS} voltage spike is kept below the XM3 voltage rating.

Si828x DESAT performance for all test cases summarized in the table below demonstrates that the Si828x protected the XM3 well. For slightly lower power dissipation (larger RSS value), the Skyworks Si828x-AW-GDB evaluation boards are built with the component values listed in Figure 2.5 Si828x 625 ns DESAT response time with $R_I = 2.2\text{ k}\Omega$, $R_H = R_L = 1\ \Omega$, $R_{SS} = 4.02\ \Omega$ on page 15.

Table 2.1. DESAT Test Results

Figure #	RT36/ R_I	R346/ R_{SS}	R350/ R_H	R351/ R_L	Response	Detection	SSD	+ DC Rail	V_{DS} Spike	I_{DS} Peak
2.3	3.3 k Ω	4.02	1	1	800 ns	320 ns	800 ns	1000 V	1040 V	900 A
2.4	2.2 k Ω	1	1	1	560 ns	280 ns	600 ns	1000 V	1075 V	650 A
2.5	2.2 k Ω	4.02	1	1	625 ns	280 ns	800 ns	1000 V	1040 V </tr	

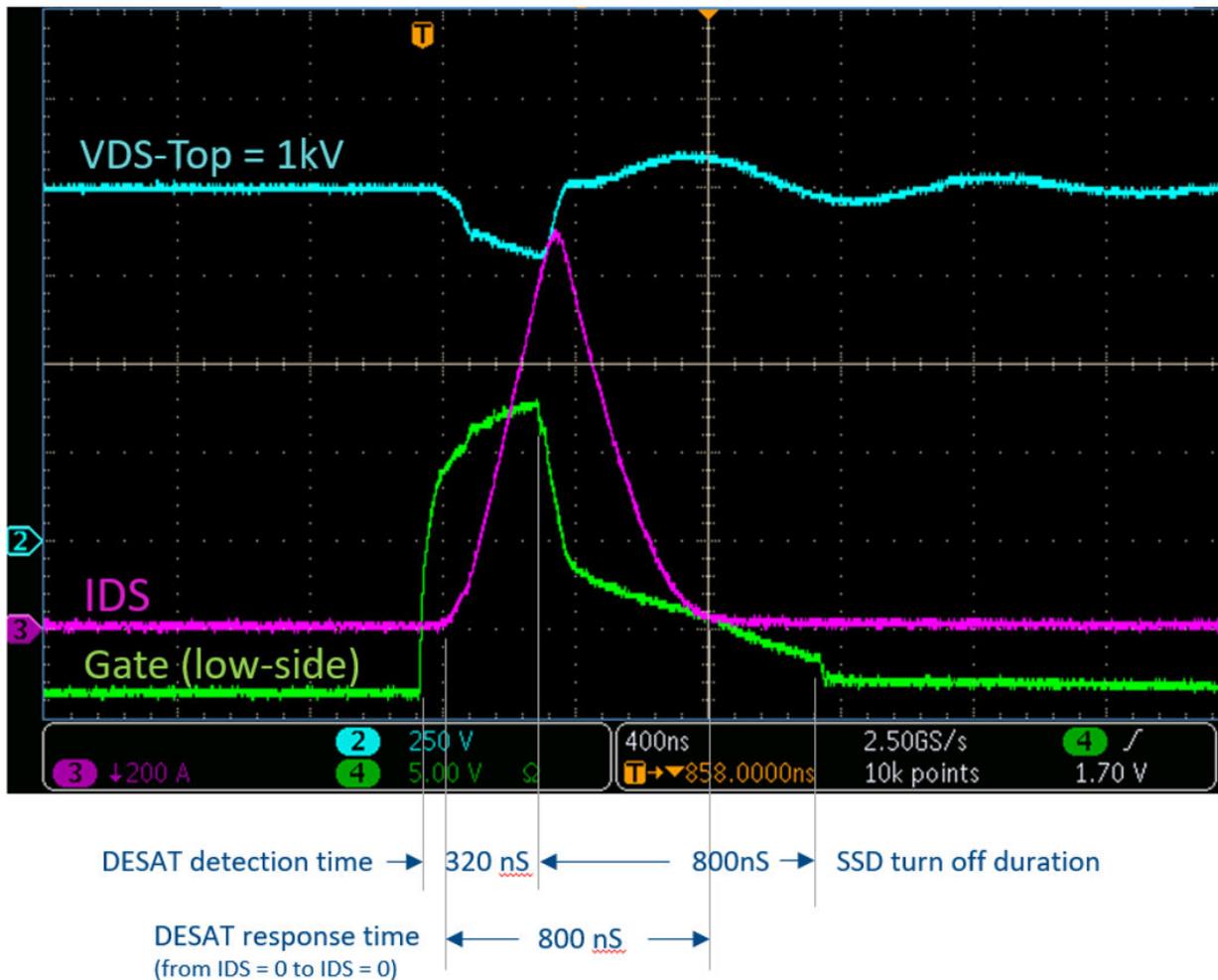
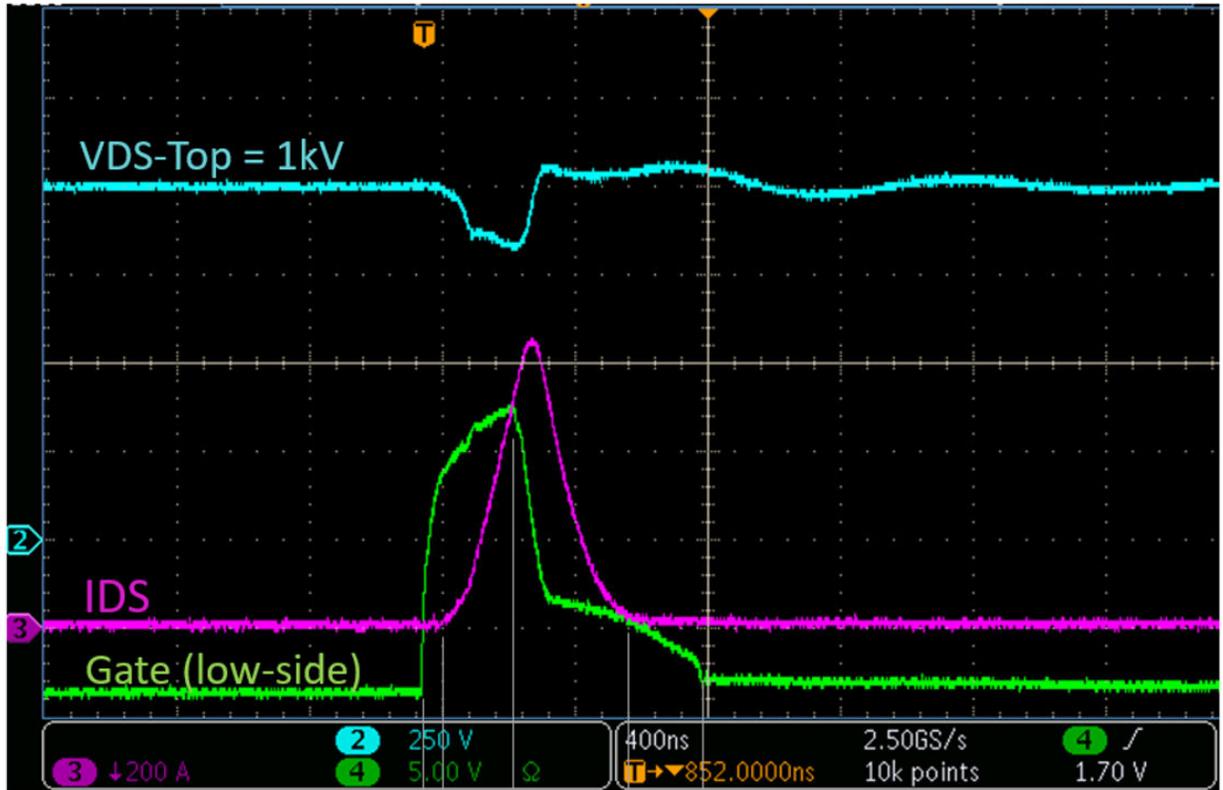


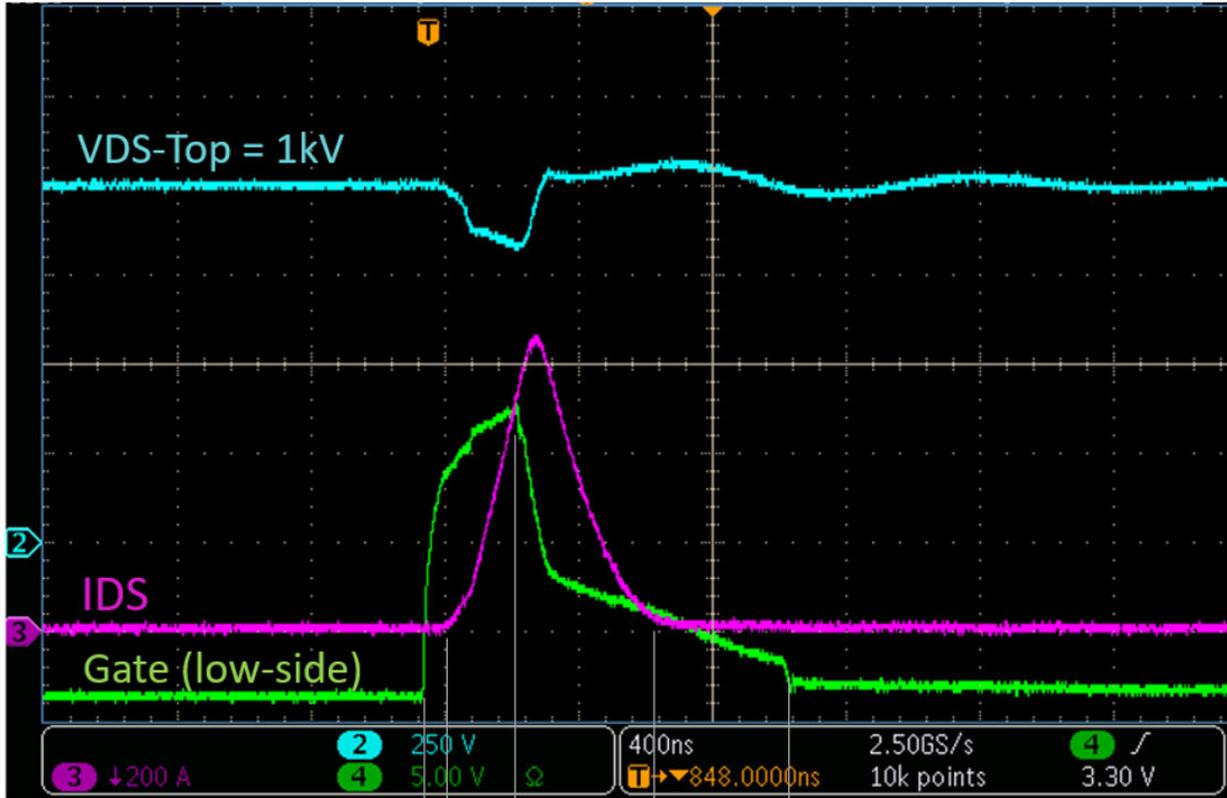
Figure 2.3. Si828x 800 ns DESAT response time with $R_I = 3.3\text{ k}\Omega$, $R_H = R_L = 1\ \Omega$, $R_{SS} = 4.02\ \Omega$



DESAT detection time → 280ns ← 600ns → SSD turn off duration

DESAT response time ← 560ns →
(from IDS = 0 to IDS = 0)

Figure 2.4. Si828x 560 ns DESAT response time with $R_I = 2.2 \text{ k}\Omega$, $R_H = R_L = 1 \text{ }\Omega$, $R_{SS} = 1 \text{ }\Omega$



DESAT detection time → 280ns ← 800ns → SSD turn off duration

DESAT response time ← 625ns →
 (from IDS = 0 to IDS = 0)

Figure 2.5. Si828x 625 ns DESAT response time with $R_I = 2.2 \text{ k}\Omega$, $R_H = R_L = 1 \text{ }\Omega$, $R_{SS} = 4.02 \text{ }\Omega$

3. Crosstalk

In the XM3 half-bridge power circuit shown in the figure below, the S1 and S2 switching devices are stacked in series and connected to the high-voltage V_{dc} . In this configuration, there must be only one switching device in the On state at any point in time. If both S1 and S2 are on simultaneously, substantial current flow from V_{dc} through S1 and S2 can cause excessive power loss and possible damage to the S1 and S2 (a condition known as current shoot-through). The PWM signals that drive the gates of S1 and S2 are conditioned to absolutely avoid turning on both S1 and S2 at the same time. However, during S2 high-speed turn-on (S1 is turning off), the voltage at the MID terminal is rapidly going toward V_{dc} + (large dv/dt) and induces Miller current flow through the gate of S1, across R_L and generates a positive voltage at the gate of S1. Depending on the dv/dt level and the total impedance in series with R_L , the Miller voltage spike can become larger than the gate threshold voltage (V_{th}), turn on S1 momentarily, and cause shoot-through current across S1 and S2. A similar condition occurs in the opposite switching condition when S1 turns on while S2 turns off and can cause a shoot-through condition as well.

The Si828x gate driver has bipolar power supplies to provide a negative voltage to the gate of S1 or S2 in the Off state to alleviate the effect of the Miller voltage spike. It is essential to validate that the Miller voltage spike at the gate can never go above the XM3 gate threshold voltage.

3.1 Crosstalk Board Setup

The figure below illustrates the crosstalk test circuit. In this test, S1 was held in the Off state while a function generator controlled the gate of S2. The gate voltage of S1 was monitored while S2 was switched. The current in the inductor L_o grew as S2 was pulsed on multiple times and allowed crosstalk testing at the different current levels.

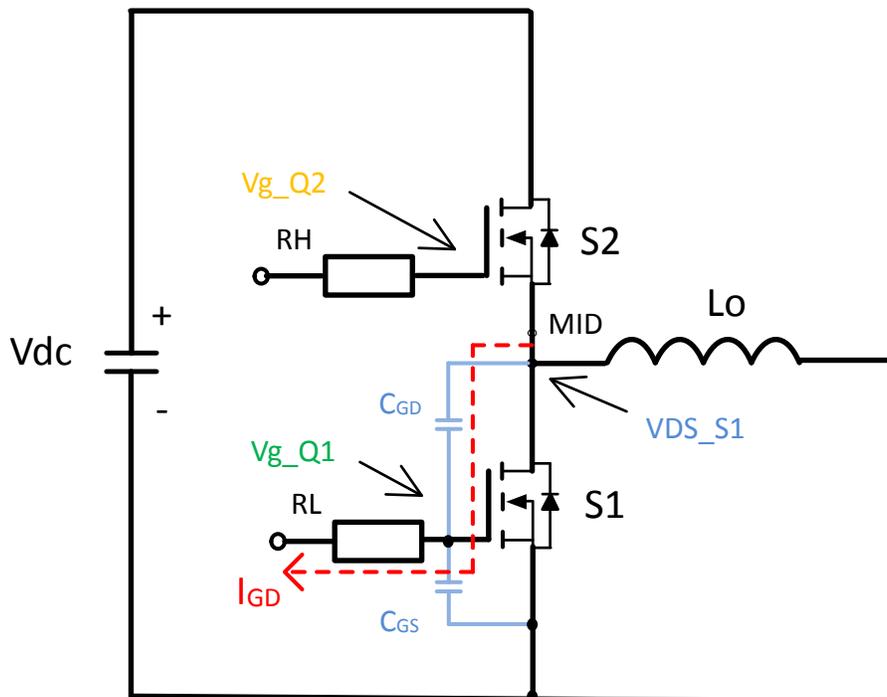


Figure 3.1. Crosstalk Test Circuit

3.2 Crosstalk Test Results

The following scope plots show the behavior of the lower gate S1 as the upper S2 SiC FET is turned on.

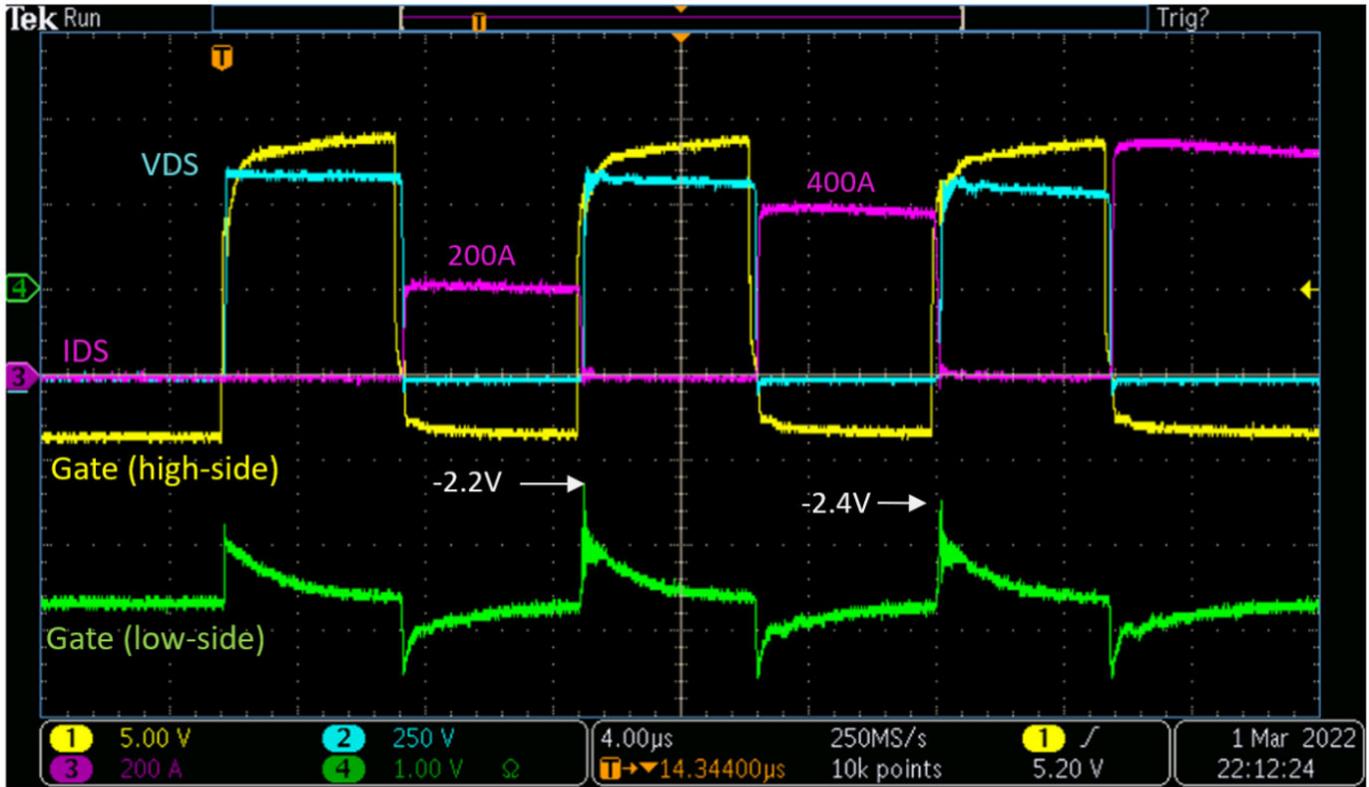


Figure 3.2. Crosstalk Test $R_H = R_L = 1 \Omega$, $V_{DS} = 600 \text{ V}$, $L_o = 14 \mu\text{H}$

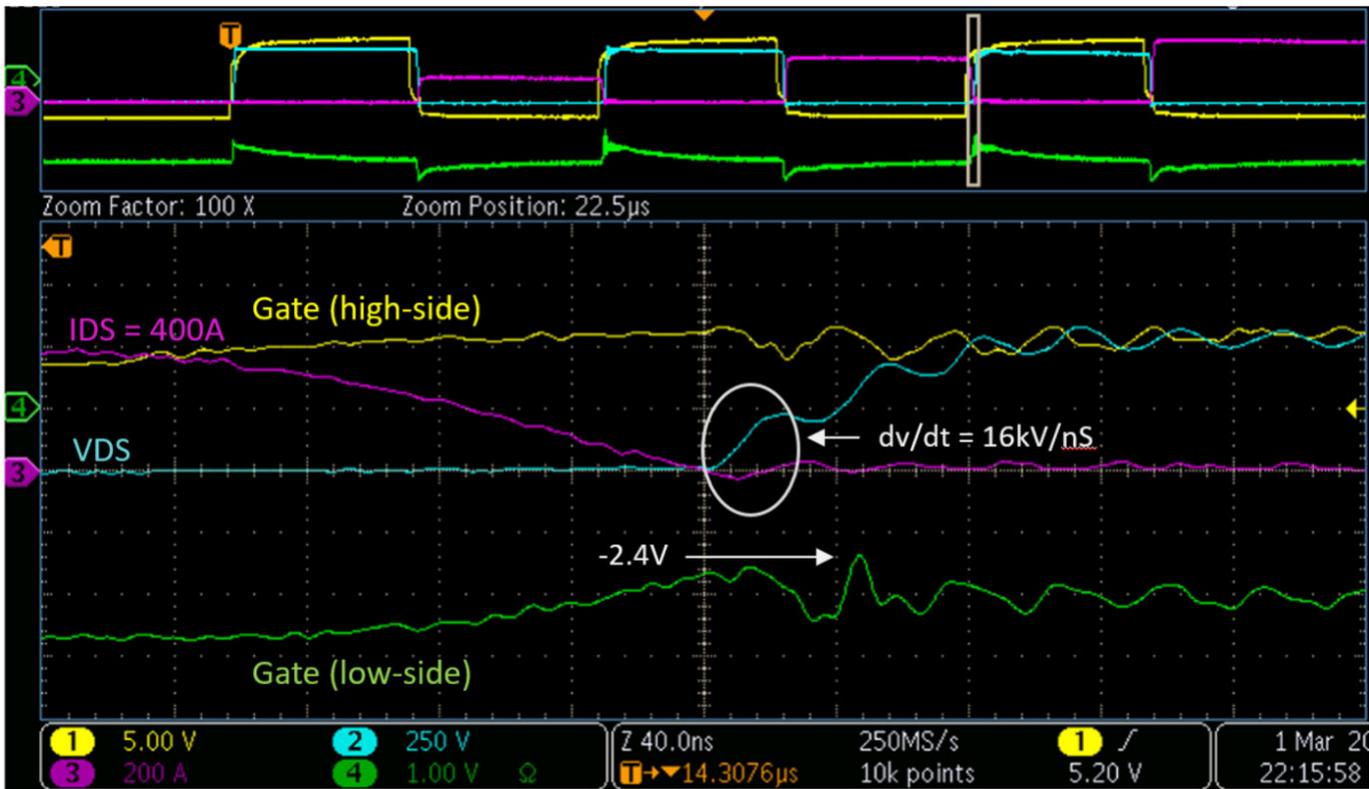


Figure 3.3. Crosstalk Test $R_H = R_L = 1 \Omega$, $V_{DS} = 600 \text{ V}$, $L_o = 14 \mu\text{H}$, $I_{DS} = 400 \text{ A}$ (Zoomed)

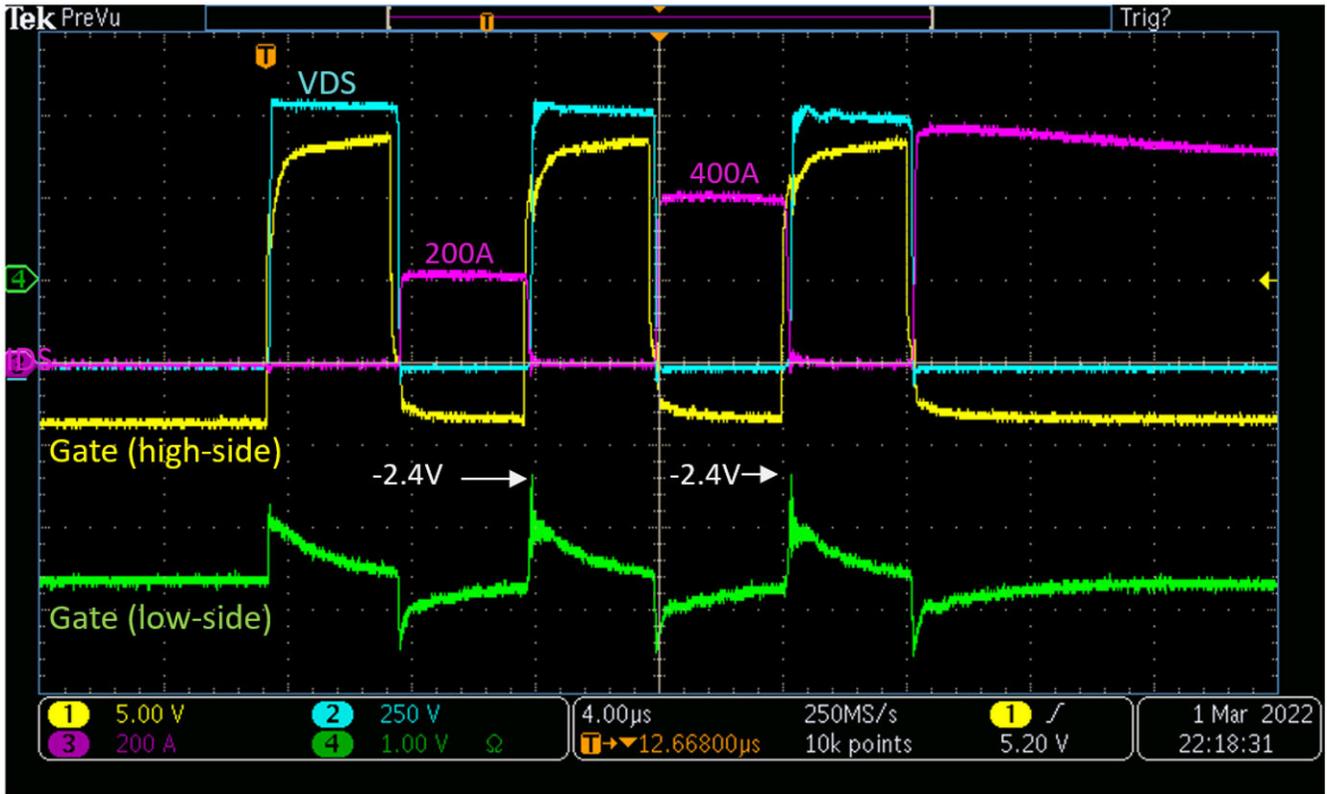


Figure 3.4. Crosstalk Test $R_H = R_L = 1 \Omega$, $V_{DS} = 800 \text{ V}$, $L_o = 14 \mu\text{H}$

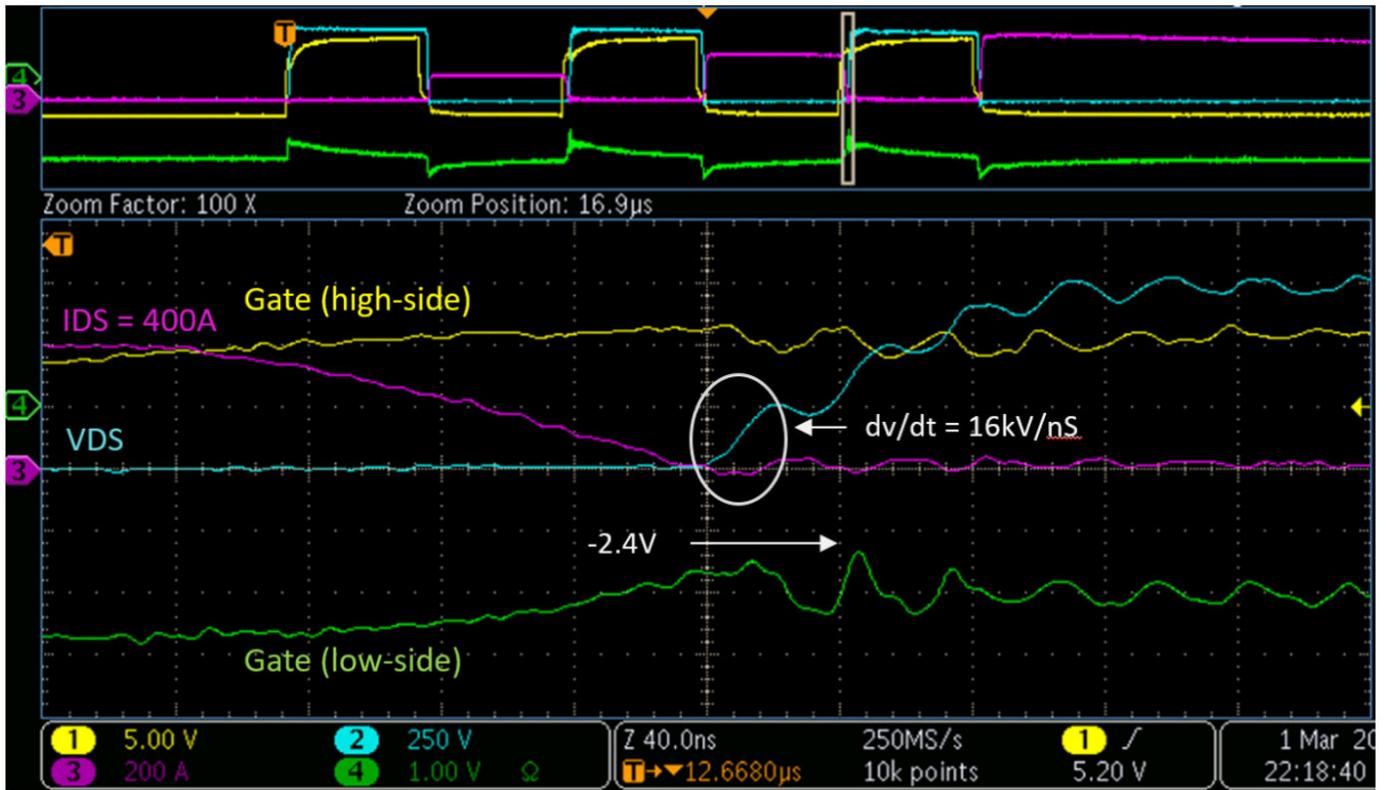


Figure 3.5. Crosstalk Test $R_H = R_L = 1 \Omega$, $V_{DS} = 800 \text{ V}$, $I_{DS} = 400 \text{ A}$, $L_o = 14 \mu\text{H}$ (Zoomed)

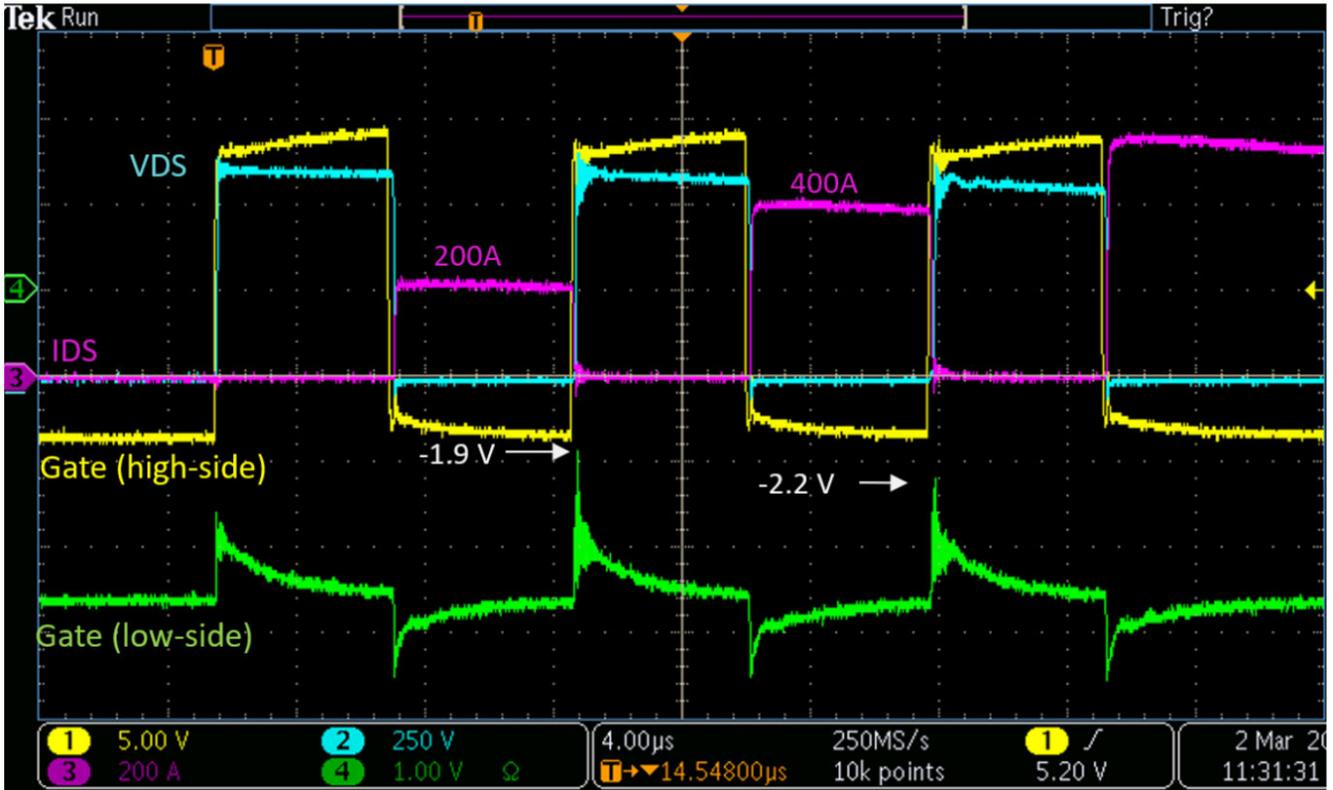


Figure 3.6. Crosstalk Test $R_H = R_L = 0 \Omega$, $V_{DS} = 600 \text{ V}$, $L_o = 14 \mu\text{H}$

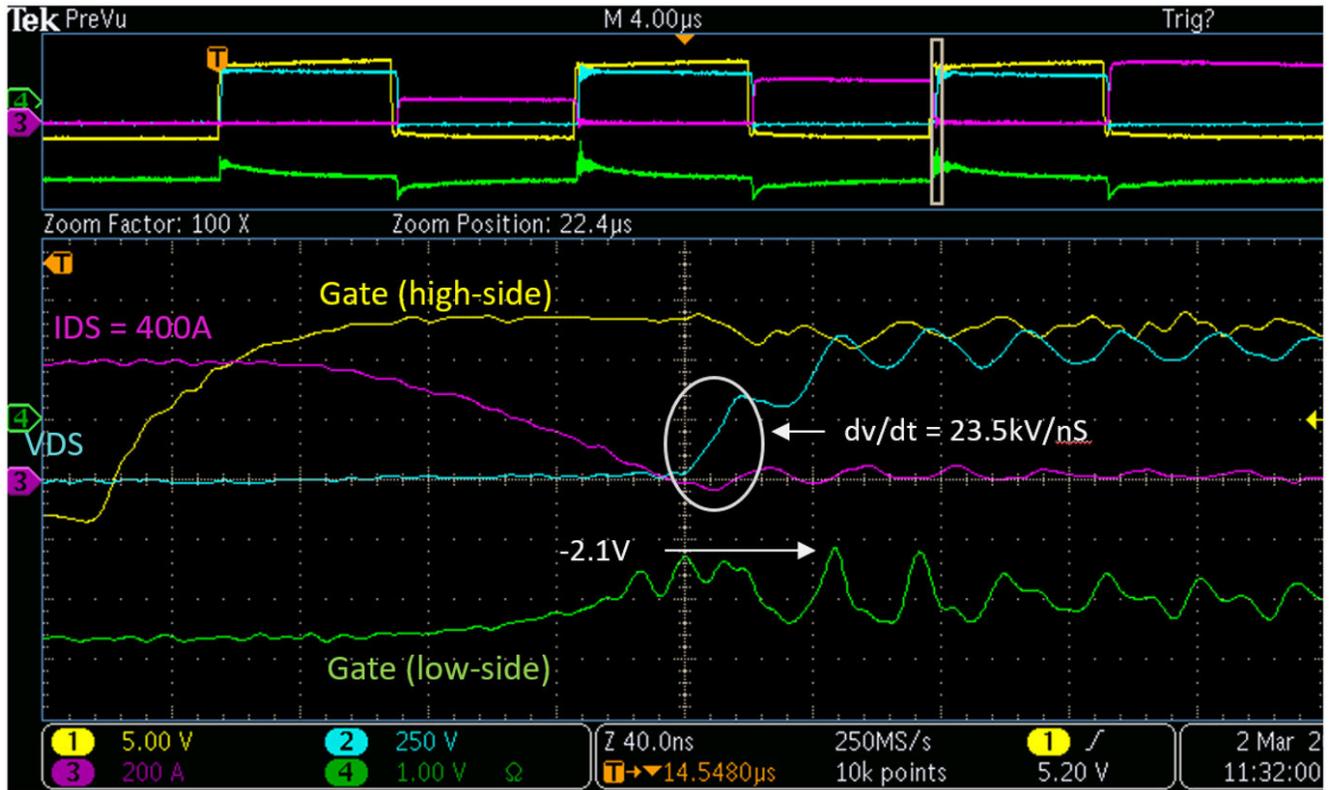


Figure 3.7. Crosstalk Test $R_H = R_L = 0 \Omega$, $V_{DS} = 600 \text{ V}$, $I_{DS} = 400\text{A}$, $L_o = 14 \mu\text{H}$ (Zoomed)

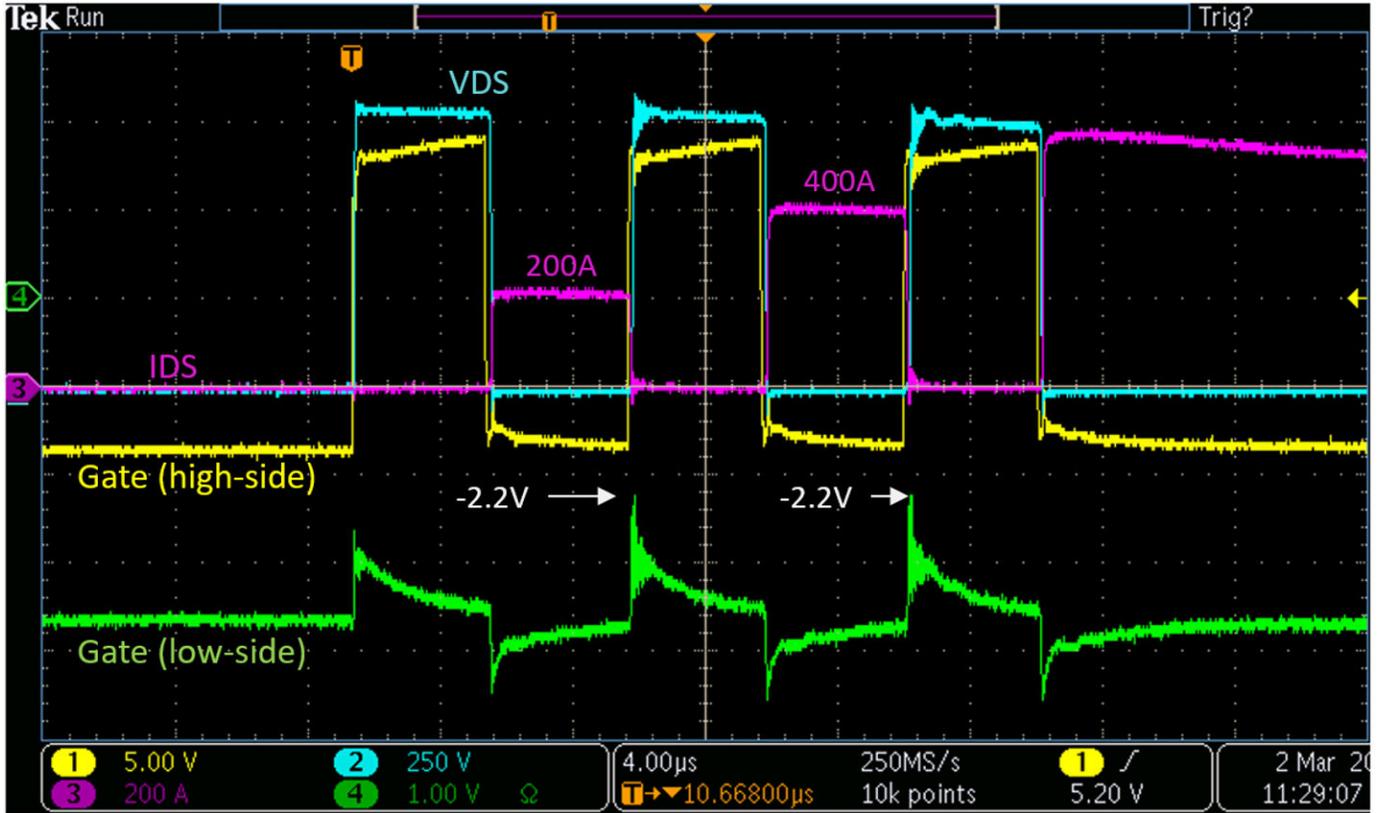


Figure 3.8. Crosstalk Test $R_H = R_L = 0 \Omega$, $V_{DS} = 800 V$, $L_o = 14 \mu H$

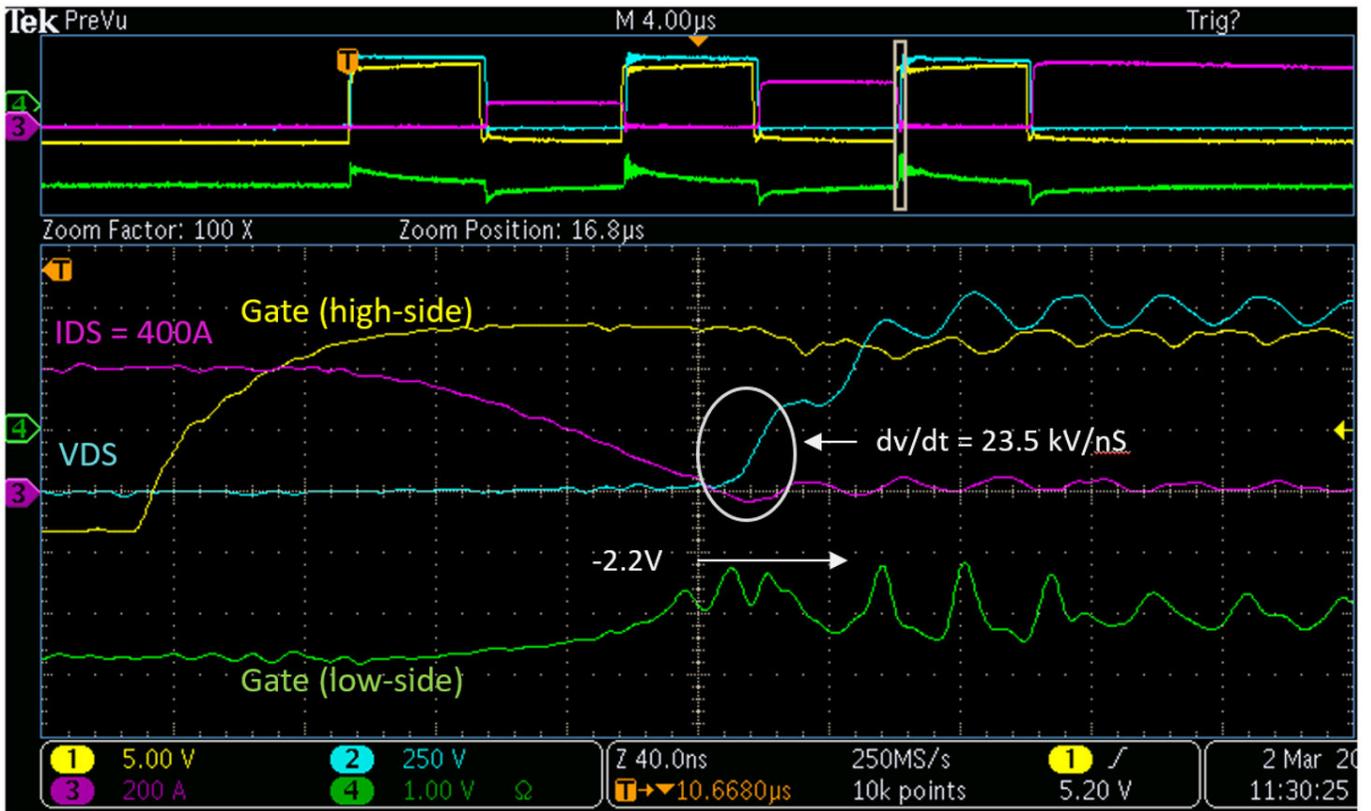


Figure 3.9. Crosstalk Test $R_H = R_L = 0 \Omega$, $V_{DS} = 800 V$, $L_o = 14 \mu H$ (Zoomed)

The table below summarizes the crosstalk test data. It shows that even under extreme conditions with 0 Ω gate resistors and $dv/dt = 25$ V/ns the driver can keep the low-side XM3 SiC MOSFET safely turned off at < -2 V, which is well below the minimum XM3 threshold voltage of $V_{th} = 2$ V.

Table 3.1. Crosstalk Test Results

Figure #	R348/R _H	R349/R _L	V _{dc} (V)	I _{DS} (A)	dv/dt (kV/ns)	V _G -max (V)
15	1	1	600	200	17	-2.2
15 (Z)	1	1	600	400	16	-2.4
16	1	1	800	200	16	-2.4
16 (Z)	1	1	800	400	16	-2.4
17	0	0	600	200	25	-1.9
17 (Z)	0	0	800	400	23.5	-2.1
18	0	0	600	200	23	-2.2
18 (Z)	0	0	800	400	23	-2.2

4. Switching Loss Testing

Switching loss testing was performed using a double-pulse test circuit, as illustrated in the figure below. This test measures the XM3 power loss during switching. Compared to the data sheet's XM3 switching loss, it verifies that the gate drivers have sufficient source and sink current capability to drive the XM3 SiC FET module with minimum switching loss.

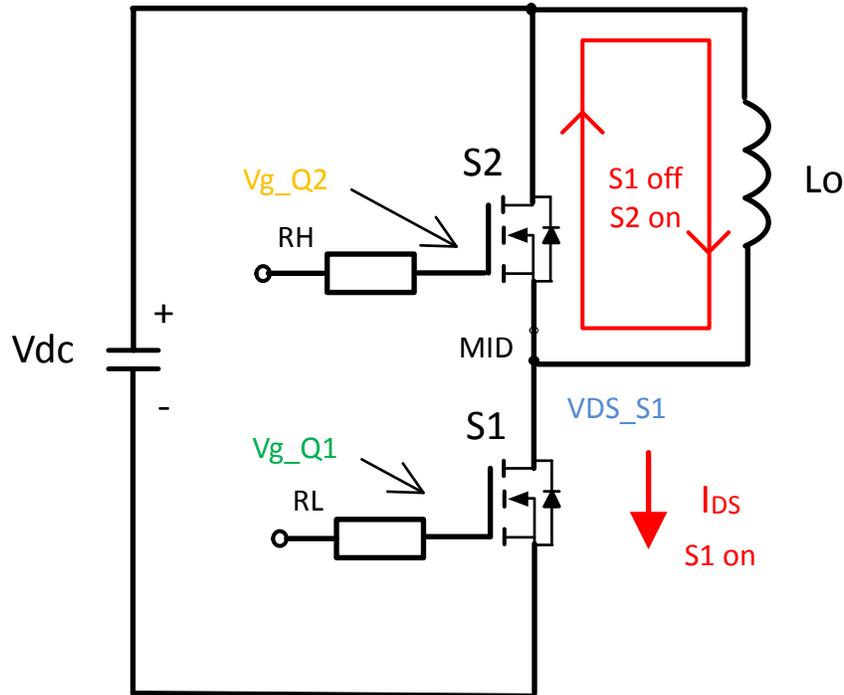


Figure 4.1. Switching Loss Test Circuit

4.1 Switching Loss Board Setup

In this test, S1 and S2 were driven by a two channel function generator to build up current through the air-core L_o inductor. Every time S1 is switched on (S2 is switched off), the current in L_o is ramped up and when S1 is switched off (S2 is switched on), L_o current is maintained through S2. This cycle is repeated multiple times to facilitate switching loss measurement on S1 at different current levels.

4.2 Switching Loss Test Results

An oscilloscope was used for switching loss measurements. The oscilloscope's math function integrates the product of S1's V_{DS} and I_{DS} over time to provide switching loss data. The scope image in the following figure indicates that S1 was turned on five times to ramp the I_{DS} current for switching loss measurement.

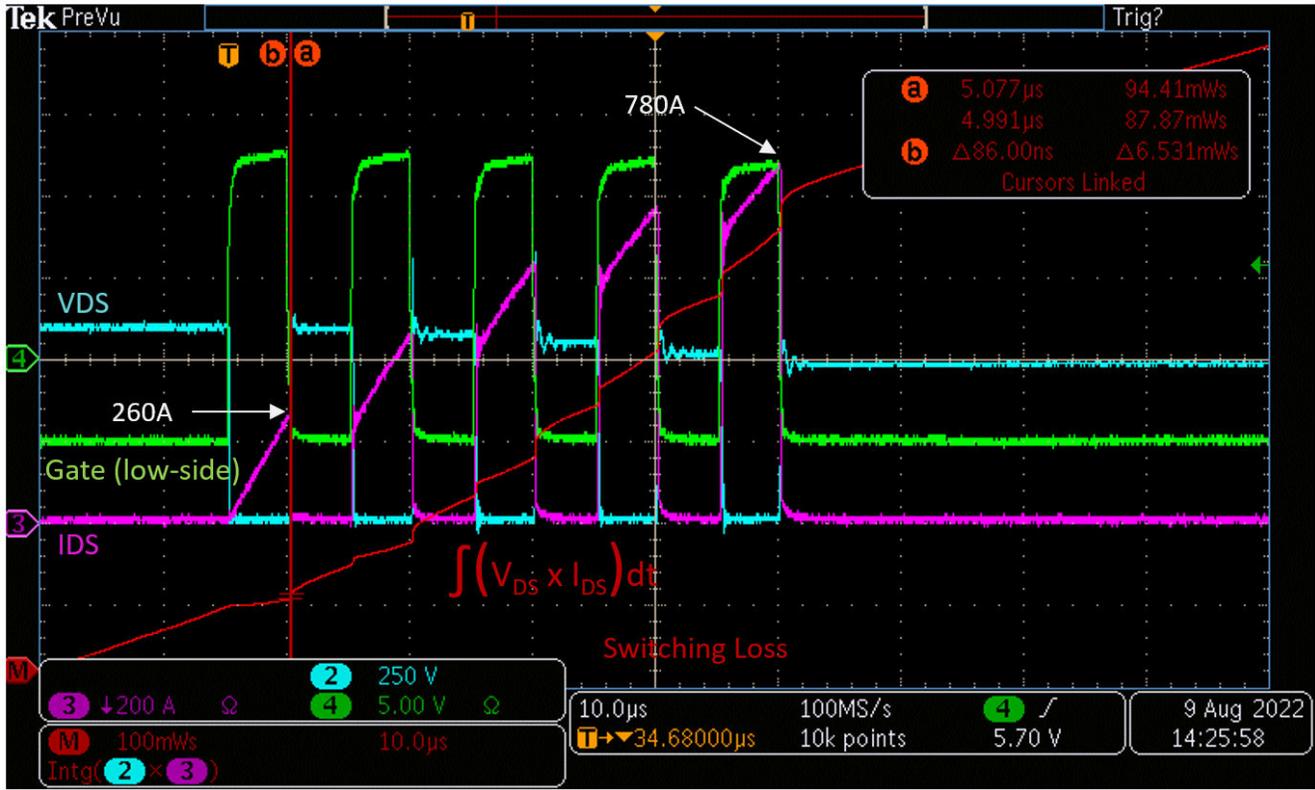


Figure 4.2. Switching Loss Test $R_H = R_L = 1 \Omega$, $L_o = 14 \mu H$, $I_{DS} = 0 A-780 A$, $V_{DS} = 600 V$

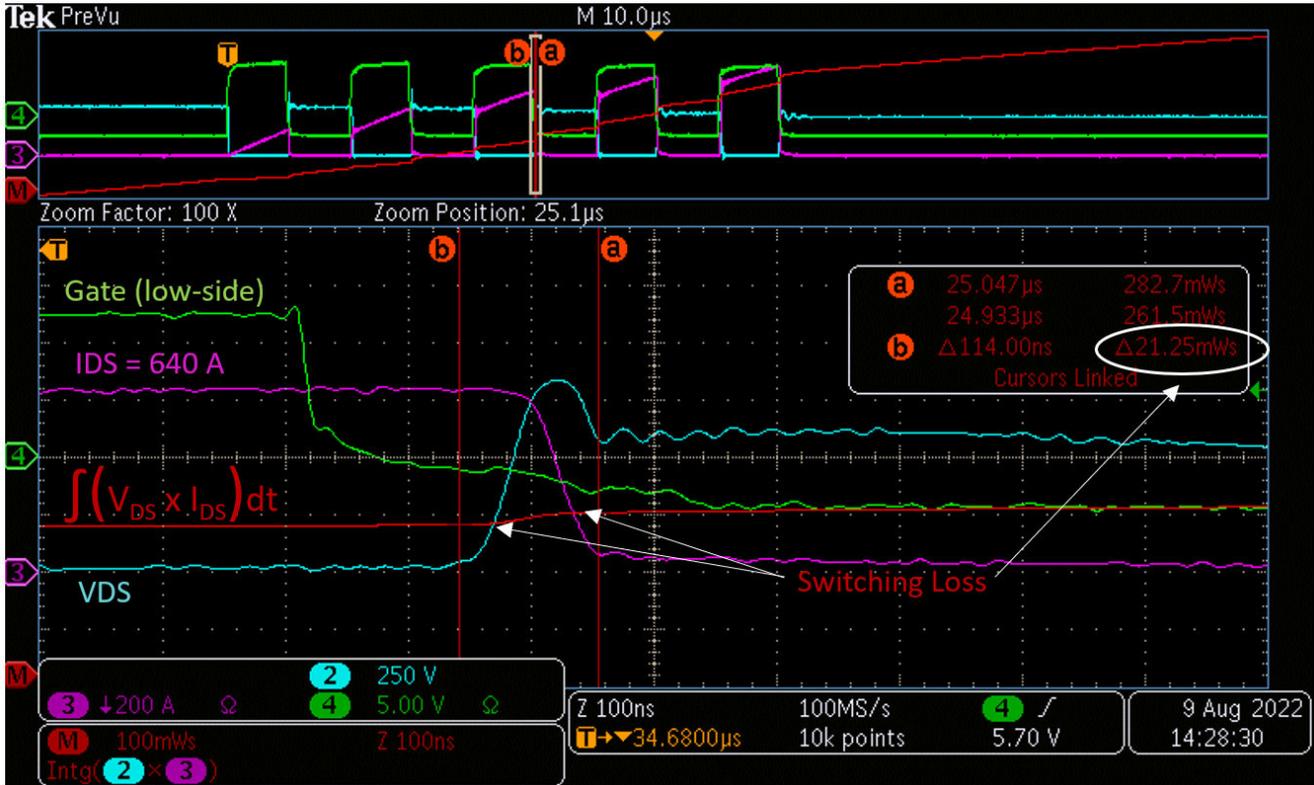


Figure 4.3. Switching Eoff Loss $R_H = R_L = 1 \Omega$, $I_{DS} = 650$ A, $L_o = 14 \mu$ H, ($V_{DS} = 600$ V)

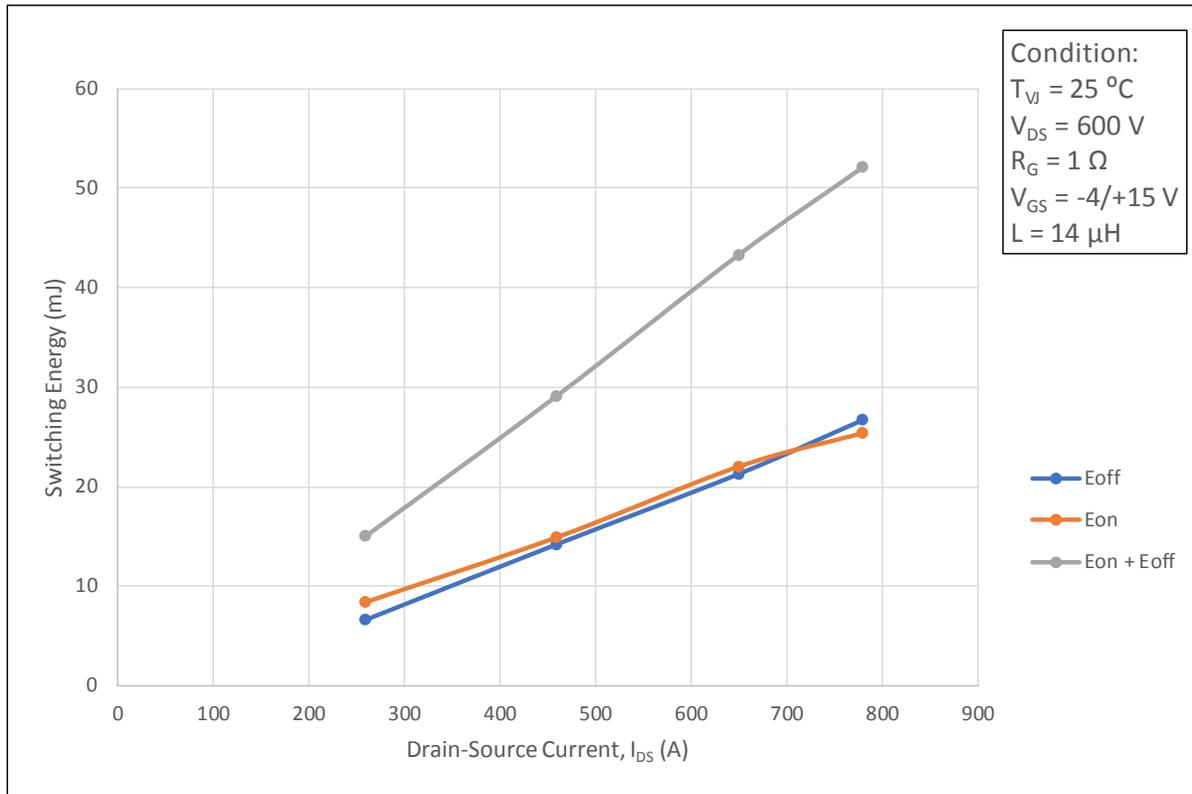


Figure 4.4. Switching Loss vs. Drain Current $R_H = R_L = 1 \Omega$ ($V_{DS} = 600$ V)

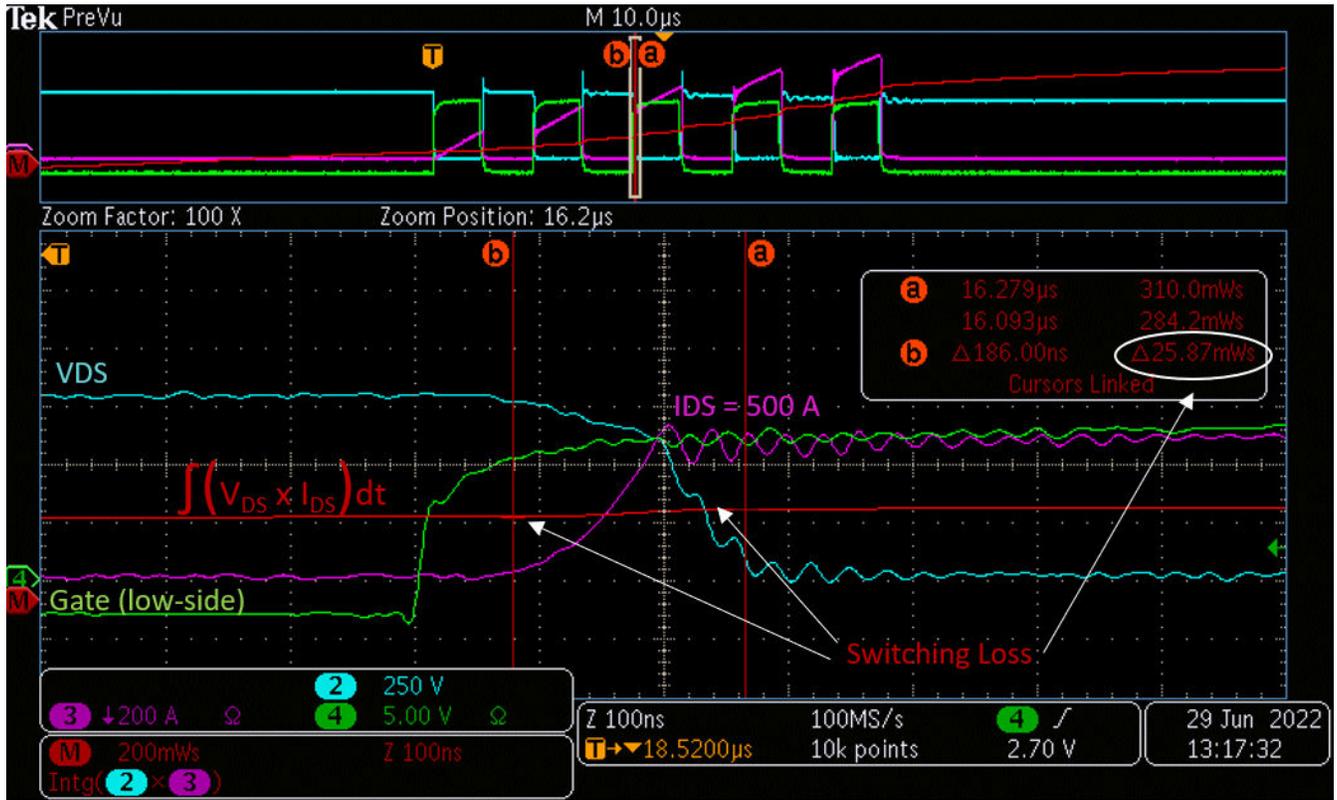


Figure 4.5. Switching Eon Loss $R_H = R_L = 1 \Omega$, $L_o = 14 \mu\text{H}$, $I_{DS} = 500 \text{ A}$, $V_{DS} = 800 \text{ V}$

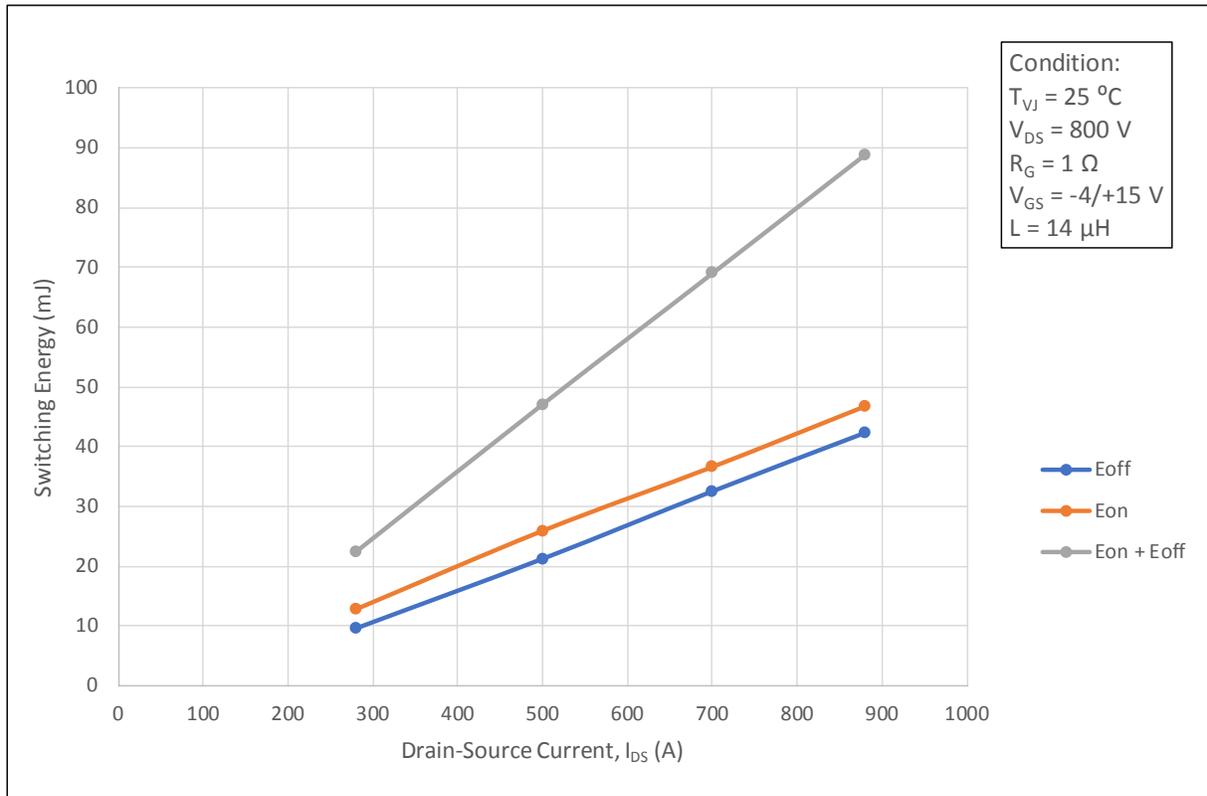


Figure 4.6. Switching Loss vs. Drain Current $R_H = R_L = 1 \Omega$ ($V_{DS} = 800 \text{ V}$)

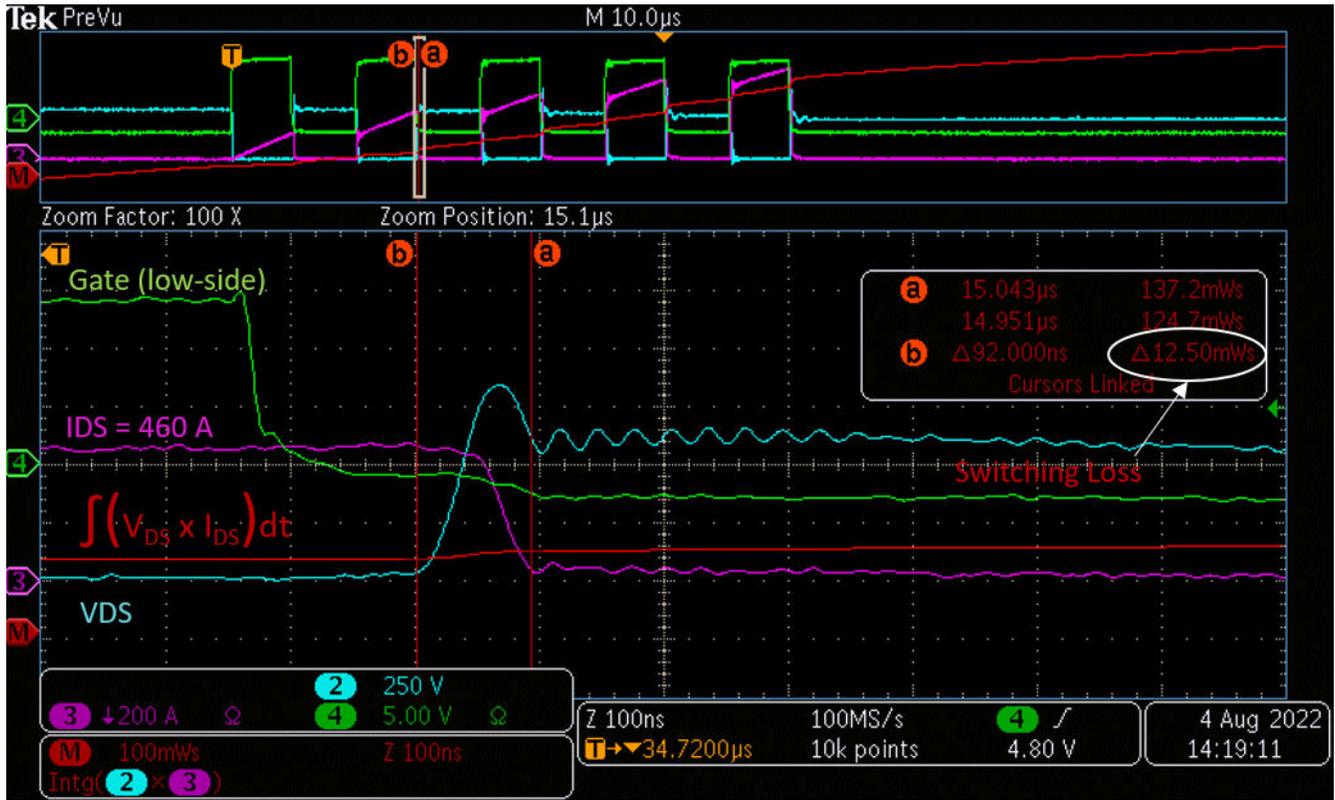


Figure 4.7. Switching Eoff Loss $R_H = R_L = 0.5 \Omega$, $L_o = 14 \mu\text{H}$, $I_{DS} = 460 \text{ A}$, $V_{DS} = 600 \text{ V}$

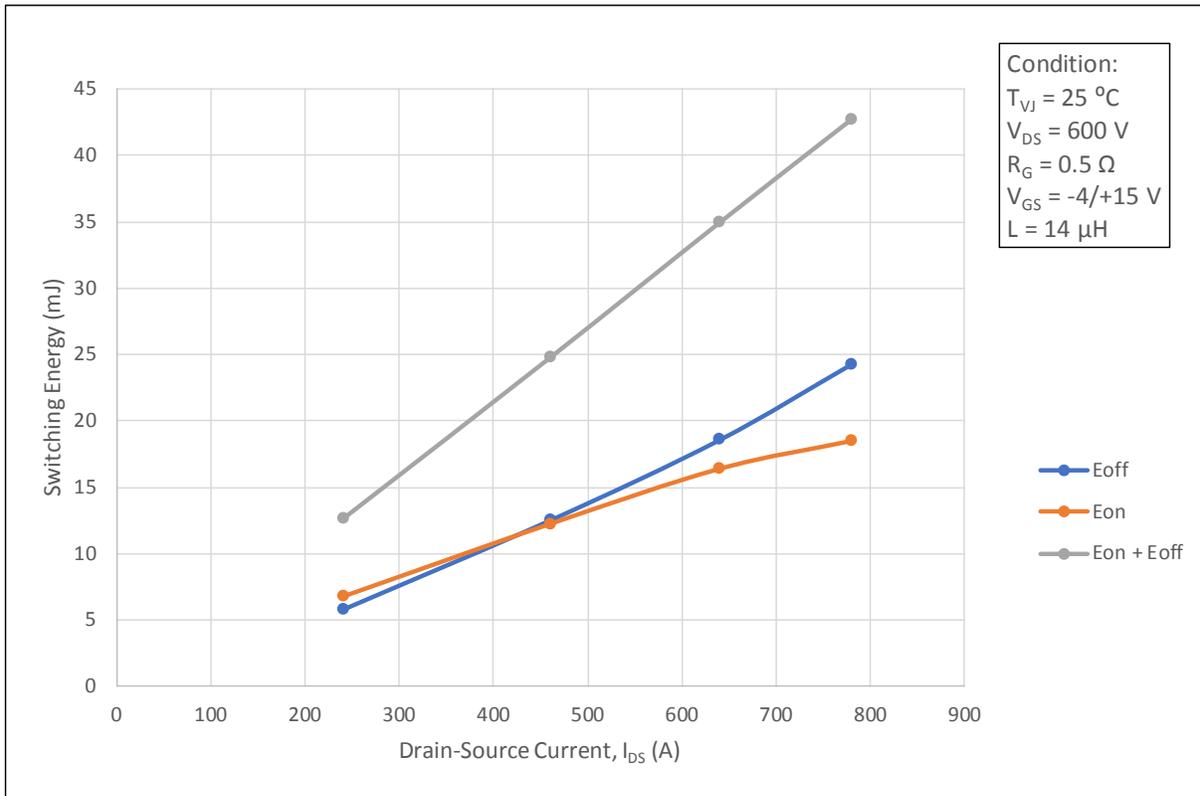


Figure 4.8. Switching Loss vs. Drain Current $R_H = R_L = 0.5 \Omega$ ($V_{DS} = 600 \text{ V}$)

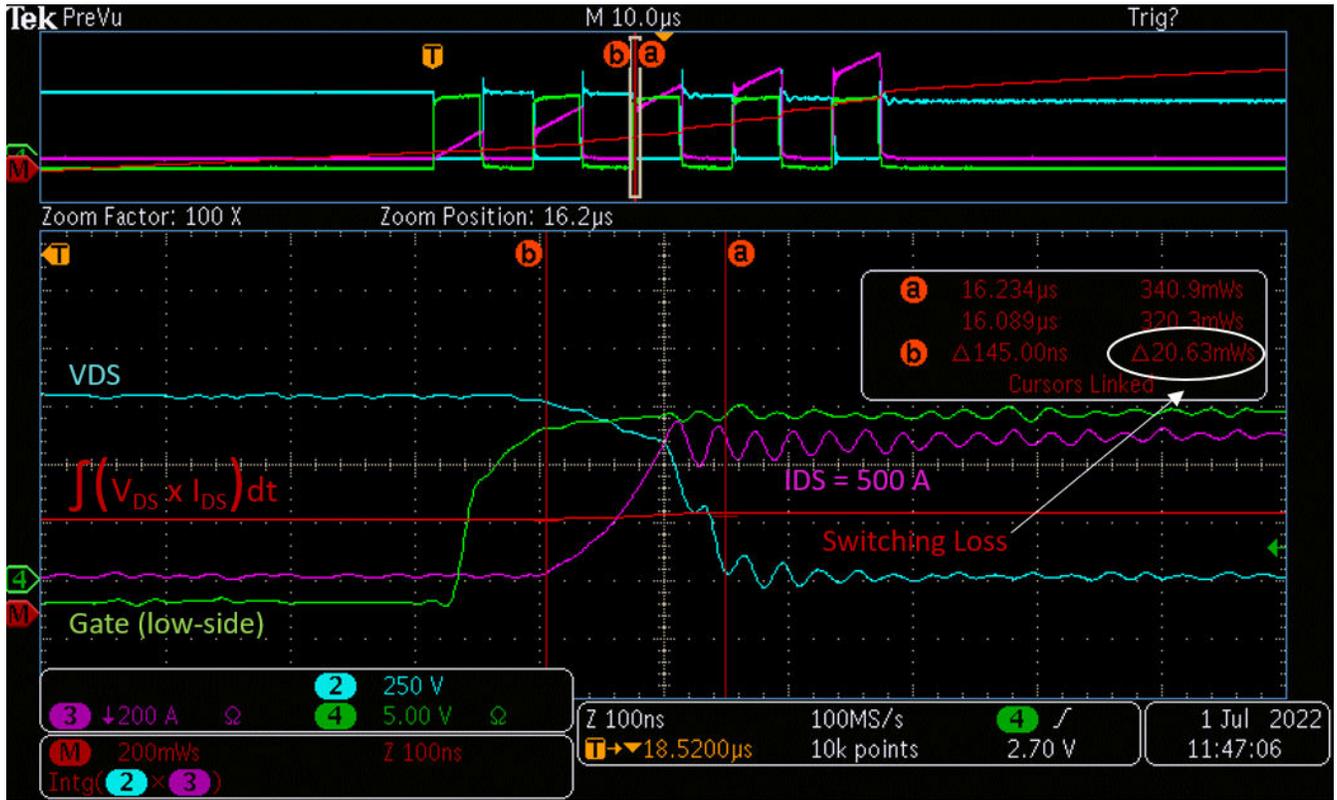


Figure 4.9. Switching Eon Loss $R_H = R_L = 0.5 \Omega$, $L_o = 14 \mu$ H, $I_{DS} = 500$ A, $V_{DS} = 800$ V

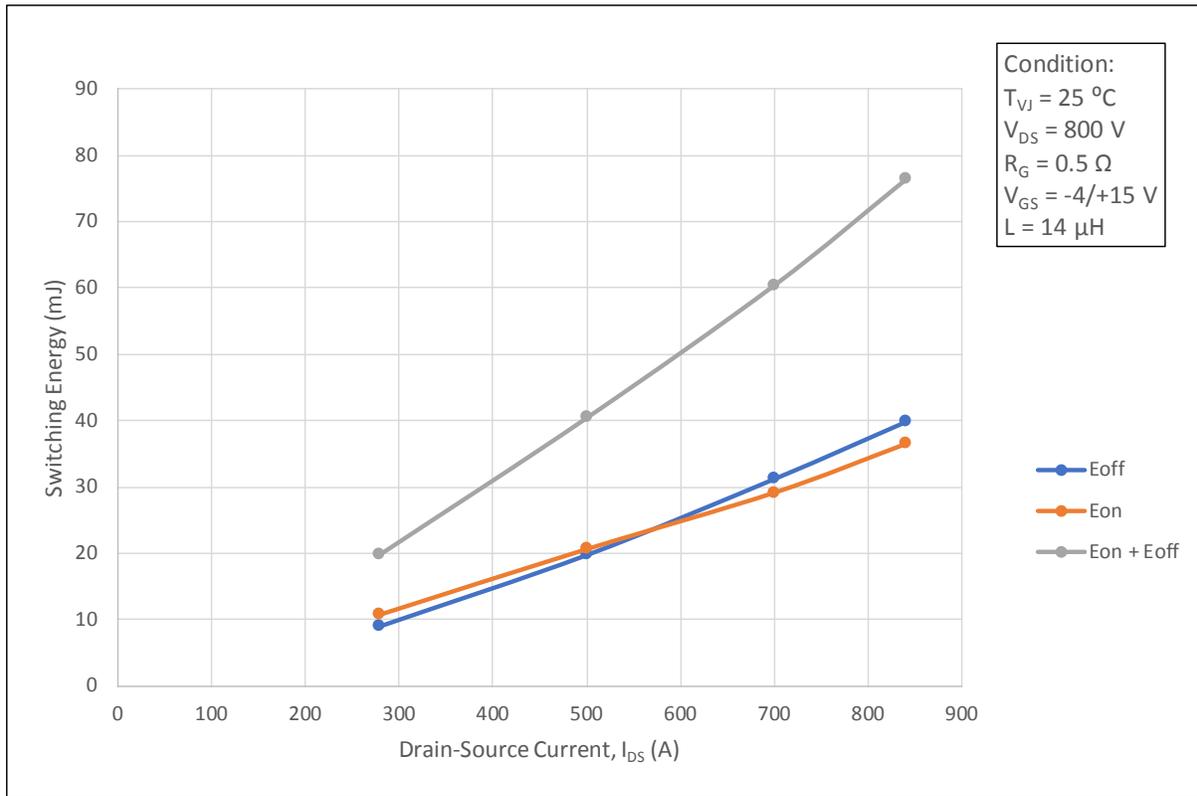


Figure 4.10. Switching Loss vs. Drain Current $R_H = R_L = 0.5 \Omega$ ($V_{DS} = 800$ V)

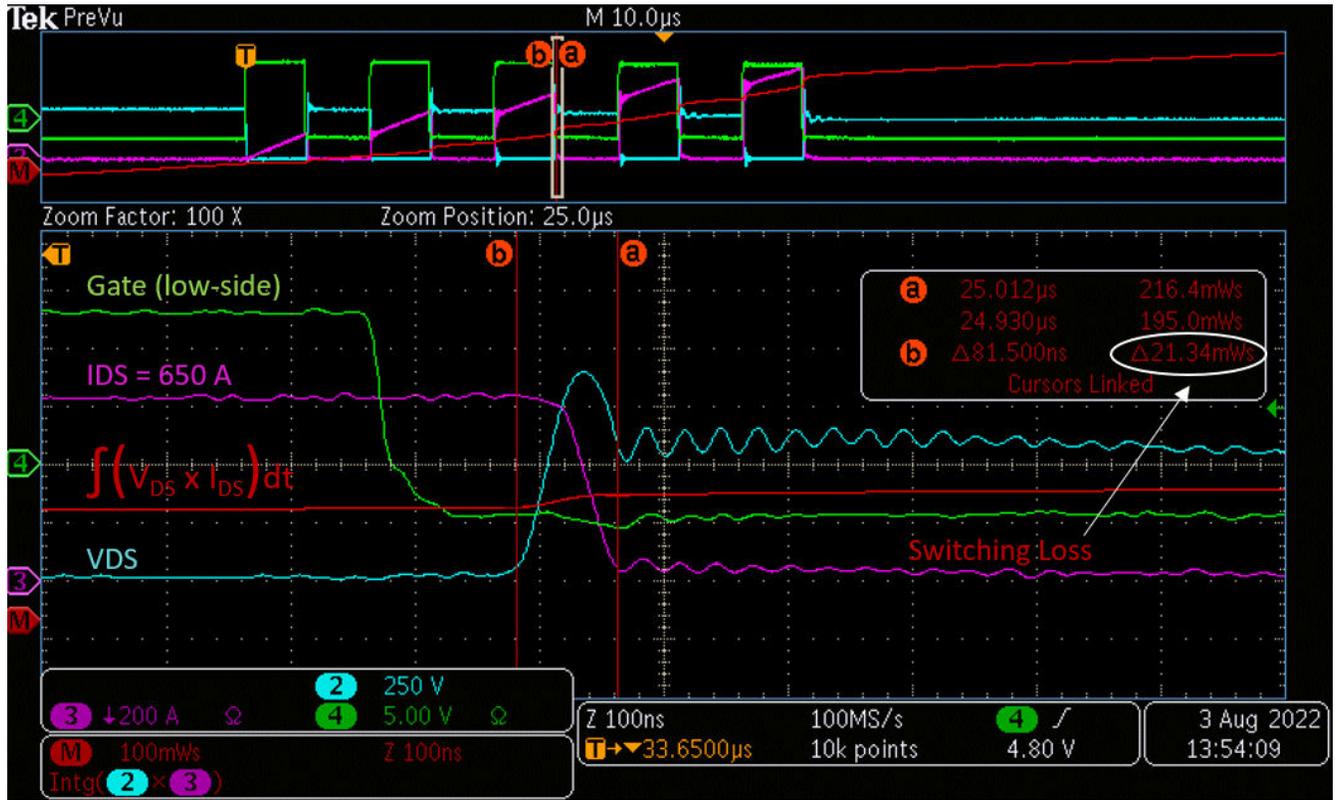


Figure 4.11. Switching Eoff Loss $R_H = R_L = 0 \Omega$, $L_o = 14 \mu\text{H}$, $I_{DS} = 650 \text{ A}$, $V_{DS} = 600 \text{ V}$

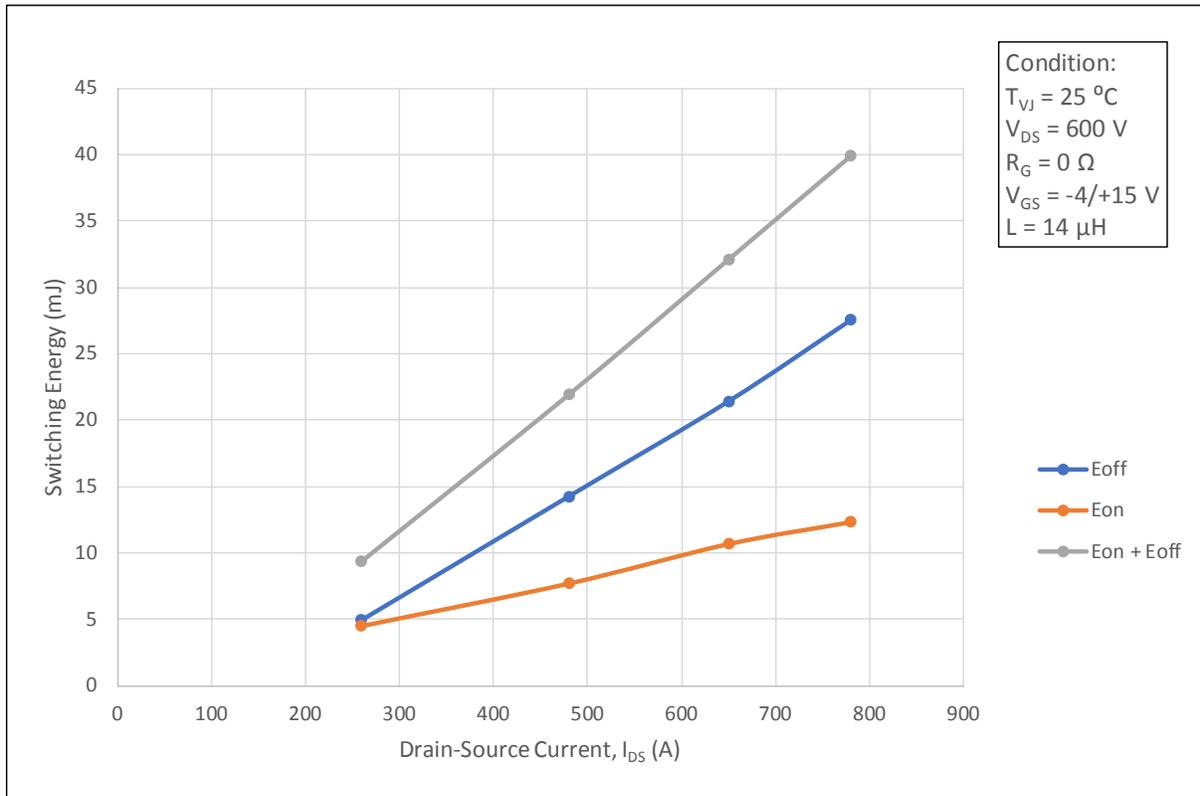


Figure 4.12. Switching Loss vs. Drain Current $R_H = R_L = 0 \Omega$ ($V_{DS} = 600 \text{ V}$)

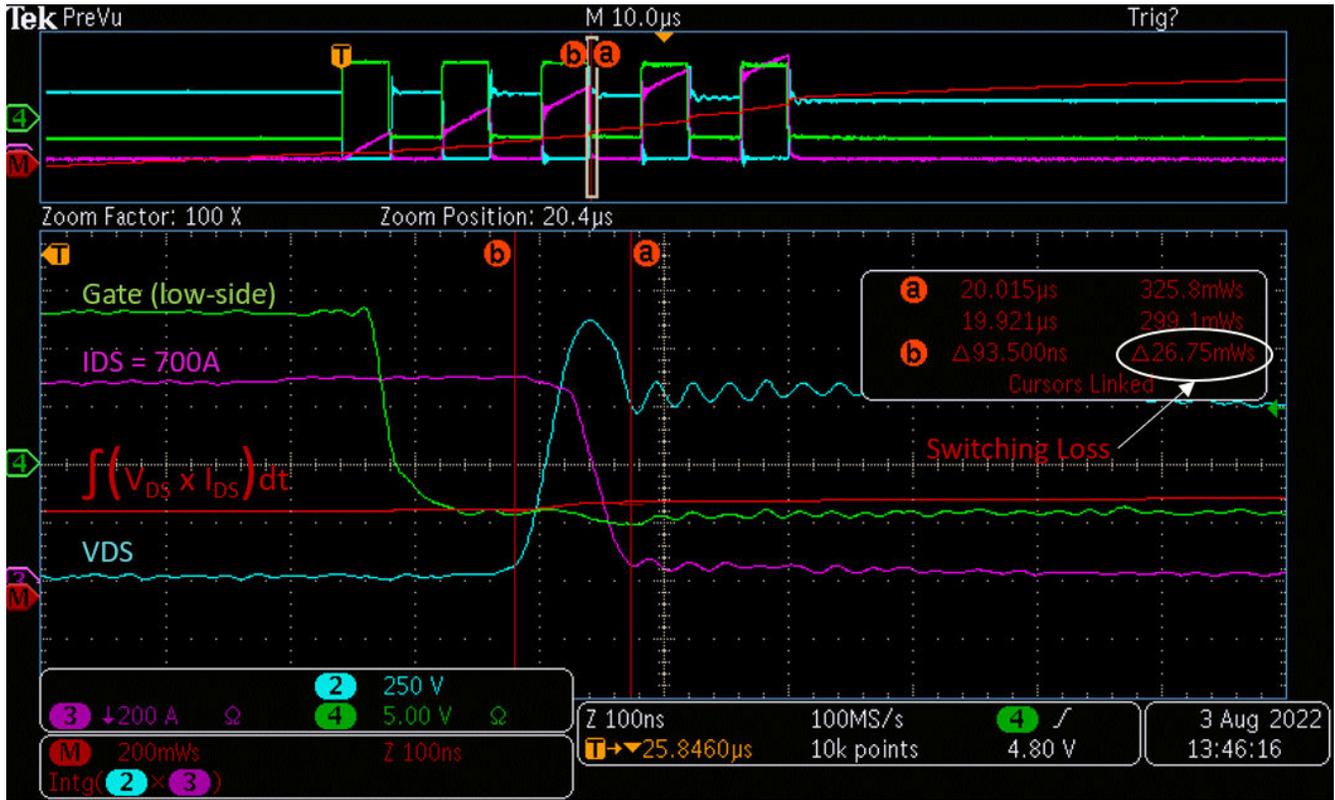


Figure 4.13. Switching Eoff Loss $R_H = R_L = 0 \Omega$, $L_o = 14 \mu H$, $IDS = 700 A$, $V_{DS} = 800 V$

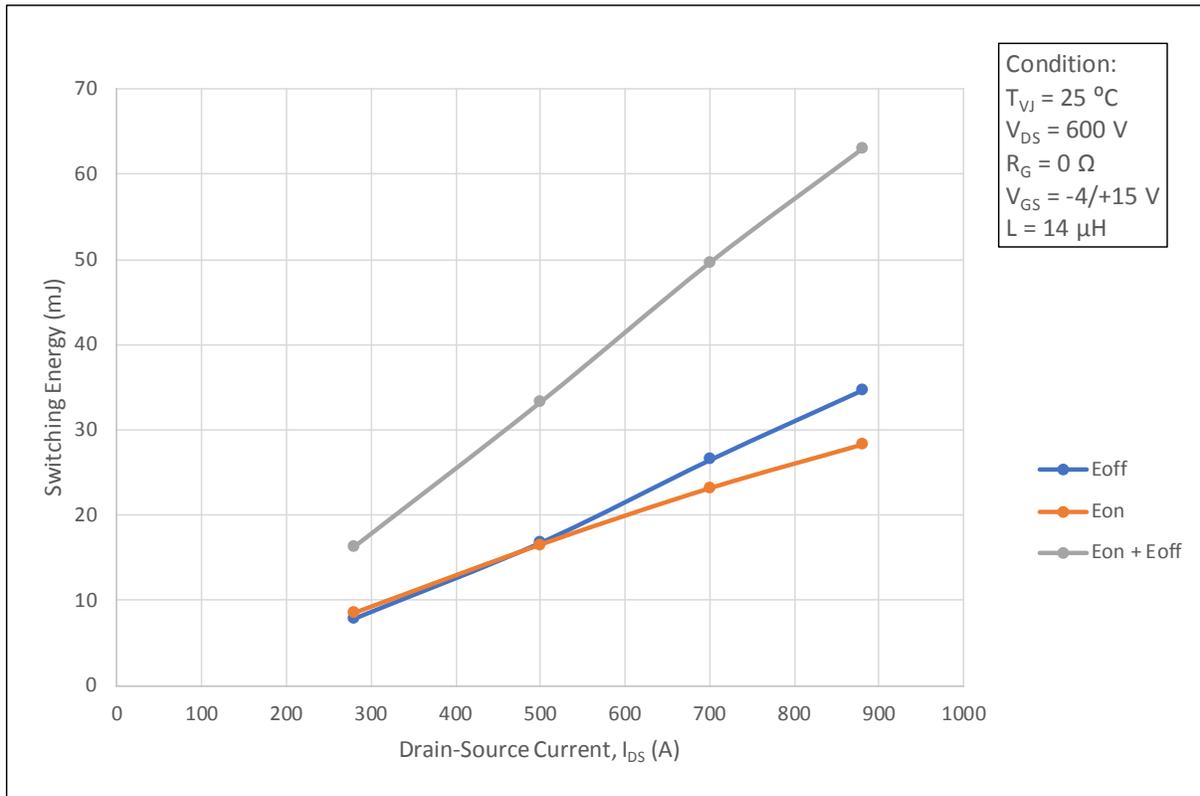


Figure 4.14. Switching Loss vs. Drain Current $R_H = R_L = 3.3 \Omega$ ($V_{DS} = 800 V$)

The following figures summarize total switching loss versus gate resistors at 600 V and 800 V, respectively. These switching loss results demonstrate the effect of different gate resistances on the switching losses and confirm that the Si828x gate driver circuit can drive the SiC FETs with a low, 0.5 gate resistor.

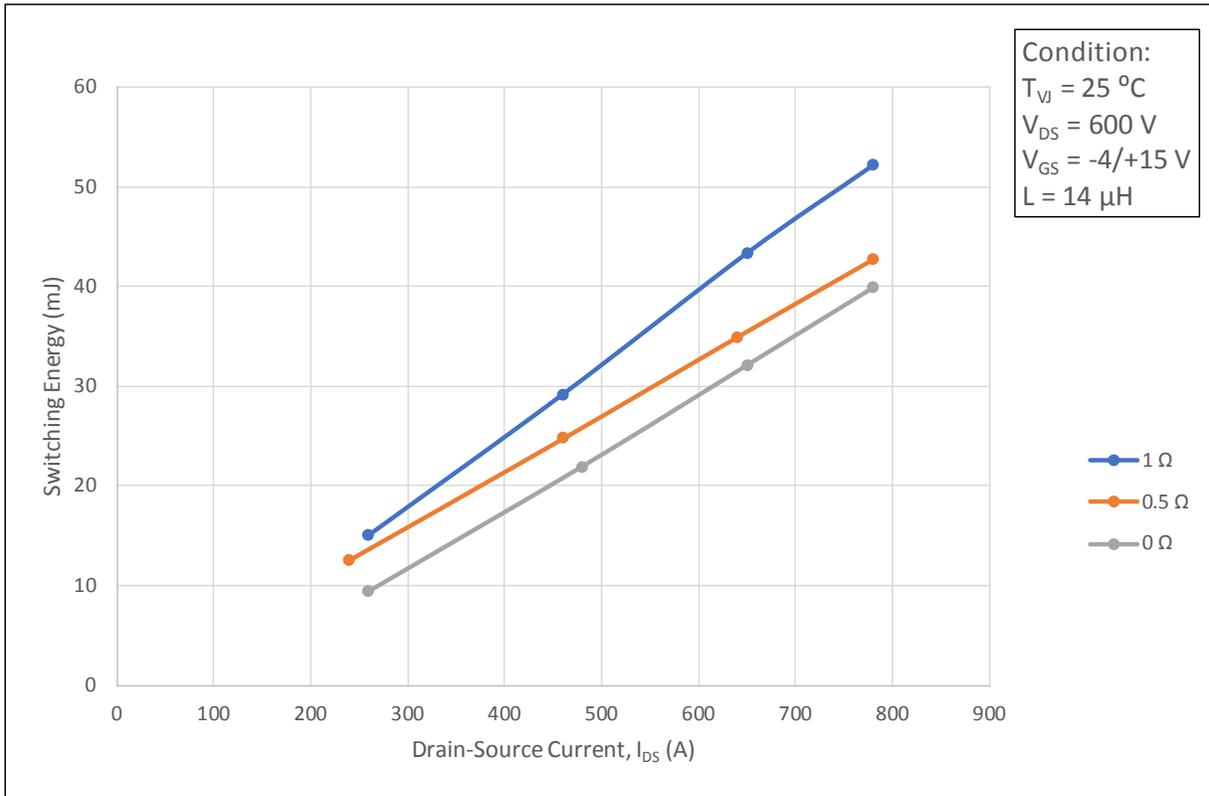


Figure 4.15. Total Switching Loss vs. Rg ($R_H = R_L$), $V_{DS} = 600 \text{ V}$

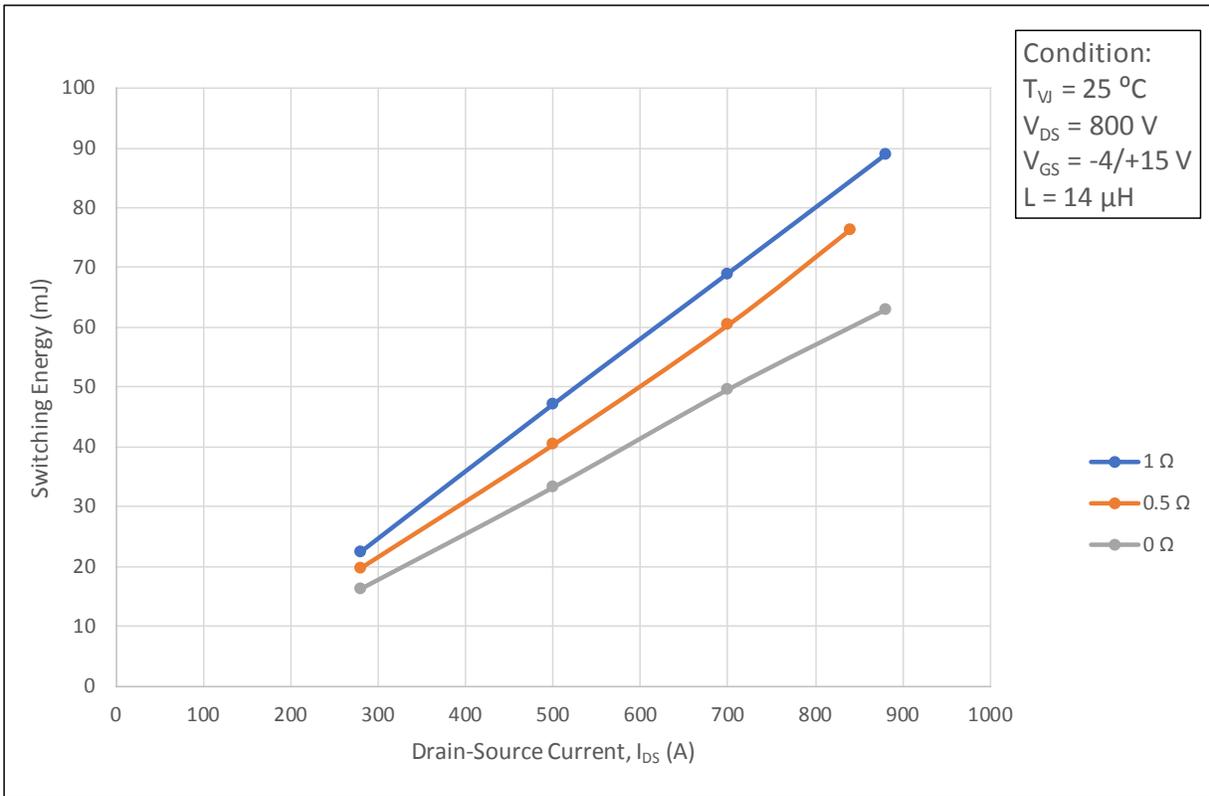


Figure 4.16. Total Switching Loss vs. Rg ($R_H = R_L$), $V_{DS} = 800 \text{ V}$

5. Conclusion

The above data demonstrate that the Skyworks Si828x gate driver circuits perform well with the Wolfspeed XM3 SiC FET module in critical characterization tests. The Si828x's DESAT protection circuit has a fast response time (less than 1 μ s) to minimize I_{DS} peak current and power dissipation on the XM3 module and reliably protects it under repeated extreme shorted conditions. The Si828x's DESAT circuits also provide flexible control, so designers can set the response timing, soft shutdown timing, and voltage spike levels for optimized protection.

The Skyworks Si828x driver was tested with the Wolfspeed 1.2 kV, 450 A CAB450M12XM3 SiC module and demonstrated sufficient drive strength to switch the part quickly, minimizing switching loss. The switching loss data with $R_g = 0.5 \Omega$ looks similar to the switching loss in the CAB450M12XM3 data sheet. Furthermore, the Si828x demonstrated immunity to both crosstalk and high common-mode transients present in a hard-switched SiC FET topology, and the Miller Clamp and negative gate bias eliminated dv/dt-induced turn-on. The specific Skyworks drivers evaluated in this test were the Si8284 and the Si8285, but the entire Si828x series of drivers offers the same short-circuit protection and CMTI capabilities.

Together, Skyworks' Si828x family of drivers and Wolfspeed's XM3 SiC module tested in this report enable high-efficiency, robust power conversion.

6. Revision History

Revision 206423A

November, 2022

- Updated decimal-based revision numbering system to alpha-numeric revision code.
- Updated [1.1 Si828x Isolated Gate Driver](#).
 - Updated [Figure 1.1 Si8285 and Si8284 Gate Drivers](#) on page 3.
 - Updated [Figure 1.2 Low-Voltage Signals and I/O](#) on page 4.
 - Updated [Figure 1.7 Si828x-AW-GDB Evaluation Board](#) on page 9.

Revision 0.1

March, 2022

- Initial release.

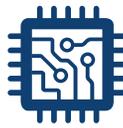


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