High Voltage SOI Stacked Switch with Varying Periphery FETs

Yu Zhu, Oleksiy Klimashov, Ambarish Roy, Guillaume Blin, David Whitefield, and Dylan Bartle
Skyworks Solutions, Inc.
20 Sylvan Rd.
Woburn, MA 01801 USA

Abstract-The breakdown voltage of a FET stack is limited by the unequally divided voltage drop among the stacked FETs. A novel stack composed of varying periphery FETs is proposed. Uniform voltage distribution, and thus much higher breakdown voltage, can be achieved by carefully designing the periphery of each FET. A FET stack with varying periphery was designed and fabricated. Significant improvement in breakdown voltage was experimentally confirmed. Unlike the approach of inserting feed-forward capacitance, the breakdown voltage increase is achieved without isolation degradation.

I. INTRODUCTION

A high-quality microwave switch is a key block of an RF front end of time division duplexing (TDD) wireless communication system. The power handling capability is the most stringent specification of antenna switches. Among various process technologies, silicon-on-insulator (SOI) CMOS process has become a promising technology [1, 2].

The antenna switch is designed with each branch being able to support the maximum voltage seen at the antenna. In SOI technology, where the FET breakdown is much lower than the peak RF voltage, stacking FETs into a cascade configuration is a straightforward way to withstand the voltage [3]. It was believed that the voltage across the stack is equally divided among the stacked FETs [4]. For a shunt branch of stacked FETs, the breakdown voltage can thus be written as

$$BV = nBV_{FET},$$

(1)

where $BV_{FET}$ is the breakdown voltage of a single FET, and the $n$ is the number of stacked FET, namely the stack height.

Because of the capacitive coupling between off state FET and the ground, however, the voltage drop across the FET stack is not equally divided. The voltage drop decreases gradually from the signal input side to the grounded side. The FET at the input side sees the biggest voltage drop, which limits the stack breakdown voltage.

The breakdown voltage of FET stack can be expressed as [5].

$$BV = \sqrt{\frac{C_{ds}}{C_{gnd}}} \sinh(2n\alpha) BV_{FET}$$

(2)

where $C_{ds}$ and $C_{gnd}$ are the drain-source capacitance and the capacitance to the ground, respectively, and $2\sinh\alpha = \sqrt{\frac{C_{gnd}}{C_{ds}}}$. Fig. 1 shows the stack height dependence of breakdown voltage depicted by (1) and (2) respectively. It can be seen that no matter how many FETs are stacked, the maximum breakdown voltage can be achieved is [5]

$$BV_{\text{max}} = \left(\frac{C_{ds}}{C_{gnd}} + 0.5\right)BV_{FET}$$

(3)

Feed-forward capacitances have been used to increase the stack breakdown voltage via reducing the uneven distribution of the voltage drop [6]. However, the feed-forward capacitances inserted inevitably increases the off state capacitance. The increase in breakdown voltage is achieved at the expense of isolation degradation.

A novel stack composed of varying periphery FETs is proposed in this paper. A uniform voltage distribution can be achieved by carefully designing the periphery of each FET stacked. The stack breakdown voltage can thus be increased with no extra capacitance, and thus no isolation degradation.

This paper is organized in the following way. The analysis of the voltage distribution inside FET is performed with electromagnetic (EM) simulation and equivalent circuit in II. The stack with varying periphery is proposed in III, the design procedure and measurement results are also provided. A conclusion is given in IV.
II. VOLTAGE DISTRIBUTION INSIDE STACK

EM simulation can be a powerful tool for investigating the voltage distribution inside a FET stack. Since MOSFET, being considered as an active device, actually works in its passive states in a switch, EM simulation was performed on the entire MOSFET including both the metal electrodes and the semiconductor channels [7].

In order to find the internal voltage distribution, ports are attached at both drain and source sides of each FET. N+1 ports are needed for a stack with n FETs. The simulated S parameter was then imported into a circuit simulator and represented with an n+1 port black box. The stack is connected between a signal source and the ground. The voltage distribution can easily be obtained with an AC simulation at desired frequency. The simulated voltage drop inside stack, shown in Fig. 2, is believed to be accurate, since all of the coupling and distributed effects were taken into account.

An equivalent circuit, shown in Fig. 3, is then generated to gain more insight into the voltage distribution. There are three kinds of capacitances, the $C_{ds}$, $C_{gnd}$, and $C_{cp}$, the coupling capacitance among FETs. All of the capacitances can be accurately extracted from the $Y$ parameters, which was converted from simulated $S$ parameters, as

$$C_{ds,i} = -\text{imag}(Y_{di,i+1}) / \omega,$$  \hspace{1cm} (4)

$$C_{gnd,i} = \text{imag}(\sum_{j=1}^{n} Y_{ij}) / \omega,$$  \hspace{1cm} (5)

$$C_{cp,ij} = -\text{imag}(Y_{ij}) / \omega.$$  \hspace{1cm} (6)

As shown in Fig. 2, the voltage drop distribution from the EM simulation can be accurately reproduced with the equivalent circuit.

III. STACK WITH VARYING PERIPHERY FETS

The FET stacks reported so far are composed of FETs with the same periphery, which lead to unequally divided voltage drop as shown in II. A stack with varying periphery FETs is proposed in this paper. The periphery of each FET inside the stack is carefully designed to achieve uniform voltage drop. The stack breakdown voltage can therefore be increased without degrading the isolation.

Since the current changes along the stack, the uniform voltage drop can be achieved by adjusting the impedance. Unlike the approach of inserting feed forward capacitance, the impedance is changed by changing the periphery of each FET. FET periphery can be changed either by changing finger number or by changing the unit gate width.

A stack with varying unit gate width FETs is investigated in this study. The design procedure is as follows

1) EM simulation is first performed on a stack composed of the same periphery FETs.
2) The equivalent circuit, as shown in Fig. 3, is then extracted from the simulated $S$ parameter.
3) Optimization of the equivalent circuit is then performed to achieve uniform voltage drop with each $C_{ds}$ set as optimal variable.
4) The optimized FET peripheries can easily be determined based on extracted $C_{ds}$ values.
5) The voltage distribution is confirmed by performing EM simulation on a stack composed of FETs with optimized peripheries.
The uniformity of the voltage drop distribution can be further improved by iterating the procedure. Fig. 4 shows the distribution of voltage drop for the stacks with the same and the optimized peripheries, respectively. Significant improvement in the voltage distribution can be observed. A SOI FET stacked with 35 FETs has been designed and fabricated. As shown in Fig. 5, the breakdown voltage above 100V has been achieved with varying periphery FETs, and no additional capacitances are needed.

**IV. CONCLUSIONS**

The voltage distribution inside FET stack has been investigated with EM simulation. An equivalent circuit is then extracted from the simulated S parameter. It is shown that the stack breakdown voltage is limited by the unequally divided voltage drop among the FETs. A novel stack with varying periphery FETs is proposed to achieve a uniform distribution of voltage drop. The design procedure is then described. Significant improvement in voltage drop distribution has been achieved in the simulation. A 35-FETs stack is designed and fabricated. Breakdown voltage of 100V is achieved experimentally with no isolation degradation.

**REFERENCES**


