Highly integrated CMOS RF SPDT switch with ESD and unit cell optimisation in MCM

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Presented is the performance of a highly integrated RF single-pole double-throw (SPDT) switch fabricated in a 0.18 μm bulk CMOS process and housed in a low-cost laminated multi-chip module (MCM-L) package. A switch controller is also implemented and consumes ~40 μA from a 3.4 V supply. The switch, based upon the 1.8 V thin-oxide devices with resistive body-floating and unit cell layout optimisation techniques, achieves an insertion loss of 0.52/0.78 dB at 0.9/2.45 GHz, respectively. TX-to-RX isolation of >29 dB and return loss of >15 dB are achieved at these frequencies. The measured IP_{1dB} of 21.7/21.2 dBm and IIP_3 of 38.3/37.4 dBm are accomplished at 0.9/2.45 GHz, respectively. Finally, the switch achieves a RF electrostatic discharge (ESD) rating of 4 kV for the ±2 kV human body model and 500 V for the ±200 V machine model.

Introduction: Low-cost silicon bulk CMOS technologies have been used ubiquitously for decades for modern wireless communication systems. However, the high power amplifier (PA) and transmit/receive (T/R) switch remain to be the two most critical front-end components to be ultimately integrated to realise a true system-on-chip (SOC) for wireless transceivers. Switches with reasonably low insertion loss (IL), high isolation, linearity, and moderate to high power handling capability that were once only possible in the III-V compound semiconductors such as the GaAs pHEMT have emerged in silicon bulk CMOS [1–6] and silicon- on-insulator (SOI) [7]. In this Letter, we present the performance of an area-efficient CMOS RF single-pole double-throw (SPDT) switch and consider the practical aspects of electrostatic discharge (ESD) protection, integrated switch controllers, as well as laminated packaging. Design techniques including resistive body-floating and unit cell layout optimisation are demonstrated on the 1.8 V thin-oxide triple-well devices.

Switch design: Illustrated in Fig. 1 are the SPDT switch and switch controller. The switch consists of two series FETs (M1 and M2) and two shunt FETs (M3 and M4). The width of the series devices (324 μm) is chosen to accommodate the IL performance over the frequency range of interest (0.9–2.45 GHz). The shunt device is ~1/4 the size of the series devices to improve the isolation with a marginal penalty on the IL. The high precision control voltages for the switch are internally generated by an integrated switch controller, which is composed of a bandgap reference, low dropout regulator (LDO), and digital logics. The equivalent circuit of a triple-well FET with biasing for both ON- and OFF-state is described in Fig. 2. During ON-state, V_{SB}/V_{DB} is set to 0 V for best IL (no bulk effect) for a given V_G. High value unsilicided poly gate resistors (40 kH) are used to improve IL further and mitigate the degradation in power handling capability at high input power [7]. The body-floating resistor ($R_{BF} = 25$ kΩ) is introduced to ensure that the bulk terminal voltage swing is in accordance with the source/drain. This also guarantees that the source/drain-to-bulk is reversed-biased to achieve good linearity and avoid excessive capacitive coupling to the substrate. A customised unit cell technique is applied towards the device layout that improves IL by reducing the intrinsic distributed series source/drain resistances and extrinsic source/drain interconnect resistances, as illustrated in Fig. 3*a*. A 3 × 3 unit cell matrix layout with source/drain sharing to minimise the parasitic capacitance is used for the series switch devices, with finger width (W_f) of 4 um and nine fingers. During OFF-state, V_{SB}/V_{DB} is biased at 1 V (Fig. 2*b*) in order to delay the onset of the junction diodes (C_{SB}/C_{DB}), thus improving the power handling capability. Consequently, the V_G is 2.8 V for ON-state and 0 V for OFF-state while the source and drain voltages are biased at 1 V (compromise between turn-on of V_{GD}/V_{GS} and gate oxide breakdown for the OFF devices). The V_{nwell} is biased at the highest potential available (3.4 V) to keep $C_{pwell-nwell}$ and $C_{nwell-psub}$ reversed-biased while improving the compression characteristics at high power levels. RF ESD protection is also implemented at the Ant port which is typically exposed and most likely to encounter an ESD event. The reliability issue for a switch design is more susceptible to time-dependent dielectric breakdown (TDDB) which is a strong function of the electric field across the gate dielectric. The diode size and number of diode stacks are trade-offs among the gate oxide reliability, IL due to the diode parasitic capacitance and series resistance, and linearity. In this design, the number of series diode stacks connected anti-parallel to ground is four. The degradation in the IL due to the additional ESD diodes is ~0.07 and ~0.1 dB in simulation at 0.9 and 2.45 GHz, respectively. The core switch area is only 0.02 mm^2 while the effective area for the switch controller is ~0.04 mm^2, as shown in Fig. 3*b*.

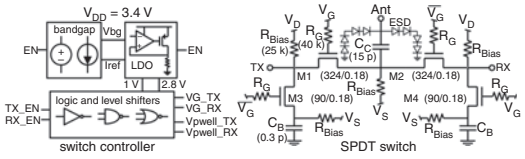

Fig. 1 *Simplified block diagram of switch controller and SPDT*

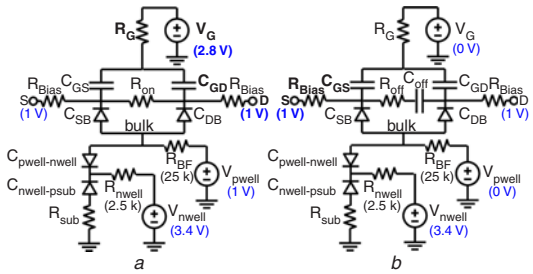

Fig. 2 *Equivalent circuit model of triple-well FET with biasing scheme*
a ON-state
b OFF-state

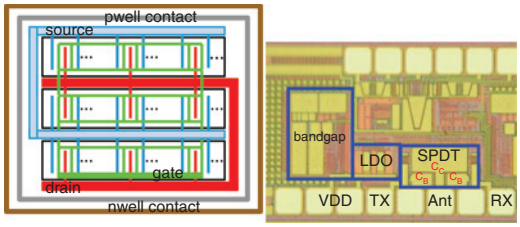

Fig. 3 *Customised unit cell layout and chip microphotograph*
a 3 × 3 unit cell matrix layout of series switch device
b Chip microphotograph of SPDT and switch controller breakout

Experimental results: The characterisation of the multi-chip module (MCM)-packaged switch was mounted on an evaluation board as shown in Fig. 4. Due to the symmetrical packaged switch design, the measurement data for the TX-to-Ant path and the Ant-to-RX path are nearly identical. Between 900 MHz and 3 GHz, the switch achieves a return loss (RL) >15 dB at both the TX port and the Ant port, from −20 to 85 °C (Fig. 5*a*). The measured IL at 25 °C is 0.52 and 0.78 dB at 0.9 and 2.45 GHz, respectively. Under the worst-case temperature (85 °C), the measured IL (Fig. 5*b*) is 0.59 and 0.89 dB at 0.9 and 2.45 GHz, respectively. This increase in IL at the hot condition is mainly attributed to the mobility degradation of the FET device in strong inversion. The loss associated with the package is ~0.05 and ~0.14 dB at 0.9 and 2.45 GHz, respectively. The isolation from TX to RX (TX mode) illustrated in Fig. 5*c* is >31 dB while that from Ant to TX (RX mode) is >22 dB at 2.45 GHz (85 °C). Depicted in Fig. 5*d*, the measured IP_{1dB} is 21.7 and 21.2 dBm at 0.9 and 2.45 GHz, respectively. The measured IIP3 (two-tone spacing of 1 MHz) is 38.3 and 37.4 dBm at 0.9 and 2.45 GHz, respectively. The switch controller draws an overall current of ~40 μA from a 3.4 V supply. Finally, the RF ESD test was demonstrated using a handheld mini-zapper (KeyTek TPC-2A) with both human body model (HBM) and machine model (MM) inserts. The switch has successfully achieved a RF ESD rating of >4 kV and >500 V for the target ±2 kV HBM and ±200 V MM, respectively. Table 1 summarises the performance of prior published CMOS RF SPDT switches.

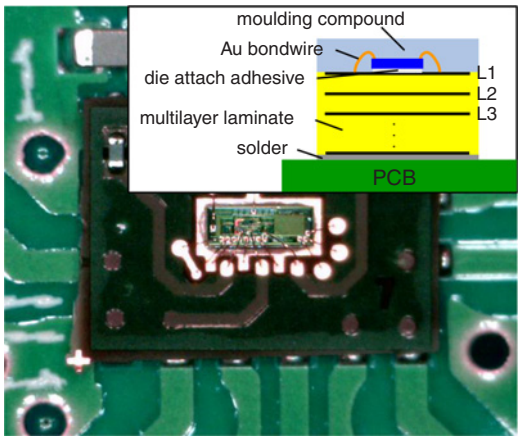

Fig. 4 *Packaged switch mounted on PCB*

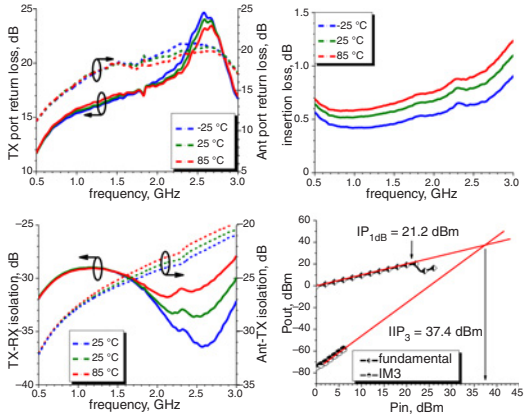

Fig. 5 *Measured RL, IL, and isolation at different temperatures and linearity characteristic of SPDT switch*

a TX port RL and Ant port RL
b IL
c Isolation
d IP_{1dB} and IIP_3 at 2.45 GHz

Table 1: Performance of prior published CMOS RF SPDT switches

Ref.	Process	Technique	Frequency (GHz)	IL (dB)	IPIdB (dBm)	IIP3 (dBm)	Package
This work[1,2]	0.18 µm CMOS	Resistive body-floating	0.9 2.45	0.52 0.78	21.7 21.2	38.3 37.4	MCM
[1]	0.5 µm CMOS	Low Rsub	0.9	0.73	18.9	38.2	SOIC
[2]	0.18 µm CMOS	Impedance transformation	0.9 2.4	0.97 1.1	26.3 22.7	37.7 29.8	SOIC
[4][3]	0.18 µm CMOS	LC substrate biasing	2.4	TX: 1.5 RX: 1.6	28.5	NA	On-wafer
[5]	0.18 µm CMOS	Resistive body-floating	2.4	0.7	21.3	30.3	On-wafer
[6]	0.13 µm CMOS	Body-floating and feed-forward caps	0.9	TX: 0.5 RX: 1.0	31.3	42	On-wafer

[1]Denotes SPDT switch with measured HBM (4 kV) and MM (500 V) ESD ratings
[2]Denotes SPDT switch with integrated switch control
[3]Denotes SPDT switch with measured HBM (4 kV) ESD rating

Conclusion: This Letter describes a highly integrated yet area-efficient CMOS RF SPDT switch. The switch achieves an IL of 0.52/0.78 dB and IP_{1dB} of 21.7/21.2 dBm at 0.9/2.45 GHz while satisfying the target RF ESD rating of ±2 kV HBM and ±200 V MM. To the best of the author's knowledge, this packaged CMOS switch has achieved the highest level of integration including the switch control and RF ESD protection among all reported to date.

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One or more of the Figures in this Letter are available in colour online.

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