

# Linear Power Amplifier Architectures and Its Packaging Technologies for New Generation Smart Phone Applications

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**Abstract** --- The design highlight of a power amplifier (PA) for 3G and beyond handset applications is to maximize its power-added efficiency (PAE) with specified linearity requirement at both peak and back-off power levels. In addition to PAE, its cost and size are of very important design considerations among others. The design principle of a linear PA with good PAE is summarized. An overview of different GaAs HBT handset linear PA architectures is presented. Pros and Cons of a single-ended PA and a balanced PA are discussed. The packaging technologies to realize low cost, small size and good performance for PA modules are illustrated. A tri-power mode PA module packaged in 3mm x 3mm x 1mm size is developed using Skyworks super efficiency at low power (SEAL) PA engine and advanced packaging technologies.

Index terms — Power amplifier, PAE, Linearity, and GaAs HBT.

## I. INTRODUCTION

The use of mobile communication devices is wide spread and has become an essential part of daily life. The PAs in mobile terminals are the major gating building blocks for ensuring a flawless connection between the handset and the base station. New generation (3G/4G) digital mobile communication systems require PAs with both high PAE and good linearity over a wide range of output power. Because PAs consume the majority of handset battery power, they are required to operate with high efficiency at different output power levels due to its dynamic output power change depending on their distance from a base station. In the meantime, the high linearity of the PA is needed due to the high peak to average power ratio of HSDPA/HSUPA or LTE modulations applied in 3G or 4G mobile systems. Generally, PAE and linearity work against each other. In other words, the improvement of the PAE of a PA is usually at the cost of trading-off its linearity and vice versa. For a linear handset PA in 3G and beyond, a

certain level of linearity is a prerequisite. A PA designer has to squeeze out the highest PAE with just enough linearity margin at each power level.

In addition to the requirements in electrical performance, PAs in handset applications must have small size, low cost and good thermal dissipation. Advanced packaging technology is essential to meet all these requirements.

## II. LINEAR POWER AMPLIFIER DESIGN AND ITS ARCHITECTURES

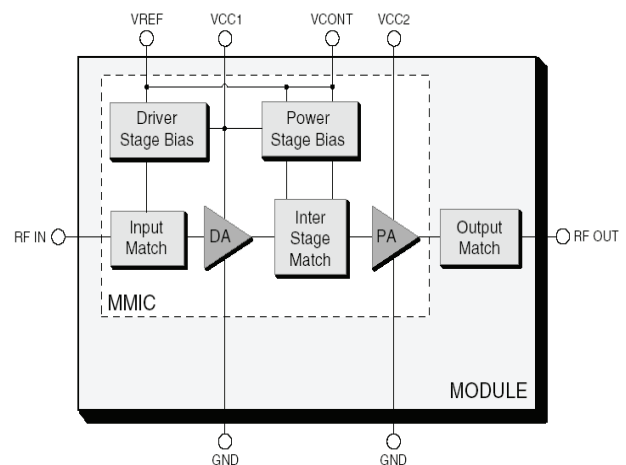
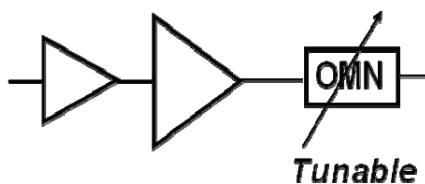


Fig. 1 The block diagram of a simplified two-stage handset linear PA

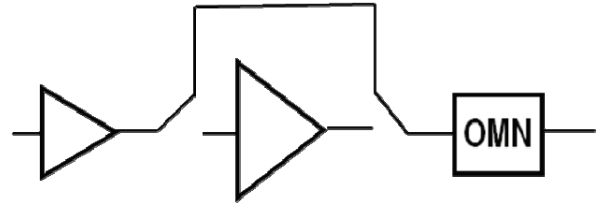
The block diagram of a simplified two-stage handset linear PA is shown in Fig. 1. Two main semiconductor technologies are available for PA design: III-V-compound-based technologies and silicon-based ones. To realize linear power amplifiers with good PAE, GaAs heterojunction bipolar transistor (HBT) with the emitter made of indium gallium phosphide (InGaP) is widely used as preferable technology. HBTs have excellent linear performance due to the cancellation mechanisms among their nonlinear sources [1]. GaAs HBTs also have high breakdown voltage, high gain, enhanced PAE, and superior ruggedness, which make them very competitive for low-cost handset PA applications.

PAs operating in different classes (class A to F) have different trade-offs between their efficiency and linearity. Linear handset PAs, if no linearization techniques are used, are usually selected to operate at class AB, which has better PAE than class A and better linearity than class B. With the PA set to operate in class AB, the PAE can be optimized by controlling load impedances and bias points at different power levels. The rule of thumb is that higher load impedances are required for lower output power levels to achieve good PAE at each power level. The enhancement of the PAE at backed-off power levels can also be achieved by lowering the quiescent current at these levels.

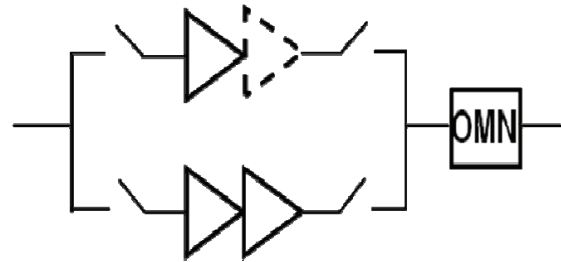
Many different PA architectures are employed to improve its PAE at different power levels. Fig. 2 illustrates some of these architectures. A lot of papers [2] through [5] have reported to achieve good PA performance such as high PAE and good linearity by using one of these architectures. They are classified as two categories: single-ended architectures and balanced ones. Fig 2 (a), (b) and (c) represent single-ended structures; while, Fig 2 (d) illustrates balanced structure. Balanced structure has its popularity on PA design since it has some unique features such as less load sensitivity, less sensitivity to load matching component variations and wider bandwidth compared with single ended one [6]. Moreover, one of the two branches in a balanced PA can be switched off without significant change of the insertion phase and gain. In other words, PAs operating in high power mode (with two branches on) and in low power mode (with one branch on only) have similar insertion phase and gain level if other conditions are maintained; while as, the single-end structure tends to have higher PAE at high power level (due to less output matching loss) and at low power levels (due to less loading impact from large PA side).



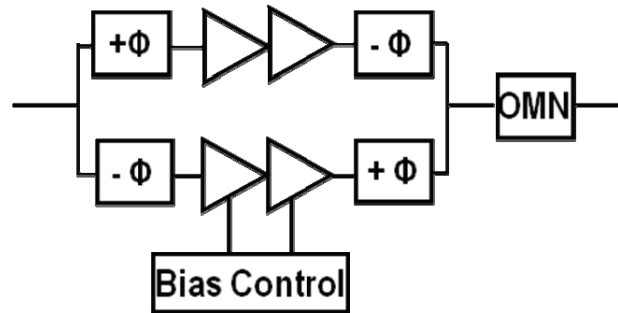
(a) A single-ended PA with tunable load



(b) A single ended PA with stage by-pass



(c) A single ended PA with pass selection



(d) A balanced PA with bias switch control

Fig. 2 different linear PA architectures (OMN represents output matching network)

### III. PACKAGING TECHNOLOGIES FOR PA MODULES

Single chip with QFN packaging is ideal for applications in low cost and small size PAs. However, on-chip output matching networks have high insertion loss and little tuning flexibility in the single chip solution. It is difficult to achieve the best PAE for PAs. Presently, the mainstream of PA vendors use multi-chip technologies for core PA die, PA logic control and bias supply die and RF switch die. All of these make the PA module packaging more complicated and challenging. Usually, output matching network is realized using multilayer ceramic substrates (LTCC or HTCC) or organic laminates with surface mounted (SMT) components. From the cost standpoint, organic laminates are better choice and little performance trade-off is seen. Fig. 3 shows the typical laminate packaging technology currently used for handset PA modules. The core PA die is usually attached on laminate substrate using

conductive epoxy and is connected through bond wires. It can also be flipped and solder-bumped so that it can be directly connected to laminate substrate like SMT components. RF switch die and/or PA logic control die are usually placed in parallel to the core PA die. One of the big challenges with multiple dies in parallel is that the module is very clumsy. In order to make the module compact and size competitive, RF switch die and/or PA logic control die may be placed on the top of the core PA die so that the PA overall module size can be reduced. Another big challenge for PA packaging is thermal dissipation since more than half of the DC consumed power from linear handset PA is converted to heat. In order to achieve good thermal dissipation, thermal enhanced vias are applied in the substrate underneath the PA die. Flip-chip assembly is claimed to have better thermal relief.

SMT components are used in the PA module for RF coupling, decoupling and DC blocking. The module is usually molded with plastic compound to cover PA die, bond wires and SMT components after it is fully assembled.

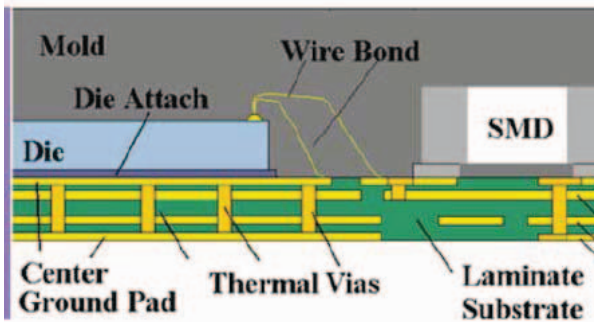


Fig. 3 Packaging technology illustration of a PA module

**IV. A TRI-POWER MODE LINEAR PA FOR WCDMA, CDMA2000, AND LTE MODULATION APPLICATIONS**

A 3x3mm<sup>2</sup> tri-power mode PA module (PAM) using Skyworks SEAL architecture with a high performance coupler was developed at the frequency range From 824 to 849 MHz for multi-mode WCDMA/CDMA2000/LTE applications. Fig. 4 illustrates the assembled PA module before the molding compound is applied. A core PA die was attached on multilayer organic laminate. An RF switch die was placed on the top of the PA die. The output matching network was partially realized off-chip for low insertion loss. The PAM was the combination of a PA with a true 50 ohm high performance coupler. The PAM was optimized for 3 power modes. An RF switch was applied to provide a different load-line for low and

middle mode. A reduced quiescent current ( $I_{cq}$ ) was used to further boost its PAE at low power mode. 41% of PAE at 28.25dBm in high power mode, 23% of PAE at 17dBm in middle power mode and 7% of PAE at 7dBm in low power mode were achieved at the frequency range from 824 MHz to 849 MHz with ACPR1 of minimum -48dBc under CDMA2000, -40dBc or better under WCDMA and better than -35dBc under LTE modulations. Fig. 5 shows the PAE of the developed PAM at different power levels and Fig. 6 shows its linearity performance. The coupler directivity is better than 24dB with 20dB coupling factor. The peak-to-peak coupler error is 0.3dB under 2.5:1 load VSWR. The RxBn is measured at -135dBm/Hz from 869MHz to 894MHz.

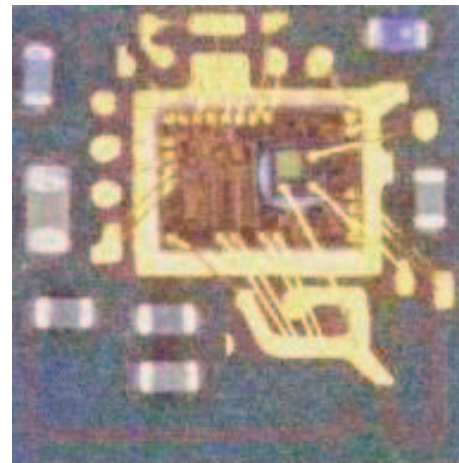


Fig. 4 A module assembly of a tri-power mode PA on the 3mm x 3mm multilayer organic laminate

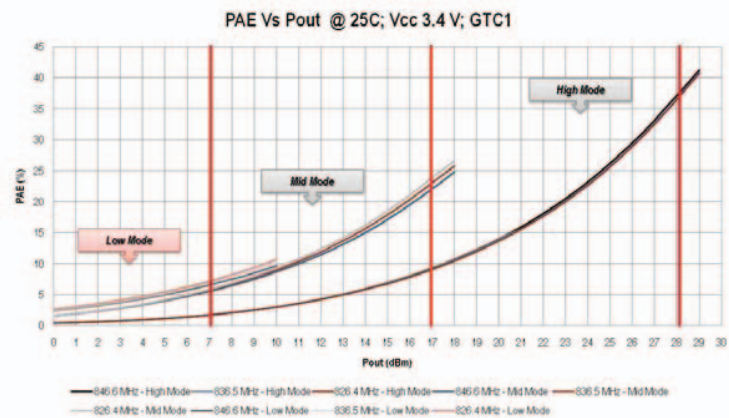


Fig. 5 PAE vs. Pout at three power modes from the developed PAM

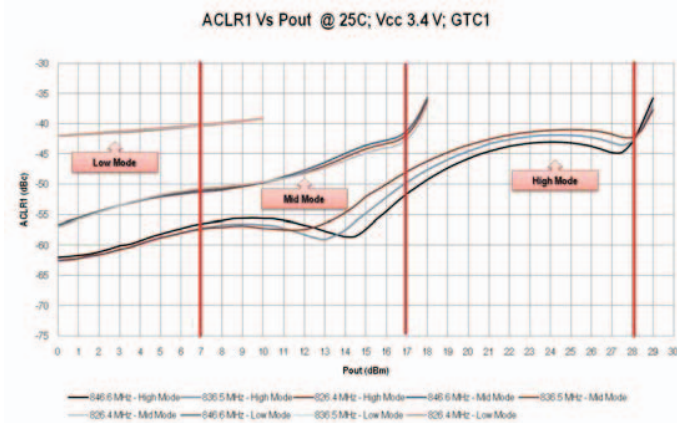


Fig. 6 ACPR1 vs. Pout at three power modes from the developed PAM

## V. SUMMARY

Because PAMs used in cellular phone handsets operate with a battery supply, a high PAE is essential for battery life. Linearity is also critical for 3G applications or beyond. Different PA structures were discussed compared to achieve good PAE for a linear PA module at different power levels. Advanced packaging technologies were briefed to develop low cost, small size and thermally effective PA modules. A tri-power mode PAM was developed using III-V compound technologies and a single-ended PA architecture. The module operated at the frequency range of 824 MHz to 849 MHz was realized in a molded multi-chip module (MCM) compact package. Decent PAE was achieved at three different power levels. The PA overall performance is very competitive in the current handset market.

## VI. ACKNOWLEDGEMENT

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