Optimized CMOS-SOI Process for High Performance RF Switches
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ABSTRACT
In recent years, CMOS on Silicon-on-Insulator has rapidly evolved as a mainstream technology for switches used in wireless applications. Since such applications can involve switching high power levels (35 dBm) at high frequencies (~2 GHz), the technology considerations are substantially different than those for SOI used in high speed, small signal applications such as microprocessors. This paper provides an overview of key technology challenges and trade-offs.

INTRODUCTION
In a wireless system, a front-end module (FEM) acts as an interface between the antenna and RF transceiver. An FEM typically consists of power amplifiers, switches, low-noise amplifiers, control circuitry, and passive elements. Traditionally, the ICs in a FEM are manufactured using technologies that provide best-in-class performance for the specific application; for example, pHEMT for switches.

FET OPTIMIZATION
A primary decision in FET optimization is channel length. As $R_{on}$ scales with channel length (Fig. 2), it would appear that a short channel length device would be a better solution for switch FETs. However, it should be noted that $C_{off}$ increases as a result of technology optimization (e.g. $C_{ox}$ due to gate oxide thickness scaling). As a result, the $R_{on}$*$C_{off}$ improvement reaches diminishing returns for scaling past ~0.25 μm.

SUBSTRATE OPTIMIZATION
The preceding section focused on two critical performance aspects of a switch; insertion loss and isolation. In this section, we will discuss the third aspect: linearity.

Fig. 3 plots voltage handling capability of a switch arm as a function of number of FETs. Due to substrate loss, this capability has diminishing marginal improvement as more and more FETs are stacked into a switch arm. Further, as more FETs are stacked, the resulting increase in parasitic capacitance actually degrades the overall switch performance. A stack height of 10-14 FETs is generally adopted to maximize the voltage handling capability without degrading isolation.

Typically, switches are designed in series-shunt configuration wherein series arms provide a low resistance path for the RF power that leaks to the OFF ports. For switches with a high throw count, large parasitic capacitance of OFF arms provides a leakage path for the RF signal, which translates into insertion loss for the ON arm.

There are several metrics of linearity such as harmonics ($2^{nd}$, $3^{rd}$), inter-modulation distortion (IMD), etc. Typical system specifications require that harmonics generated by the antenna switch are >70 dB (1 part in 10 million!) lower than the carrier signal. In addition to FET, SOI substrate plays a critical role in switch linearity.
We have characterized the role of substrate in Fig. 5 by monitoring RF signal loss into the substrate. These results track well with the C-V measurement on the buried oxide (BOX) capacitor [7]. A ‘non-linear’ substrate, for which BOX capacitance shows strong voltage dependence, results into non-linear loss as shown in Fig. 5. There are various techniques at substrate (e.g. ‘trap-rich’ region between BOX and handle wafer [8]) as well as wafer processing [9] level that are used to reduce the non-linearity. Such improved substrate linearity has demonstrated an improvement of >15 dB in IMD for the resulting switch. Based on our analysis, BOX capacitance contributes <5 percent to total $C_{\text{off}}$ in the thickness range of interest; 0.5-1 μm. As shown in Fig. 5, BOX thickness has minimal impact on loss, provided the substrate is linear.

Finally, resistivity of the handle wafer is a critical component. Combined with BOX, the handle wafer forms an R-C network. The resulting signal loss is important not only from an insertion loss standpoint, but it also results in unequal voltage drop across FETs in a switch arm [7]. Ensuring high substrate resistivity minimizes both these effects. Ensuring high resistivity (> 1KΩ-cm) for a fully processed wafer is essential to realize a high performance switch.

**CONCLUSION**

Linkage between switch performance (insertion loss, isolation, linearity) and technology components (FET, SOI substrate) was discussed. Trade-offs were highlighted and an optimized technology space was outlined to enable switches that can meet the challenging system requirements of today’s wireless applications.

**REFERENCES**


![Fig. 1: Benchmark of $R_{\text{on}}C_{\text{off}}$ for Various Switch Technologies](image)

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![Fig. 2: Scaling of $R_{\text{on}}$ (normalized) with Channel Length](image)

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![Fig. 3: Voltage Handling as a function of stack height](image)

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![Fig. 4: Limitation of technologies with different FoM](image)

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![Fig. 5: Impact of Substrate Linearity and BOX Thickness on RF Loss into Substrate](image)

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