

Automatic Hardware Reconfiguration for Current Reduction at Low Power in RFIC PAs

Nicolas G. Constantin, *Member, IEEE*, Peter J. Zampardi, *Senior Member, IEEE*, and Mourad N. El-Gamal, *Member, IEEE*

Abstract—This paper presents a novel hardware reconfiguration technique implemented in a dual integrated-circuit (IC) GaAs HBT power amplifier (PA) design and demonstrates reduced current and improved efficiency at low power. The method automatically reconfigures the hardware of an RF IC PA over a given power transmission. Hardware interfacing and synchronization from outside the PA is minimized, and automatic gain compensation upon hardware reconfiguration is achieved with minimal temperature-dependant calibration. The challenge of integrating such complex on-chip hardware functions in a GaAs HBT technology was circumvented by the introduction of a gating concept used in conjunction with envelope feedback, and careful tradeoffs between circuit complexity and performance. Designs that suit the on-chip integration of the technique in GaAs HBT or Si bipolar junction transistor technologies are described. Experimental data are reported to support the proposed method.

Index Terms—Efficiency, envelope feedback, GaAs, HBT, power amplifiers (PAs), reconfigurable.

I. INTRODUCTION

THE minimization of current consumption in RF integrated circuit (RFIC) power amplifiers (PAs) used in wireless communication equipment, thus increasing the power-added efficiencies (PAEs), is a critical design goal, due to its impact on battery charge lifetime.

The PAE of RF PAs operating at high transmitted power levels are significantly improved with design techniques that shape the output current and voltage signals in the time domain (e.g., [1]–[7]). However, it is also desirable to reduce the current (improving PAE) of RFIC PAs at low power levels [8], where RF voltage and current waveform shaping have less impact on PAE. Therefore, an efficiency improvement strategy that reduces current at low power, while still allowing the use of large-signal techniques (e.g., [2]–[7]) at high power, is valuable.

RF transistor array switching (ON and OFF) has been proposed to reduce current in RFIC PAs at low power levels (e.g.,

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N. G. Constantin is with the Department of Electrical Engineering, École de Technologie Supérieure, Montreal, QC, Canada H3C 1K3 (e-mail: nicolas.constantin@etsmtl.ca).

P. J. Zampardi is with Skyworks Solutions Inc., Newbury Park, CA 91320 USA (e-mail: peter.zampardi@skyworksinc.com).

M. N. El-Gamal is with the Department of Electrical Engineering, McGill University, Montreal, QC, Canada H3A 2T5 (e-mail: mourad.el-gamal@mcgill.ca).

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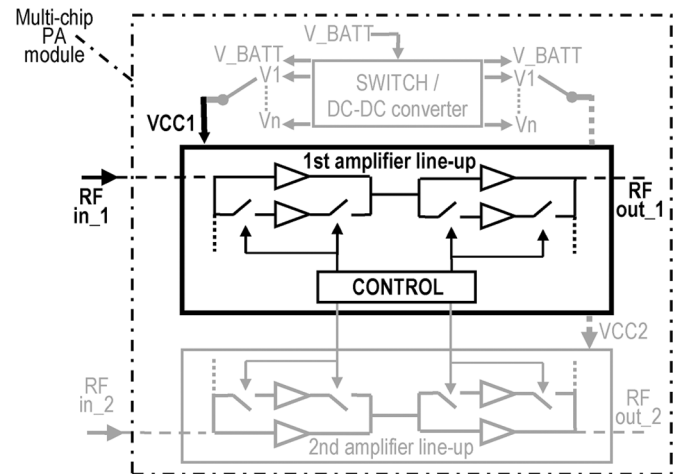


Fig. 1. Conceptual diagram illustrating the relevance of automatic hardware reconfiguration in RFIC PA modules.

[9]–[12]). Such large current reductions show the importance of circuit techniques for RF transistor switching in RFIC PAs. In this work, the concept of *automatic* RF transistor array switching as a function of power, together with automatic gain compensation, is introduced. The relevance of the automated feature for multistate RF transistor switching in one or multiple PA lineups in future wireless transceivers is highlighted in the conceptual diagram shown in Fig. 1.

A first RF amplifier lineup is built with sections of RF transistor arrays that are turned ON or OFF (symbolized by the series switches) and are biased with a supply line (VCC1) that may be switched among the battery voltage feed (VBATT) and the multiple outputs of a dc–dc converter (V1 to Vn) to improve PAE. As the number of RF transistors and VCC1 states increases (along with the number of discontinuities in the amplifier gain), automatic switching and gain compensation becomes attractive, especially for minimizing the amount of hardware interfacing for control and for gain compensation.

This paper investigates an RFIC PA structure and CONTROL circuit block for the amplifier lineup shown in Fig. 1 (highlighted with dark lines) using automatic RF transistor switching and gain compensation. We targeted single-chip integration using GaAs technology, which offers RF advantages in the personal communication system (PCS) band [13], but were limited by integration capabilities. Accordingly, we focus on circuit techniques that suit pure GaAs HBT integration and perform these relatively complex automated functions up to power levels where the AM–PM distortion levels still allow meeting linearity specifications (e.g., with CDMA2000 [14] excitation

in this work). Note also that, while it is beyond the scope of this paper, combining digital pre-distortion (DPD) (e.g., [4]) with our circuit techniques would allow further extension of the applicable power range where the linearity specifications are met. The feasibility of sharing the same CONTROL block (Fig. 1) for a second PA lineup (shown in gray) or multiple PA lineups was considered since this reduces the overhead of the added circuitry on overall size and cost. The applicability of our technique in conjunction with large-signal PAE improvement techniques was also evaluated.

The concept was presented in [15] and a distortion estimation method related to this technique was presented in [16], but no details on the circuit techniques were reported and only limited analyses of its potential were presented. In Sections II and III, we highlight the advantages of the method and further detail the concept. In Section IV, we describe a full on-chip GaAs HBT implementation of the method and address the important AM-PM consideration. We present experimental results and discuss the potential of the technique in Section V.

II. STATE-OF-THE-ART AND THE PROPOSED METHOD

In previously proposed methods for RF transistor array reconfiguration (e.g., [9]–[12]), external digital control lines are used to minimize current consumption by reconfiguring the PA to reduce quiescent current, or completely shutoff arrays, as the average transmitted power level is lowered. Drawbacks of these methods include: 1) increased number of external control lines as the number of hardware states increases; 2) synchronization of state activation from outside the PA; and 3) demanding temperature-dependant gain calibration requirements, since a typical-behavior lookup table of gain correction factors may not be sufficient to compensate for large and nonlinear gain perturbations that occur upon hardware reconfiguration. These must be compensated for in CDMA transmitters [14].

In this paper, a new technique called *gated* envelope feedback (GEF) [15], [16] is presented to reduce current at low power levels by automatically switching RF transistors, while addressing the three limitations above. In particular, it theoretically allows for automatic switching between any number of hardware states within a given power range with a *single* external control line, together with automatic gain compensation. Besides, in theory, envelope feedback automatically compensates the gain against AM-AM perturbations (e.g., with a dc-dc converter, Fig. 1), without extra hardware, digital processing, and the associated currents as with DPD. Hence, combining GEF with DPD allows shutting off such DPD functions at very low power.

The proposed method is based on a novel hardware gating concept using on-chip circuits that condition the operation of envelope feedback [1] at low power (i.e., where AM-PM distortion levels still allow meeting CDMA linearity specifications) through the CONTROL block of Fig. 1. This concept's key benefit is that it restricts the requirement for envelope feedback performance optimization to only a limited power range, drastically reducing circuit complexity. This enables full on-chip integration (except for a few LC components) in a dual-IC GaAs HBT solution with only 1.4 mm² of die area, and single-chip integration is foreseeable.

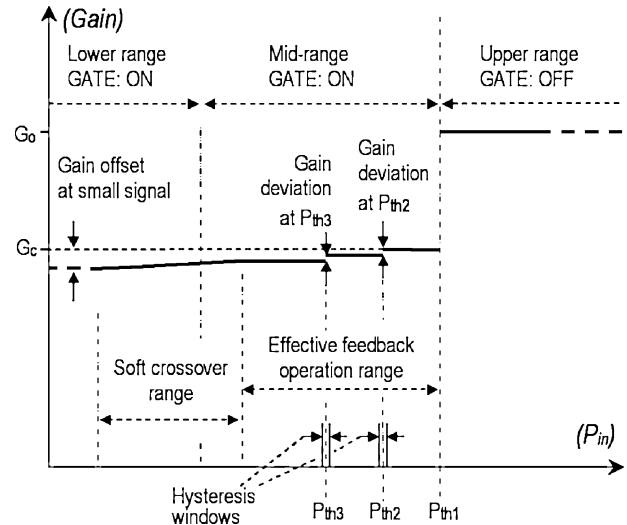


Fig. 2. GEF concept illustrated on a gain versus average input power curve (from [15]).

Besides cellular handset applications, the method is also attractive for standalone RFIC PAs used in other transmitters with limited PA control and requiring minimum calibration.

III. GEF CONCEPT AND ARCHITECTURE

Fig. 2 illustrates the GEF concept applied to an RF amplifier on a gain versus input power (P_{in}) curve. A continuous wave (CW) excitation is assumed.

At high P_{in} , the external GATE control signal is at logic OFF. The envelope feedback circuitry is disabled and the full gain, G_o , is available. As P_{in} decreases to P_{th1} threshold in Fig. 2, the GATE signal is enabled, turning ON the envelope feedback circuitry. In this second mode, the gain is forced to a value G_c lower than G_o , and ideally, independent of temperature, as per the feedback characteristics. This gain reduction at low power is desirable, as it reduces transmitter noise [8]. Activation of the GATE signal at P_{th1} may also be used to reconfigure part of the PA's on- and off-chip hardware to reduce the current (e.g., the biasing and the output impedance matching circuitry).

As P_{in} further decreases past P_{th2} , on-chip hysteresis comparators automatically set a third hardware condition by turning OFF a section of the amplifier's output stage to reduce current consumption. The gain variation from turning off transistors is theoretically cancelled through the envelope feedback, maintaining the gain at $\sim G_c$. Similarly, as P_{in} crosses below P_{th3} , a fourth condition is automatically set with a section of the amplifier's driver stage turning OFF with the gain still $\sim G_c$.

As P_{in} further decreases, the nonlinear gains of the envelope detectors (within the envelope feedback circuitry) with respect to the power of the RF signal also decrease. The design of the detector circuitry (discussed in Section IV-A) avoids sharp gain variations in the RF to analog conversion gain profiles so that the overall feedback loop gain decay has a limited rate of change toward near zero for small signals. This results in a soft crossover (Fig. 2) from closed-loop operation to open-loop mode (i.e., with no feedback loop gain) in the lower range and effectively acts to gate off the envelope feedback, although the

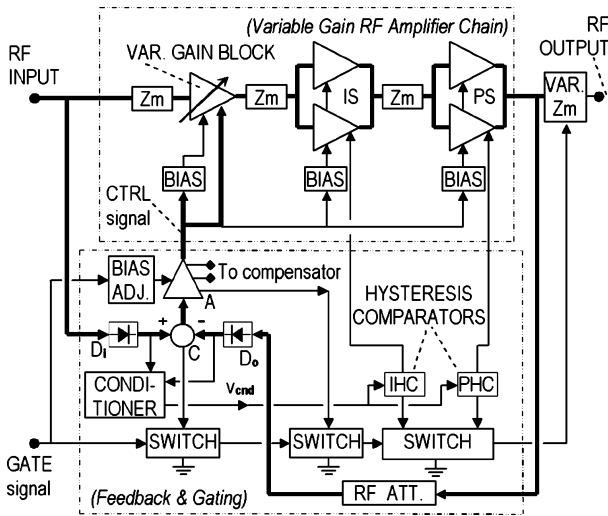


Fig. 3. Block diagram of the GEF implementation in a dual GaAs HBT IC solution: the RF amplifier IC, and the feedback and gating IC (from [15]).

GATE signal is still ON. Minimizing the gain variation as a function of input power to achieve a soft crossover is critical for meeting the linearity requirements for envelope varying excitations (e.g., CDMA). While we only considered three hardware conditions below P_{th1} here, the method theoretically allows for automatic switching between any number of hardware conditions within the effective feedback operation range, which corresponds to an effective gating ON condition between P_{th1} and the upper edge of the soft crossover range (Fig. 2) using only one control line. At small signals, the gain offset (Fig. 2) can be minimized through direct control of the gain of the PA.

Gain variations over temperature are automatically cancelled through feedback within the effective feedback operation range. Since no hardware reconfiguration takes place outside of this range, lookup tables with temperature-dependant gain correction factors are sufficient. Hence, our method requires only three measurement points at room temperature, corresponding to the three ranges of Fig. 2, for transmitter gain compensation.

For envelope varying excitations (e.g., CDMA), the threshold levels discussed above use the *average* RF input power (P_{in-ave}). Hysteresis functions (Fig. 2), as well as filtering capacitors used in sequential logic circuits, are necessary to prevent the triggering of hardware reconfiguration by the instantaneous envelope of the signal, which would cause excessive distortion. Hence, automatic reconfiguration is triggered only when the slow varying average power level crosses the P_{th2} and P_{th3} thresholds. Assuming good gain regulation, this has negligible effects on the transmission.

Since the envelope feedback and control circuitry are shut OFF when the GATE is OFF, large-signal efficiency improvement techniques (e.g., [2]–[7]) can still be used in this hardware state.

Fig. 3 shows the block diagram of the designed 1.88-GHz CDMA GaAs HBT GEF PA (which corresponds to the first amplifier lineup and the CONTROL block in Fig. 1). A dual IC solution (i.e., a variable gain RF amplifier IC and a feedback and gating IC) was selected to facilitate the investigations. The envelope signal path is highlighted with thicker lines. The forward

path includes an input envelope detector D_i , an envelope comparator C, an analog error amplifier A, and a three-stage variable gain RF amplifier chain. The gain of the amplifier chain is controlled through a variable gain stage (VAR. GAIN BLOCK), and is a function of the amplified error signal (CTRL signal). This signal is also used to control the biasing of the three RF stages for enhanced gain control dynamic range.

The feedback path includes an RF attenuator (RF ATT.) followed by the output envelope detector D_o . A conditioner circuit provides buffering and voltage scaling between the reference envelope signal delivered by D_i and the two hysteresis comparators (IHC and PHC), and also minimizes the voltage offset between the inputs of the error comparator C. The hysteresis comparators provide the necessary threshold detection (P_{th2} and P_{th3} in Fig. 2) and sequential logic for automatically switching ON or OFF sections of the RF transistor arrays in the intermediate stage (IS) and in the power stage (PS), for current reduction purposes.

The input and inter-stage *LC* impedance matching (Z_m) are realized on chip. The off-chip output matching (VAR. Z_m) is designed in this work to maximize efficiency while meeting CDMA linearity specifications at large signal (GATE OFF), using well-known matching techniques for class AB amplification [1]. As shown in Fig. 3, it could be electronically reconfigured at low power when the GATE is switched ON. However, to simplify the experiments, VAR. Z_m in this work is a load-pull tuner that is manually controlled based on the GATE state. The switch circuits shut off most of the feedback and gating circuitry for minimum current when the GATE is OFF.

IV. CIRCUIT DESCRIPTION AND SIMULATION RESULTS

A. Description of the Envelope Detector Circuits

The roles of the envelope detectors in a GEF amplifier are to sample the input and output envelope (as illustrated in Fig. 3) and to shape the gain profile of the crossover range (Fig. 2). As a key benefit from the gating approach, the requirements for large enough detector conversion gain and feedback operational dynamic range over power are restricted to the effective feedback operation range only (Fig. 2). This enables the use of far simpler on-chip envelope detector circuit topology than other proposed topologies for RFIC PAs (e.g., in [17], where patented precision RF detectors are used). Minimizing the on-chip cells allows a compact detector integration in GaAs HBT. A drawback, however, is the strong nonlinear response with this simple topology. Fig. 4 shows the schematic of the input and output RF envelope detectors and the error comparator that were implemented.

The nonlinear RF to analog conversion gain profiles of the input and output detectors (built with Q1, Q2) are dependent on self-biasing as is typical of transistors operated in class-AB [1], and are mainly determined by the transistors' quiescent currents and the resistor values of the diode-resistor nonlinear loads in their collector circuitry. The detected envelope voltage signals at the collectors of Q1, Q2 are filtered by R11, C3, L3 and R12, C4, L4, and then applied to the envelope error comparator circuit. These transistors are biased with the same on-chip regulated dc source (~ 1.35 V) for improved symmetry, which favors matched detector performances.

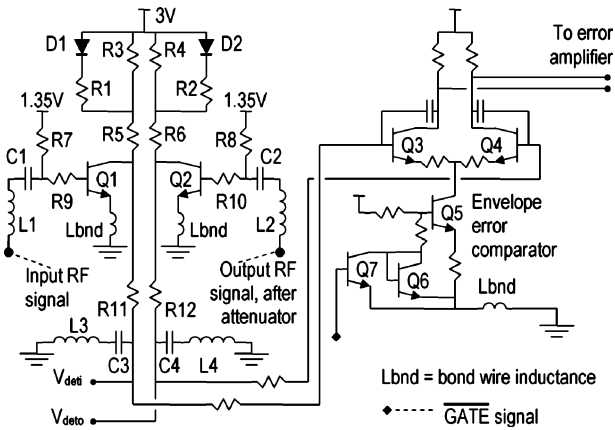


Fig. 4. RF envelope detectors and the error comparator (from [16]).

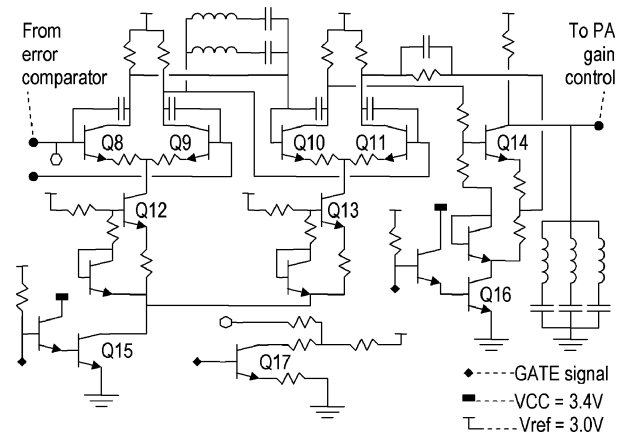


Fig. 6. Schematic of the analog error amplifier.

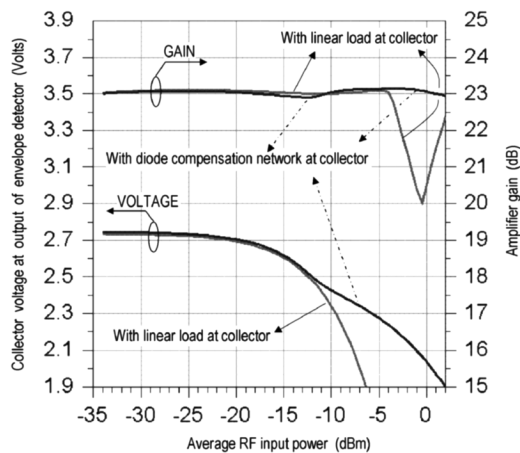


Fig. 5. Simulated conversion gain and dynamic range of the envelope detector, and closed-loop gain of the GEF amplifier system.

As the RF input power level reaches a threshold of ~ -12 dBm, the voltages across R3 and R4 turn on D1 and D2, providing nonlinear compensation as a function of power.

The simulated envelope voltage at the collector of Q1 and closed-loop gain of the amplifier system are shown in Fig. 5 for two cases with: 1) a purely resistive (hence, linear) collector circuitry and 2) the nonlinear compensation mechanism described above. In the first case, the rapid drop of the detected envelope signal over the power axis results in transistor saturation in the envelope error comparator and collapses the closed-loop gain at ~ -4 dBm and above. In the second case, the nonlinear compensation reduces the conversion gain above ~ -12 dBm, which results in adequate feedback operation beyond $+2$ dBm. Thus, for the same detected voltage swing between 2.5–1.9 V, the usable dynamic range of P_{in} as an effective feedback operation range is improved by ~ 8.5 dB. By restricting the switching of D1 and D2 to the 14-dB effective feedback operation range only (i.e., from ~ -12 to $+2$ dBm), the associated gain variation is kept below ~ 0.3 dB.

The high-impedance ($\sim 250 \Omega$) wideband *RLC* matching networks at the bases of Q1, Q2 were designed for 1.88 GHz, but can be adjusted to allow use of the same CONTROL block in a

multiple PA lineup implementation, as shown in Fig. 1 (e.g., for cellular and PCS bands).

The differential envelope error comparator (Q3, Q4 in Fig. 4) may be shut off for minimum current consumption with the help of transistor Q7 when the envelope feedback operation is disabled, with GATE OFF in Fig. 2.

B. Error Amplifier and the Phase Compensator

The error amplifier (block A in Fig. 3) contributes most of the feedback loop gain, and provides envelope gain and phase compensation for stability. The circuit used (Fig. 6) is designed to operate linearly (without voltage clipping or transistor saturation), but only within the small signal, the crossover, and the effective feedback operation ranges (Fig. 2). Limiting this operating range stems from the GEF approach, and allows the implementation of the error amplifier and its switch circuitry (Q15, Q16) using 1.35-V VBE NPN transistors. The error amplifier can be shut off with the GATE signal OFF.

The three differential-input stages (Q8–Q11 and Q14) are designed with low quiescent current levels, but still provide desensitization of the PA gain control signal (CTRL in Fig. 3) against voltage fluctuations across the switches (Q15 and Q16). The dc through Q17 is controlled with the 1.5–2.8-V range of the GATE signal, and allows adjustment of the dc voltage of CTRL to set the PA's small-signal gain.

Off-chip *LC* resonators (~ 8 – 100 MHz) form a passive phase compensator for stability and transient performance. The performance criteria targeted a maximum steady-state gain deviation of 0.15 dB upon reconfiguration of IS and PS in Fig. 3 at the P_{th2} and P_{th3} thresholds (Fig. 2). This compares favorably with the 0.5-dB precision specification for incremental power control steps for CDMA mobile terminals [14]. The required open-loop gain in static conditions was found, by simulation, to be 36 dB.

The simulated loop gain and phase response of the GEF amplifier system showed a phase margin of 38° at the 0-dB gain crossing (~ 15 MHz), which is adequate for stability and transient performance. The simulated closed-loop operation (at ~ 23 -dB gain, Fig. 5) gave a 3-dB cutoff frequency that is above the CDMA2000 1.23-MHz channel bandwidth (~ 3 MHz).

While the use of off-chip *LC* resonators for this pure GaAs HBT GEF implementation was sufficient for CDMA2000, a

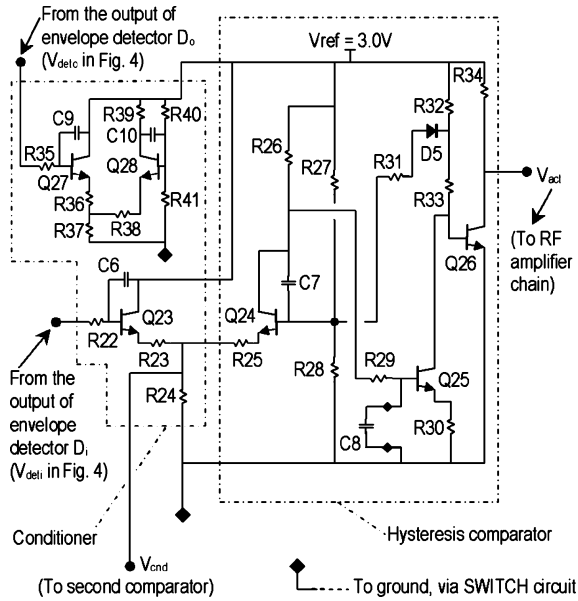


Fig. 7. Schematic showing the signal conditioner and only one of the two similar hysteresis comparators.

much larger loop bandwidth is required for W-CDMA. Note that in the context of a multitechnology PA module, a CMOS implementation of the CONTROL block (Fig. 1) allows higher performance op-amp-based active phase compensators, providing much larger loop bandwidths.

C. Envelope Signal Conditioner and the Hysteresis Comparator Circuits

The envelope conditioner (Fig. 3) provides buffering to the detected input envelope signal and scales its range to levels within the full input voltage range of the hysteresis comparators (IHC and PHC). It must minimize any voltage perturbation generated between the inputs of the error comparator as a result of hardware reconfiguration. IHC and PHC must trigger the reconfiguration of the IS and PS stages (Fig. 3), but only when the P_{in_ave} crosses the P_{th2} and P_{th3} thresholds (Fig. 2).

Such functions are relatively complex for integration in a pure GaAs HBT technology. The circuit topology used in our design (Fig. 7) is innovative in this regard since it allows a full GaAs HBT on-chip implementation with few components, use of an unregulated 3-V supply voltage and grounding via NPN switches (Fig. 3), and use of only 1.35-V V_{BE} NPN transistors.

The detected envelope signal is conditioned by Q23, R23, and R24 and the resulting V_{cnd} signal triggers the hysteresis comparators at the P_{th2} and P_{th3} average power thresholds (Fig. 7 shows one of the two comparators).

The V_{cnd} signal is compared to the comparator's reference potential, primarily set by the R27 and R28 divider, the V_{BE} of Q24 and the conduction state of D5. When P_{in_ave} is high, the V_{deto} signal at the output of the input RF detector D_i is low and Q23 is OFF. Q24 is then biased, and its low collector voltage results in D5 being OFF and Q26 saturated (V_{act} low), corresponding to the hardware state where all RF transistors are active in the PA.

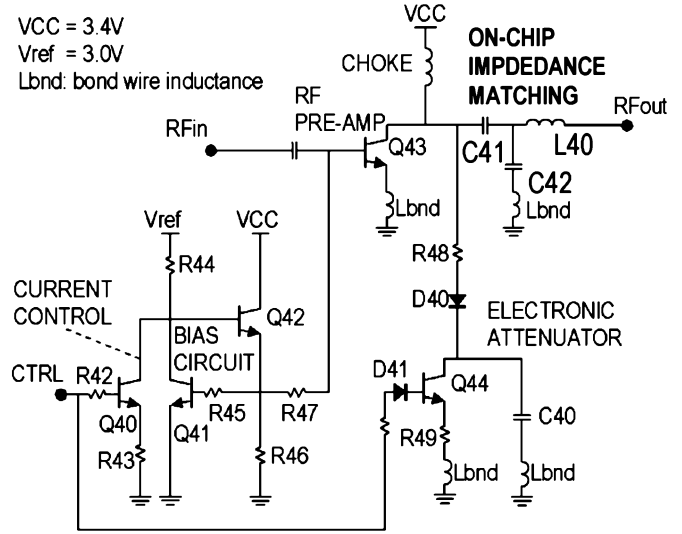


Fig. 8. Schematic of the variable gain block.

When P_{in_ave} decreases, requiring hardware reconfiguration, V_{deto} turns Q23 on and Q24 off, turning D5 on and Q26 off (V_{act} high), corresponding to the hardware state where half the RF transistors in the intermediate stage or the power stage (IS or PS in Fig. 3) are active.

The state of D5 changes the comparator reference potential by ~ 93 mV in this design, giving ~ 2 dB of hysteresis window in the RF power domain for both power thresholds (P_{th2} and P_{th3} in Fig. 2). This 2-dB window and the time constant of the off-chip capacitor C8 (Fig. 7) ensures that the reconfiguration mechanism is triggered only by the slow varying average input power, and not by the CDMA instantaneous envelope power or any undesired transient signal in the control circuitry.

The circuitry surrounding Q27, Q28 is a dummy load for the V_{deto} signal (Fig. 4) and replicates the switching load on the V_{deto} signal. This minimizes the voltage perturbations between the inputs of the error comparator.

D. Variable Gain Block

The variable gain block (VAR. GAIN BLOCK in Fig. 3) provides most of the dynamic range in the gain control of the RF amplifier chain, for the feedback operation. The circuit topology used is shown in Fig. 8, and provides a good compromise between simplicity, for on-chip integration, and a maximum dynamic range performance for the gain control. Note that the ability to make this design tradeoff stems from the key GEF characteristic—the need for feedback performance optimization *only within* the effective feedback operation range. This alleviates the dynamic-range requirement.

The RF pre-amplifier transistor (Q43) is biased by a current mirror circuit (Q41, Q42). An on-chip output impedance-matching circuit (C41, C42, L40) ensures maximum power transfer at 1.88 GHz to the following stage (i.e., IS in Fig. 3). The RF pre-amplifier gain is varied using a reflective electronic attenuator (R48, D40, Q44, R49, and C40), which is controlled by the feedback error signal CTRL (Fig. 3). The gain control dynamic range is further improved by simultaneous adjustment of the bias current to Q43 through the current mirror

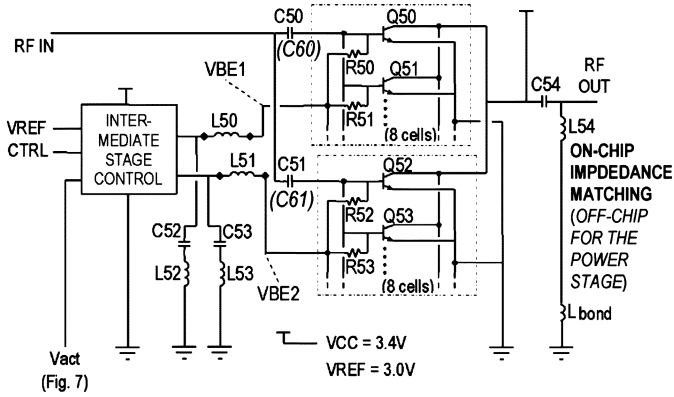


Fig. 9. Schematic illustrating the coupling and the switching of the RF transistor arrays in the intermediate stage (similar for the power stage).

(with the help of Q40), and the biasing currents in IS and PS as a function of CTRL, shown in Fig. 3. Simulation shows that the overall gain control range is limited (i.e., ~ 9 dB at P_{in} levels below -4 dBm and ~ 3 dB at $+2$ dBm), but is sufficient for the GEF operation to ensure proper feedback operation within the effective feedback operation range only (from -12 to $+2$ dBm).

E. Coupling and Switching of the RF Stages

Fig. 9 shows the coupling of the two RF transistor array sections in the intermediate stage (IS in Fig. 3), and the interfacing with the control circuitry.

While the GEF architecture allows the use of unequal array sizes, this design uses two equal size sections. Each section is made up of eight transistors of emitter area (A_e) = $56 \mu\text{m}^2$. The two sections are dc isolated at their inputs with on-chip 10-pF capacitors (C50 and C51), and are symmetrically driven with the RF signal (RF IN) delivered by the variable gain block (Fig. 8). Independent base-emitter dc signals (VBE1 and VBE2) are provided by a control circuit that is part of a current mirror bias circuit (not shown). When the activation signal V_{act} from the hysteresis comparator (Fig. 7) is set at logic high upon hardware reconfiguration, the VBE2 dc signal is pulled down to completely shut off the corresponding RF transistor array section (including Q52, Q53). Off-chip inductors (L50, L51) and on-chip LC notch filters (L52, C52 and L53, C53) desensitize the bias and control circuitry against RF signals, and small damping resistors at the base of the RF transistors (including R50, R51, R52, R53) improve stability. An on-chip matching circuit (C54, L54) ensures a maximum power transfer to the power stage when all RF transistor array sections in the amplifier chain are enabled. Direct paralleling of these sections was used to reduce die size. On-chip power combining would require further research work.

The same topology is used for the switching and coupling of two RF transistor arrays in the power stage (PS in Fig. 3). Each array is made up of 48 (A_e) = $56 \mu\text{m}^2$ RF transistors with the equivalent of two 12-pF on-chip capacitors coupling their inputs (C60, C61 in Fig. 9), but split into two groups of 48 0.25 pF in series with the RF transistor bases.

Simulation shows that the PAE decrease when RF transistor sections are shut off at low power, due to the nonoptimum inter-

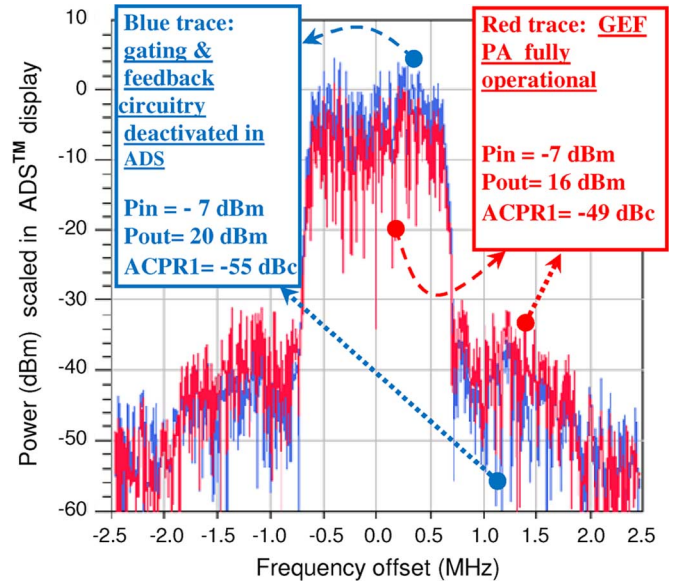


Fig. 10. Simulated ACPR1 with: in blue (in online version), the gating and feedback circuitry deactivated in ADS and in red (in online version), the GEF PA fully operational.

stage impedance matching (since Z_m blocks in Fig. 3 are optimized for full periphery operation) is offset by the PAE increase resulting from the shutting off of these array sections.

F. AM-AM AM-PM Distortion Due to Envelope Feedback

Although envelope feedback is known to exhibit AM-PM distortion (in particular, at large signal) [1], restricting its operation in a GEF PA up to some power level allows exploiting the adaptability and automation features that are inherent to feedback, while maintaining AM-PM distortion levels that allow meeting CDMA2000 linearity requirements.

Fig. 10 shows the simulated adjacent channel power ratio (ACPR) linearity performance of this PA with a 1.88-GHz CDMA2000 excitation in two cases: 1) with the entire feedback and gating circuit block (Fig. 3) shut off (by pulling the GATE signal at logic low) and 2) with the GEF amplifier fully operational. In both cases, the P_{in} level was set to -7 dBm. While a 6-dB ACPR degradation accompanies envelope feedback operation, the resulting -49 -dBc performance (compliant with the -42 -dBc CDMA2000 specification) at 16-dBm output power supports the applicability of envelope feedback at these levels. This is also consistent with the simulated AM-AM and AM-PM curves presented in Fig. 11 for different hardware conditions (i.e., 1) both the intermediate stage (IS) and the power stage (PS) fully operational and 2) half the RF transistor arrays in both these stages shut off) and over a wide temperature range. These curves show that at any given temperature, the worst case gain and phase variations during GEF operation at these power levels remain minimal in the different hardware states (e.g., less than 0.4-dB gain variation and less than 7° phase variation over a 17-dB power range at -25°C). Using well-known PM modulation formulations, it may be shown that such phase variations introduce sideband power levels that are well below the adjacent channel power levels shown in Fig. 10. Hence, these curves also support the applicability of

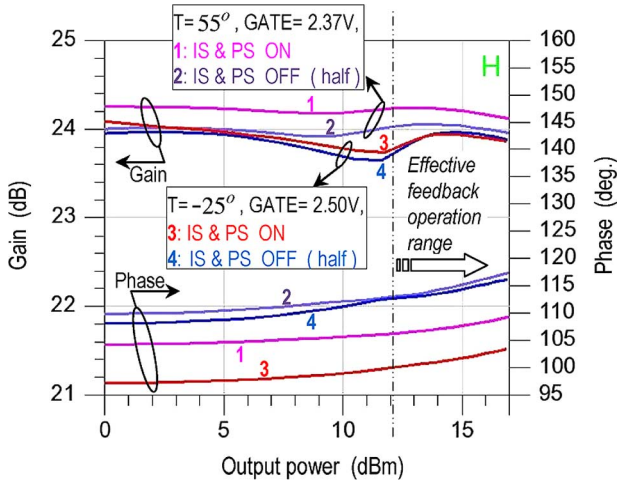


Fig. 11. Simulated gain and phase variations during GEF operation at -25°C and 55°C , and in two different hardware states: with the intermediate stage (IS) and the power stage (PS) ON and with half the RF transistor arrays in both these stages shut off.

envelope feedback at these output power levels. Combining this technique with a DPD implementation, as mentioned in Section I, provides extra margin for linearity and extends the applicable power range.

G. Gain Regulation

The gain curves in Fig. 11 also demonstrate the automatic gain compensation capability of the technique over temperature, as discussed in Section III. When switching between the two hardware states which are considered in Fig. 11 within the effective feedback operation range (~ 12 -dBm output power and above), the gain variation over temperature is maintained within 0.5 dB. Note that at one given temperature (e.g., at 55°C , in the worst case), the reconfiguration of both stages simultaneously translates into less than 0.25 dB of gain variation. In the practical application where one stage at a time is reconfigured at a given temperature (Fig. 2), the 0.15-dB gain deviation specification stated in Section IV-B is met.

V. EXPERIMENTAL RESULTS

A. On-Chip Implementation

Photographs of the variable gain RF amplifier IC and of the feedback and gating IC are shown in Figs. 12 and 13.

The circuit sections defined in Fig. 3 are located on the pictures with the inter-stage impedance matching components of Figs. 8 and 9 labeled with their respective reference designators. Both ICs were designed in an NPN only Skyworks Solutions Inc. 47-GHz f_T GaAs HBT process offering TaN thin-film resistors ($50\ \Omega/\text{square}$). The total area used, excluding the test signals and redundancies in electrostatic discharge (ESD) protection and bond pads, is $1.4\ \text{mm}^2$. We estimate that this may be reduced to $1.3\ \text{mm}^2$ using a more compact layout and semiconductor layer resistors ($\sim 600\ \Omega/\text{square}$).

B. Automatic Gain Compensation

The measured gain achievable with the RF amplifier chain alone (i.e., with GATE in Fig. 3 turned OFF) was ~ 25 dB at

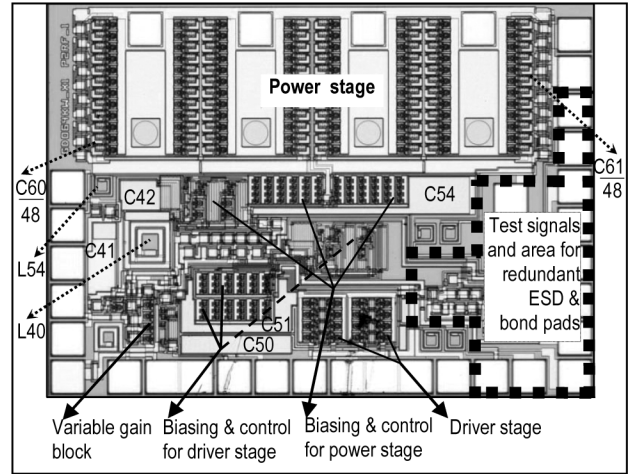


Fig. 12. Photograph of the GaAs HBT RF amplifier chain IC. The effective die area used is $1.07\ \text{mm}^2$ (from [15]). See reference designators in Figs. 8 and 9.

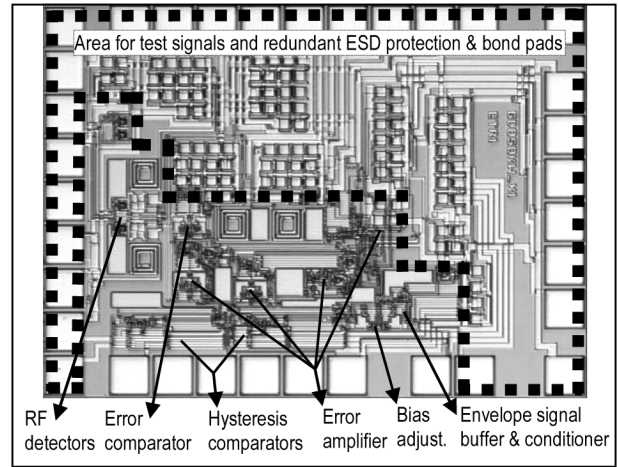


Fig. 13. Photograph of the GaAs HBT feedback and gating IC. The die area used for the gating and feedback circuitry is $0.328\ \text{mm}^2$ (from [15]).

1.88 GHz. However, all of the following reported measurements were performed after manually setting the output matching (VAR. Z_m in Fig. 3) in a fixed condition as part of a compromise to circumvent RF instability conditions, met during the experimentations, while maintaining sufficient gain (~ 20 dB) in the RF amplifier chain at power levels below ~ 20 dBm. This yielded proper feedback operation with GATE ON and with the closed-loop GEF PA gain experimentally adjusted to ~ 16 dB.

These RF instability conditions were caused by too much common-mode inductances in the multiple PA grounding paths and also by too much coupling between the multiple supply feeds of the three-stage PA chain. This was a result of the longer than usual bond wires and printed circuit board (PCB) traces that were required in the actual implementation of our dual-IC design in order to provide extensive test capabilities on each RF stage separately and on various feedback and gating circuit blocks. However, simulation shows that very good RF stability can be achieved over the full voltage range of the CTRL envelope feedback signal (Fig. 3) in the different hardware states of the PA. RF stability can therefore be achieved independently of the envelope feedback, gating, and RF transistor switching

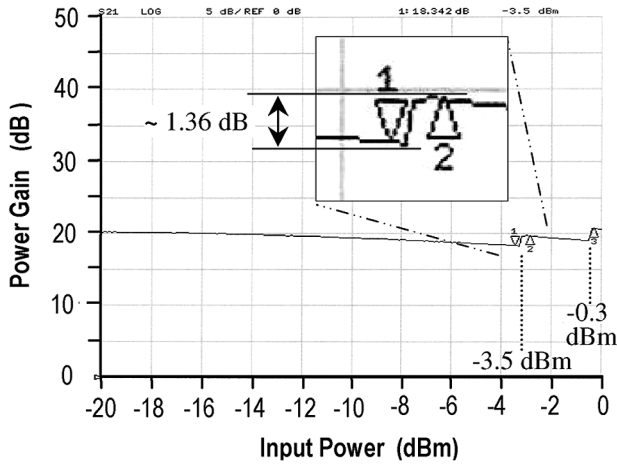


Fig. 14. CW amplifier gain versus P_{in} measured with a vector network analyzer, with the automatic hardware reconfiguration circuitry enabled, but with the envelope feedback compensation manually disabled (from [15]).

mechanisms. Hence, we believe that the design of a GEF PA in a single-chip implementation and with no such test facilities would not require the performance compromise stated above.

Fig. 14 shows the results of a CW gain measurement obtained from this GEF implementation when the GATE signal was ON, automatically reconfiguring the hardware of the power stage at $P_{in} = -3.5$ dBm (P_{th3} in Fig. 2), and the intermediate stage at -0.3 dBm (P_{th2} in Fig. 2), but with the envelope feedback intentionally disabled (i.e., CTRL in Fig. 3 set at a constant voltage).

The results demonstrate proper automatic reconfiguration at these two power thresholds by the PA, and that without envelope feedback compensation, large gain deviations of ~ 1.36 dB are observed. Such gain deviations are unacceptable for CDMA [14] (deviations up to 1.8 dB were reported in [9]).

Fig. 15 shows the CW gain under similar conditions as for Fig. 14, but with the envelope feedback enabled (CTRL in Fig. 3 connected to the error amplifier). We see that the 1.36-dB gain deviation, normally observed around -3.5 dBm without gain compensation, is reduced to only 0.27 dB, demonstrating the automatic gain compensation feature of the GEF technique. Moreover, over the full P_{in} range, the gain variation (estimated from the simulation in Fig. 5 at ~ 0.3 dB) is less than 1 dB.

Note that simulation shows a gain variation of less than 1.5 dB and a return loss greater than 15 dB across the PCS band (1.85–1.91 GHz) during envelope feedback operation at all power levels from the small-signal range to the effective feedback operation range (Fig. 2).

C. Current Reduction in an Automated Fashion

Two cases with a CW input excitation are shown in Fig. 16 that further demonstrate the potential of this proposed technique: 1) with the hardware reconfiguration and the envelope feedback circuitry disabled (GATE OFF) and 2) with the circuitry enabled (GATE ON). The current reduction in the case of enabled hardware reconfiguration is entirely automated, which provides important advantages discussed in Section II. The current values for output power between 5–12 dBm on the lower curve correspond to the hardware state where half the RF transistor arrays

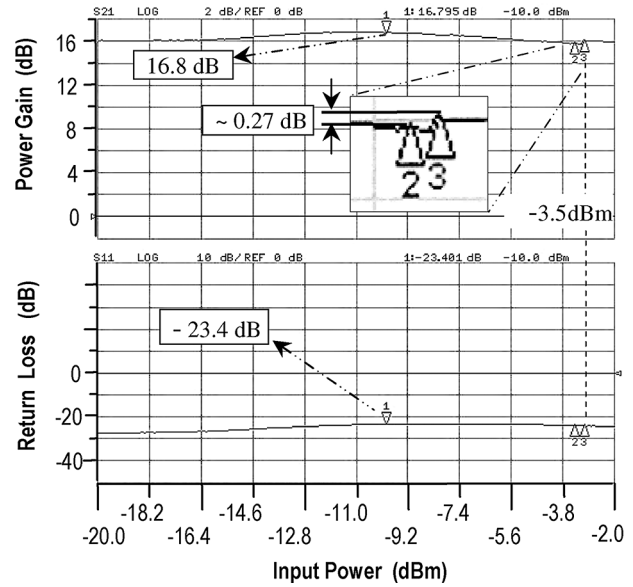


Fig. 15. Measured CW power gain (from [15]) and return loss versus P_{in} , with automatic hardware reconfiguration and envelope feedback enabled.

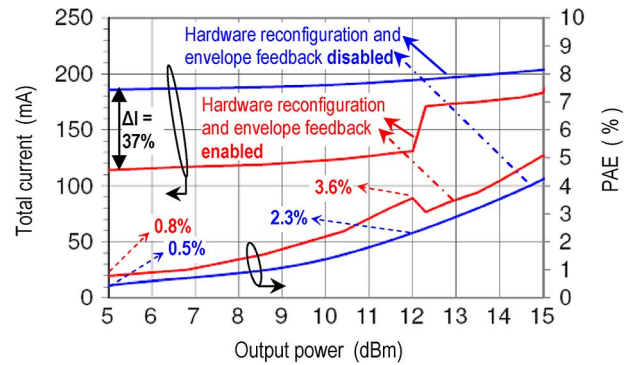


Fig. 16. Measured total current and the corresponding PAE with a CW excitation in two cases: with hardware reconfiguration and envelope feedback disabled or enabled.

in both the intermediate stage and the power stage are shut off automatically. Above the 12-dBm threshold (which also corresponds to the -3.5 -dBm input power threshold of Fig. 15), the power stage becomes fully enabled with half the transistor array in the intermediate stage disabled. For greater than 15 dBm, both stages are fully enabled automatically.

Second, this method allows a significant reduction in the overall current consumption. At 5 dBm of output power, as much as 37% reduction in the overall current consumption by the RFIC PA system (which includes ~ 15 mA for the feedback and gating circuitry in this particular design) is achieved. This represents a total current reduction from 185 to 115 mA, yielding a PAE improvement from 0.5% to 0.8%. For all measurements shown in Fig. 16, the output matching (VAR. Z_m in Fig. 3) was kept constant and in the same condition initially set to circumvent the RF instability, as stated above. Thus, a constant load condition was used in our implementation for all power ranges defined in Fig. 2. The 37% current reduction is therefore a result of half the RF transistor arrays in both the intermediate stage and the power stage being shut off.

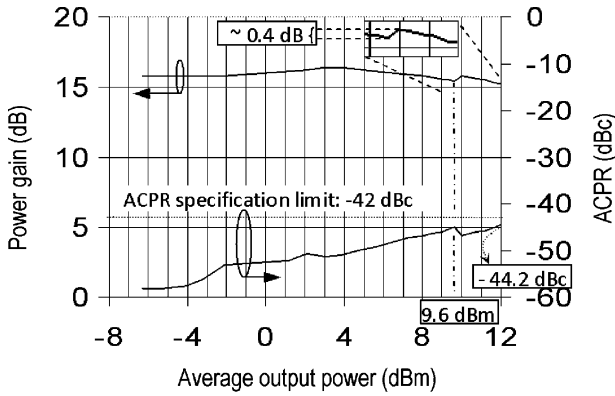


Fig. 17. Measured gain and ACPR1 (CDMA2000, from [15]).

While the PAE performance itself is lower compared to earlier works that treat specifically RF transistor array switching (e.g., 1.8% at 5 dBm in [9] and 3% at 5 dBm in [11]), our results do not represent a performance limitation that is inherent to a GEF PA. Instead, it is due to circuit design challenges in this specific implementation. First, our quiescent currents were intentionally increased to overcome an undesired gain compression condition caused by interaction between the RF signal and the nonlinear analog components in the bias and switching circuits. The gain regulation performance at the -0.3 -dBm threshold (Fig. 14) was also impaired. This explains why the closed-loop performances are shown with the lower threshold only (i.e., -3.5 dBm in Fig. 15, 12 dBm in Fig. 16), which still demonstrates the automatic current reduction and gain compensation capability of the technique. Second, the 15 mA for the feedback and gating circuitry stems from conservative design margins used in this first-time GEF design with NPN transistors. We estimate that with the availability of field-effect transistors (FETs) in a GaAs bipolar field-effect transistor (BiFET) process [18], these feedback and gating functions could be realized with less than 6 mA. Moreover, note that automatic shut off of the IHC and PHC blocks in Fig. 3 (but with the RF lineup state unchanged) could be envisaged at small signal in a new GEF PA, leaving only the other blocks biased. Finally, based on simulation, we foresee that implementing a GEF PA with a two-stage RF chain instead of three (hence, with significantly less biasing current) is feasible.

Therefore, we believe that with further RF chain and control circuitry optimization, the GEF technique can yield a much higher efficiency performance than we report here, while still providing the advantages that stem from its unique automatic switching features for standalone PAs.

D. Gain and Linearity Under CDMA2000 Modulation

Fig. 17 shows the measured gain and linearity performances with a CDMA2000 excitation. As the *average* output power ($P_{\text{out_ave}}$) drops below the 9.6-dBm threshold, half the RF transistor array in the power stage is switched OFF automatically, resulting in a gain deviation that is reduced to ~ 0.4 dB (from ~ 1.36 dB based on Fig. 14) thanks to the feedback operation.

It can be seen also that the envelope feedback operation allows meeting the CDMA2000 linearity requirement (i.e., -42 dBc for ACPR1 [14]). The waveform quality (Rho) in

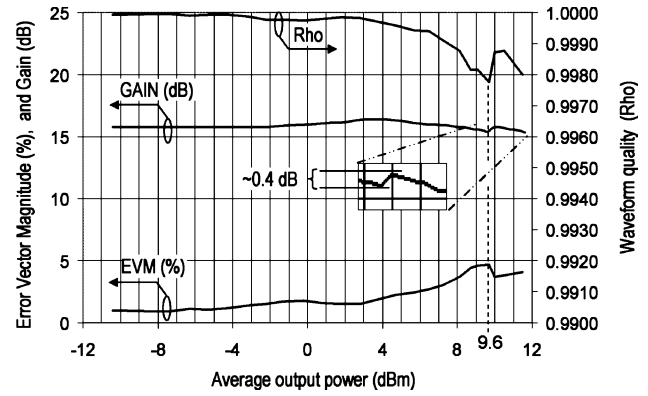


Fig. 18. Measured gain, Rho, and EVM with a CDMA2000 excitation.

Fig. 18 is well above the 0.944 minimum specification value, and the error vector magnitude (EVM) is less than 4.7%.

When $P_{\text{out_ave}}$ is close to 9.6 dBm, the CDMA instantaneous envelope power crosses repetitively above and below the threshold level. Therefore, these specifications compliant linearity figures also demonstrate that there is no excessive AM–PM distortion resulting from the reconfiguration mechanism, which confirms that the reconfiguration is not triggered by the instantaneous envelope power, as discussed in Section IV-C.

E. Discussion on the Results

We attribute the differences between the simulated (0.15 dB) and measured (0.27 dB) gain regulation performances, and between the experimental values for the CW and CDMA cases (i.e., 0.27 and 0.4 dB) mainly to gain offsets due to asymmetrical current pulling effects on the inputs of the error comparator (V_{deti} and V_{deto} in Fig. 4). These currents stem from nonlinear impedance variations at the inputs of the hysteresis comparators in the conditioner circuitry (Fig. 7), and vary with the envelope of the RF signal and the hardware states of the PA. They introduce error comparator voltage offsets that translate into PA gain offsets, and that cannot be cancelled by feedback. However, using the base current dependant power estimation technique described in [19] for triggering the hysteresis comparators would eliminate this problem since no interfacing with the error comparator (no CONDITIONER block, Fig. 3) would be required. Moreover, the GEF principle allows switching more than two RF sections (Fig. 9) per stage, hence less than 1.36-dB open-loop gain deviation (Fig. 14), therefore better closed-loop gain regulation.

The difference between the 12-dBm threshold of Fig. 16 (CW) and the 9.6-dBm threshold of Fig. 17 (CDMA) is justified by two aspects. First, the thresholds of the hysteresis comparators are dependant to some extent on the waveform of the envelope signal because these circuits are not fully desensitized against a modulated RF signal that is coupled through the V_{deti} node in Fig. 4. Second, the unequal charge and discharge time constants associated to C8 in Fig. 7 make the toggling point of the hysteresis comparator dependant on the envelope waveform. However, a 2.4-dB shift in the thresholds poses no significant problem in a GEF application.

Though limited to ~ 12 dBm of output power because of the RF-analog interaction problem discussed in Section V-C, these experimental results and the simulated results at 16 dBm in

Fig. 10 support the applicability of the GEF method for automatic RF transistor switching and gain compensation at low power. They also show that the associated level of AM-PM distortion allows envisaging simple typical-behavior based DPD linearization schemes concurrently to improve the linearity performance margin and further extend the upper power limit.

It is reasonable to assume that part of the noise generated by the envelope feedback and control circuitry may be translated to the receiver band. However, we believe its impact is not prohibitive for a handset PA application, given first that such noise may be minimized through design, and second that the GEF operation is intended for low power levels only, where comfortable receiver band noise performance margin is normally achieved due to the lower current intensity in the bias circuits and the RF transistors at these power levels. Note that the latter consideration is consistent with the fact that the GEF operation reduces the bias current in order to lower the PA gain (as illustrated with G_o and G_c in Fig. 2). Both the bias current reduction and the PA gain reduction tend to minimize the receiver band noise.

The PAE may be significantly improved with respect to our results with a two-stage RF chain and using lower current control circuit techniques in a GaAs-BiFET process, or realizing the feedback and gating circuitry on a CMOS IC in a multitechnology PA module. A CMOS active compensator also allows much larger loop bandwidths for other modulations, including W-CDMA.

VI. CONCLUSION

The proposed method allows automatic and multistate RF transistor switching for current reduction and gain compensation at low power in standalone RFIC PAs, and still allows the use of large-signal techniques for PAE improvement at higher power levels. It requires a single external control line, minimum synchronization from outside the PA, and minimum gain calibration. Results validating the method up to ~ 16 dBm were demonstrated with a pure GaAs HBT PCS-CDMA PA design. Besides cellular applications, the method is also attractive for RFIC PAs used in other transmitters with limited PA control.

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Nicolas G. Constantin (S'04–M'09) received the B.Eng. degree from the University of Quebec, Quebec, QC, Canada, in 1989, the M.A.Sc. degree from the École Polytechnique de Montreal, Montreal, QC, Canada, in 1994, and the Ph.D. degree from McGill University, Montreal, QC, Canada, in 2009, all in electrical engineering.

He is currently an Assistant Professor with the École de Technologie Supérieure, Montreal, QC, Canada. From 1989 to 1992, he was involved with the design of microwave transceivers for point-to-point radio links. From 1996 to 1998, he was an RF Design Engineer with NEC, Mulgrave, Australia, where he was involved in the development of RF and microwave transceivers for mobile telephony. From 1998 to 2002, he was a Design Engineer with Skyworks Solutions Inc., Newbury Park, CA, where he developed GaAs HBT RFIC PAs for wireless communications. While with Skyworks Solutions Inc., he was also actively involved in research on smart biasing and efficiency improvement techniques for RFIC PAs. He holds two patents. His primary research interests are in RFIC PAs and front-end modules for wireless communications.

Dr. Constantin was the recipient of a doctoral scholarship from the Natural Science and Engineering Research Council (NSERC) of Canada and a doctoral scholarship from the École de Technologie Supérieure, Université du Québec.



Peter J. Zampardi (S'93–M'96–SM'02) received the B.E. degree in engineering physics from the Stevens Institute of Technology, Hoboken, NJ, in 1986, the M.S. degree in applied physics from the California Institute of Technology, Pasadena, in 1988, and the Ph.D. degree from the University of California at Los Angeles (UCLA), in 1997.

While with the California Institute of Technology, he studied molecular beam-epitaxy (MBE)-grown GaAs/AlGaAs structures and investigated tellurium clustering in ZnSe:Te for use in visible light emitters.

In 1988, he joined the Ring Laser Gyroscope Test Laboratory, Rockwell Science Center, where he was responsible for development and testing of ring laser gyros for use in inertial measurement units. In 1990, he joined the Optics Technology Department, Rockwell Science Center, where he developed processes and procedures for the characterization and fabrication of infrared (IR) etalon filters. In 1991, he joined the High Speed Circuits Department, Rockwell Science Center, where he performed device and circuit development, characterization, and modeling of GaAs, InP, and SiGe HBTs and MESFET, HEMT, BiFET, and RTD technologies. In 1999, he led the technical development of SiGe RF models for the Analog and Mixed Signal Foundry business of IBM, Burlington, VT. Since 2001, he has been with Conexant/Skyworks Solutions, Newbury Park, CA, where he is Technical Director for Device Design, Characterization, and Modeling. The group's interest are technologies, characterization, modeling, and circuit design for wireless applications. He has authored or coauthored over 120 papers related to circuits and devices.

Dr. Zampardi actively participates in several IEEE technical conference committees.



Mourad N. El-Gamal (S'93–M'98) received the B.Sc. degree (with honors) from Ain-Shams University, Cairo, Egypt, in 1987, the M.Sc. degree (with a minor in computer science) from Vanderbilt University, Nashville, TN, in 1993, and the Ph.D. degree from McGill University, Montreal, QC, Canada, in 1998, all in electrical engineering.

Since 2004, he has held the William Dawson Scholar Chair with the Department of Electrical and Computer Engineering, McGill University, and served as a member of the Steering Committee of

the Nanofabrication Facility of the Institute for Advanced Materials. From March 2007 to July 2008, he was an Associate Vice Principal—Research and International Relations (VP-RIR) with McGill University. The office of the VP-RIR oversees all aspects of research activities at McGill University, from science and engineering to biomedical and drug development. Among the main initiatives that he spearheaded was the development of a comprehensive university–industry partnership strategic plan, including all aspects of technology transfer and commercialization. In 2002, while on leave from McGill University, he was Director of Engineering and then Vice President and General Manager of the Wireless Business Unit, MEMSCAP, Grenoble, France—a 165-employee publicly trading company specializing in microelectromechanical systems (MEMS). Earlier, he was with IBM Research and the French telecommunications company ALCATEL. He consults for companies and the Canadian Government on policies and strategies on regular basis. He has authored or coauthored over 80 technical papers and three book chapter. He holds one patent with five patents currently filed on novel micro/nano processes and devices. His research interests are in microscale and nanoscale integrated electronics and mechanical systems with a special interest in advanced materials. His research focus has been on the combination of these technologies to produce new knowledge and innovative solutions for a wide range of applications including wireless communications systems, health care, and aerospace.

Dr. El-Gamal was an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (2006–2008). He is currently the chair of the Biomedical, Sensors, Displays, and MEMS Subcommittee of the IEEE Custom Integrated Circuits Conference (CICC) (formerly the Emerging Technologies Subcommittee). He was the recipient of numerous teaching awards and his team has received several research awards.