August 2009: Product Feature

Two-stage Ultra Low Noise Amplifiers

Development of a family of two-stage low noise amplifiers covering the frequency range of 0.7 to 2.7 GHz

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From: Vol. 52 | No.8 | August 2009 | Page 100

Skyworks Solutions has developed a new family of two-stage low noise amplifiers (LNA): SKY65048-360LF, SKY65049-360LF and SKY65066-360LF. These amplifiers are fabricated with an advanced Skyworks PHEMT 0.5 µm process and packaged in low cost, miniature QFN 2x2 mm 8-lead plastic packages. Together, the three new products cover a frequency range of 0.7 to 2.7 GHz and are well suited for numerous low noise receiver applications such as ISM, GPS, GSM, CDMA, W-CDMA, TD-SCDMA, LTE, WiMAX and WLAN receivers.

These parts feature noise figures as low as 0.6 dB including all external components, adjustable gain and high linearity. Moreover, the shared pin-out and application board layout allows for easy implementation in various frequency bands. The noise figure performance of all three devices is illustrated in ***Figure 1***.

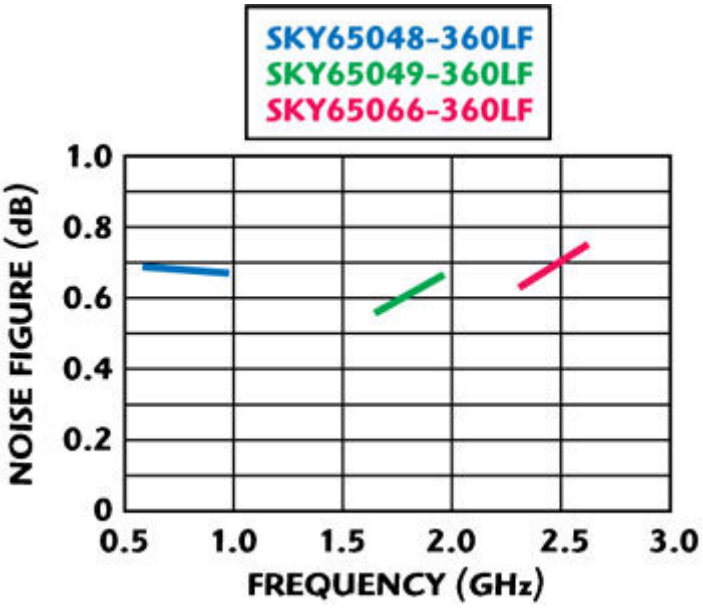

Figure 1 Noise figure performance vs. frequency.

Design

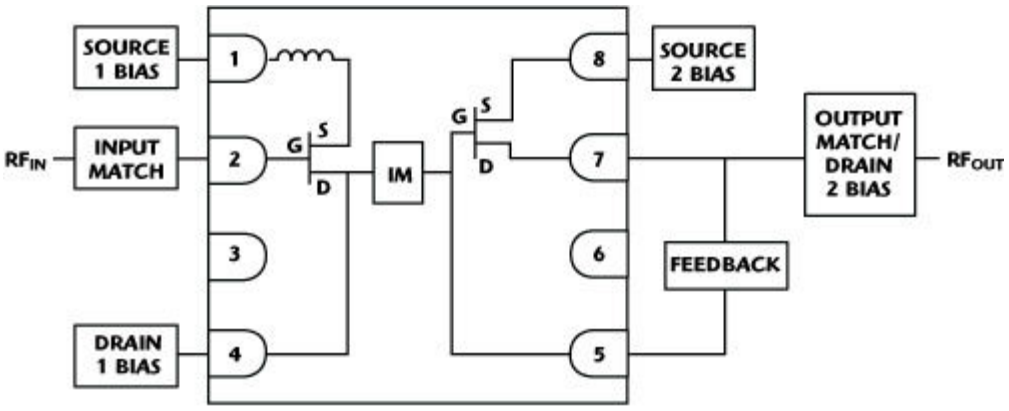

Figure 2 LNA functional block diagram.

This LNA family was designed using Skyworks' proprietary low noise 0.5 µm PHEMT depletion mode process achieving both very low noise amplification and low loss passive elements. The design topology consists of two cascaded common source amplification stages with an internal interstage matching network. This topology simultaneously produces low noise and high linearity performance in addition to providing flexibility. The flexibility of the design is a key feature as its performance can be optimized through selection of external components to meet a wide range of specifications. All three amplifiers share the same FR4 application board layout, but unique bills of material for circuits optimized for specific performance requirements are provided in the product datasheets. All reference circuits meet or exceed common performance requirements including unconditional stability up to 18 GHz. Similar RF performance can be obtained anywhere within the 0.7 to 2.7 GHz frequency band.

Figure 2 illustrates the different sections of the external reference circuit. Pins 1, 4, and 7, 8 are used to set the bias of the first and second stage, respectively. Pins 4 and 7 supply the bias voltage through a bias circuit that typically consists of a voltage drop resistor, bias inductors and RF decoupling capacitors. The bias inductors are also parts of the input and output impedance matching circuits. The supply current through each stage is set by the value of the resistors connected to Pins 1 and 8, thus eliminating the need for a negative bias at the gate of each stage. A capacitor is used to provide RF grounding. Pin 1 also has an internal source degenerating inductor for added stability, improved noise figure and better than 18 dB input return loss.

Pin 5 gives access to the gate of the second stage FET to enable optional feedback of a portion of the RF signal from Pin 7 (RF Out), thus reducing the gain without degrading the noise figure or output linearity. The feedback circuitry generally consists of an RC network.

Finally, Pins 2 (RF_{IN}) and 7 (RF_{OUT}) are externally matched through the use of simple matching networks, thus providing maximum flexibility to optimize performance over various bands. This also allows for tradeoffs in bias and output return loss for improved linearity performance.

Bias

Optimum noise and linearity performance of a transistor impose conflicting bias requirements. A two-stage design allows both noise and linearity performance requirements to be addressed simultaneously by optimizing each stage to a specific performance characteristic. Optimal noise figure is typically achieved by biasing the first stage to approximately 20 percent IDSS, which allows excellent noise performance while avoiding early saturation. The second stage transistor is biased to achieve optimal

linearity with more current or supply voltage, thereby producing higher third order intercept (IP3) or 1 dB compression level (P1dB) performance. The optimal drain voltage of each stage is also determined through the use of external voltage dropping resistors in the bias circuits.

Matching Components

Component selection for the input impedance match is critical for achieving good noise figure performance as any loss at the input will add directly to the intrinsic noise of the device. It is recommended to use high-Q components on the RF input (Pin 2) for the best noise figure results. Output impedance match and bias do not require the use of high-Q components. Output match can also be tuned to optimize output return loss and linearity performance (P1dB and IP3).

Stability and Good Layout Practice

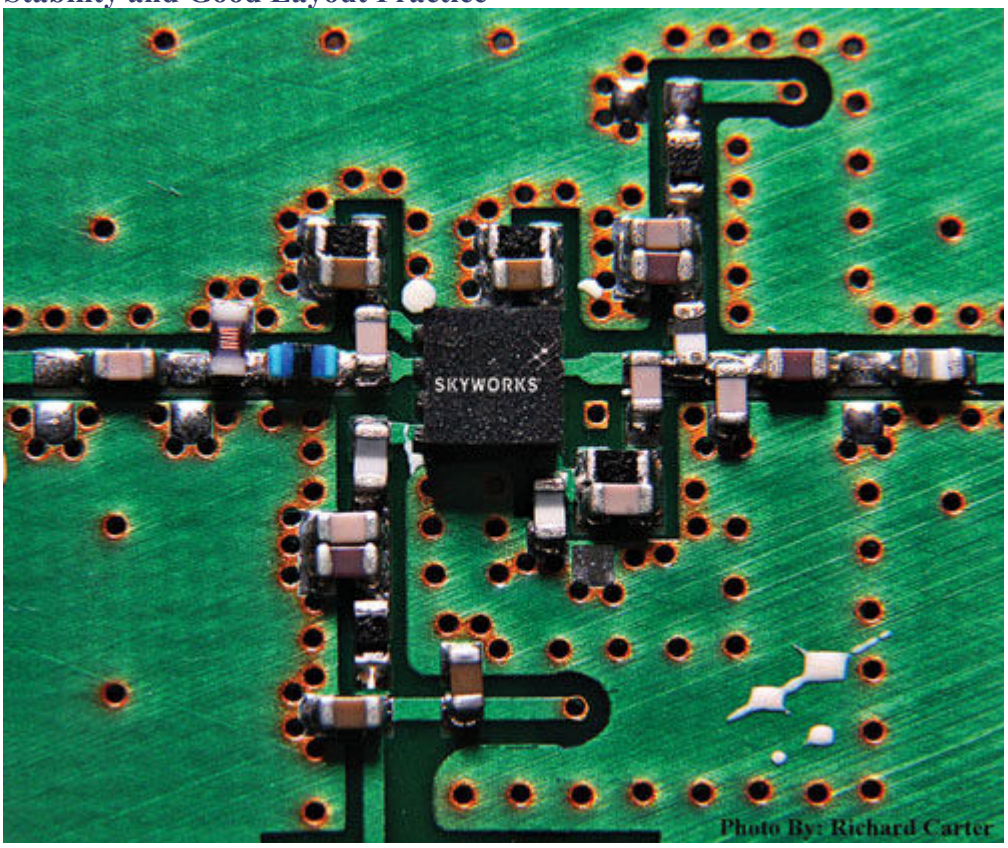

Figure 3 LNA evaluation board.

As can be seen in ***Figure 3***, a grounded coplanar waveguide transmission line (CPWG) is preferred over the microstrip line as it offers more tuning flexibility for shunt components and provides inherent signal isolation due to the presence of the grounded top metal layer.

The test board was realized on FR4. This material was selected due to its low loss, low cost and relatively low dielectric constant. The line width and spacing to the ground plane were selected to accommodate shunt 0402 size surface-mount components while maintaining a uniform 50 ohm line even when optional shunt components are not populated. Both top-side ground planes of the CPWG

line are referenced to the bottom ground plane through the use of vias on each side, to insure only the CPWG propagation mode exists.

As frequency increases, vias become increasingly inductive and the performance of lumped components may change in nature when used near or beyond their self-resonant frequency. At some frequencies, these changes may allow a positive RF feedback path, which may lead to unstable performance, including oscillation. The bias circuits of both stages are physically and electrically separated as much as possible and sharing of ground vias is avoided. The top ground plane is also intentionally broken in various sections to open any potential positive RF current feedback loops. The resulting metal "islands" are then brought to the common ground reference through the use of multiple vias in order to prevent unwanted resonances.

Vias should also be placed as close as possible to board components in order to minimize the electrical length to the ground reference, which includes the vias' length. The most sensitive regions are the input match and the RF decoupling regions of drain and source terminals of each stage. Careful attention must be paid to the layout of these regions to achieve good gain and noise figure performance. These sensitive regions are carefully addressed on the evaluation board by the addition of multiple vias to minimize parasitic inductance in these paths.

Performance

The application circuits were tuned to operate with 5 V DC drain bias and 75 to 85 mA drain current. Each stage of the amplifier is biased separately from a single DC supply to achieve the targeted noise and linearity performance. The first stage transistor is biased at 20 percent of IDSS, about 20 mA in this case. Performance specifications are summarized in ***Table 1***. These circuits can be changed to operate at lower or higher power.

TABLE I

LNA PERFORMANCE

Part Number	Operating Frequency (MHz)	Test Frequency (MHz)	Gain (dB)	$\|S_{11}\|$ (dB)	NF (dB)[1]	OIP3 (dBm)	OP_{1dB} (dBm)	VDD (V)	Quiescent Current (mA)
SKY65048-360LF	700-1000	900	15-25	18	0.7	35.5	18	5	85
SKY65049-360LF	1500-2400	1950	15-25	18	0.7	34.5	18	5	75
SKY65066-360LF	2300-2700	2500	15-25	18	0.7	35.5	18	5	75

Note 1: Input connector loss removed from measurement.

Table 1

All performance parameters are achieved with an external reference circuit. High Q, low loss Coilcraft-HP inductors and Murata-GJM capacitors are used for the input matching network to optimize noise figure. All three LNAs are able to attain less than 0.7 dB noise figure with return loss of 18 dB in their respective frequency ranges, including matching network losses. Output third order intercept (OIP3) performance is better than 34.5 dBm for all devices with output 1 dB compression (OP1dB) of 18 dBm.

Applications

These LNAs are typically used in receiver applications that demand low noise and high sensitivity while maintaining compact size and low cost. Typical examples are ISM, GPS, GSM, CDMA, W-CDMA, TD-SCDMA, LTE, WiMAX and WLAN receivers. Through the use of external components to achieve acceptable input impedance match, the LNAs can be tuned to operate over a wide frequency range and under various bias conditions, while meeting demanding performance requirements.

S-parameters, populated evaluation boards and suggested PCB layouts are available. Additional applications support is also available upon request.

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