On the Characterization of Thermal Coupling Resistance in a Current Mirror

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Abstract — **In this work, the thermal coupling resistance (R12) between the reference transistor and the output transistor in a current mirror is characterized by two different measurement techniques: the constant voltage, and the constant current R12 extractions. The extracted R12 from both methods are very similar. The constant voltage method is deemed to be more physical or accurate than the constant current method. Further TCAD simulation agrees well with R12 measurement data.**

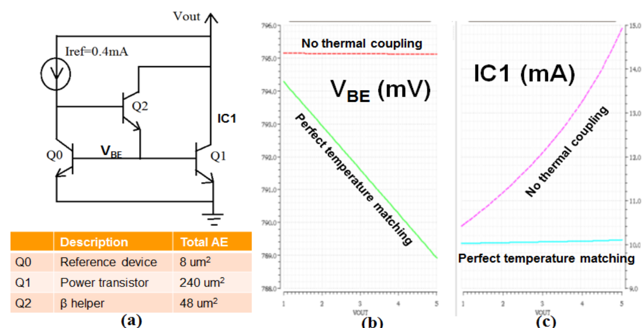
Index Terms — thermal coupling; thermal resistance; SiGe HBT; current mirror; ANSYS Mechanical; finite element modeling

I. Introduction

To support the increasing number of users, as well as the new classes of applications with high bandwidth requirements, wireless network capacity must be enhanced to meet the demands. Another notable trend is that all the mainstream smart phones or pads on the market are now thinner than 10 mm in order to better appeal to customers. As a result of the tenacious competition, today's mobile products are requesting semiconductor chips to be made ever faster, smaller, and thinner. As the WiFi power amplifiers (PAs) operate on smaller and thiner dies with high power densities, the PA thermal design has become a daunting task [1-3].

There have been many studies on the thermal behavior of single transistors and their power arrays [4 5]. However, there has been very limited work on the thermal coupling in PA designs [6]. The cadence simulation on a simplified current mirror, which is often used in today’s PA product, is demonstrated here to illustrate the importance of understanding the thermal coupling. Fig. 1a shows the schematic view of the simplified current mirror circuit. Figs. 1b and 1c show the two simulation results of the current mirrors with two different assumptions. In the first simulation, Q0 and Q1 are assumed to be independent of each other so there is no thermal coupling. As I_{REF} is fixed at 0.4mA, the base voltage is clamped at around .795 V when output voltage is swept from 1 to 5 V. The IC1 vs. Vout curve shown in Fig. 1c represents more of a constant V_{BE} output curve for power transistor Q1. Alternatively speaking, the mirror ratio (IC1/IC0) increases with V_{OUT} due to the increased junction temperature difference between Q0 and Q1 as Vout or power dissipation is increased in Q1. In the second simulation, Q0 is assumed to have perfect thermal coupling to Q1 such that these two transistors always share the same junction temperature. When Vout is increased, the junction temperature rises for both Q0 and Q1. The base voltage decreases as a negative feedback to the increased power dissipation, as shown in Fig. 1b. The IC1 vs. Vout curve shown in Fig. 1c bears more similarity to a constant Ib output curve for power transistor Q1. In the practical design there is always limited but imperfect thermal coupling between Q0 and Q1, so the IV behavior will settle in somewhere between these two extreme simulations. The difference in output conductance also suggests a significant impact on PA ruggedness from thermal coupling. In short, a lack of the prior knowledge of the thermal coupling between Q0 and Q1 will pose a grand design challenge to PA designers.

This work is organized as follows: the subsequent section presents the details for the device technology and experiment design. Two different characterization methods were used to extract the thermal coupling resistance in the next section. Then, TCAD simulation is used in the last to help understand the thermal coupling resistance data.



	Description	Total AE
Q0	Reference device	8 um²
Q1	Power transistor	240 um²
Q2	β helper	48 um²

Fig.1 a) Schematic view of current mirror; b) Base voltage response to output voltage sweep; c) Output current response to output voltage sweep

II. Experiment

A. Device and Technology

The current mirrors used in this investigation is designed with a commercial SiGe HBT BiCMOS technology that features 6.0-V BV_{CEO}, 35-GHz fT SiGe HBTs and 5-V Si CMOS devices. The total emitter areas are 30 μm^2 and 600 μm^2 for reference transistor Q0 and output transistor Q1, respectively. The emitter area is 24

μm² for the β helper Q2. The schematic view of the current mirror is shown in Fig. 2.

The through-wafer vias (TWVs) are also included in this process to enable the single-ended amplifier architecture.

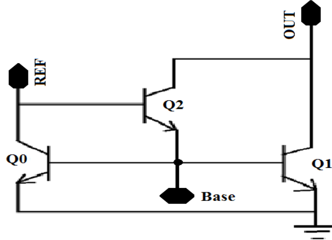


Fig. 2 Schematic representative view of the current mirror test structures

B. TCAD Simulation

A finite element modeling tool, ANSY Mechanical, is used to simulate the thermal coupling between the reference and output transistors [7]. The model consists of a large 200 x 200 mm² Silicon wafer with the current mirror located in the center. A contact conductance boundary condition at 27 °C is applied to the bottom of the wafer and all other surfaces are assumed to be adiabatic.

III. Thermal Coupling Resistance Characterization

The thermal coupling resistance (R12) is often used to quantify the junction temperature rise of a reference device that is sitting in the proximity of a heat source (the output transistor for the current mirror case). Either the collector current or the base voltage of the reference transistor is recorded as the electrical gauges to monitor the junction temperature during the power sweep of the output transistor. With proper temperature calibration steps the junction temperature in the reference device can be calculated. When the reference junction temperature is plotted against the power dissipation in the output transistor, the slope of junction temperature rise is R12.

A. Constant Current R12 Extraction

In this measurement, the input reference current is fixed at 0.9, 1.05, and 1.2 mA, respectively, while the output voltage is swept from 1 to 5 V. In Fig. 3a the output current increases with V_{OUT} due to the self-heating in the output transistor Q1. Since Q0 and Q1 are thermally coupled, the junction temperature of Q0 increases as power dissipation increases in Q1. When the junction temperature of Q0 is increased at higher V_{OUT} its base voltage will decrease to maintain a fixed I_{REF} bias, as shown in Fig. 3b.

Temperature measurements are performed in the next step to calibrate Q0 junction temperature dependence of V_{BE}. In this measurement, I_{REF} is fixed at 0.9, 1.05, and 1.2 mA, V_{OUT} is fixed at 1 V, and the V_{BE} is recorded as the temperature is swept from 25 °C to 65 °C. Based on the temperature to V_{BE} correlation data shown in Fig. 4a, the junction temperature in Q0 can be calculated from V_{BE} data shown in Fig. 3b. In Fig. 4b, the junction temperature of Q0 is plotted against the power dissipation in Q1, which is V_{OUT}*I_{OUT} to the first order. The slope of this curve is calculated as R12, which are 62.4 °C/W, 61.5 °C/W, and 61.0 °C/W for I_{REF} of 0.9 mA, 1.05 mA, and 1.2 mA, respectively.

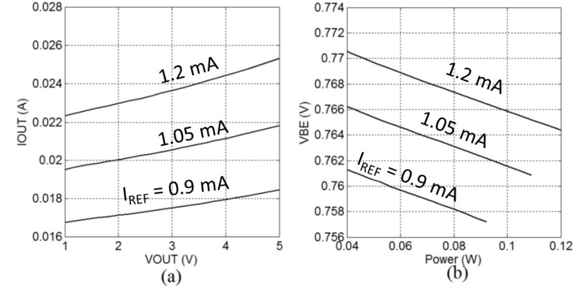


Fig. 3 Fixed I_{REF} measurement with V_{OUT} swept from 1 to 5 V a) I_{OUT} versus V_{OUT}; b) V_{BE} versus V_{OUT}

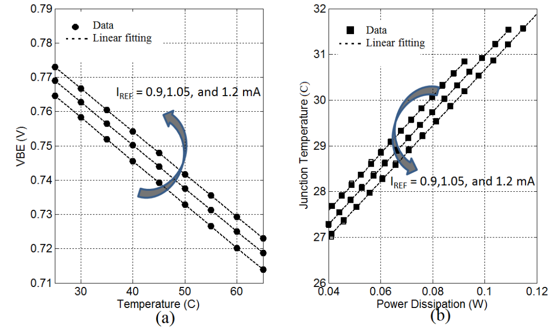


Fig. 4 The thermal coupling resistance extraction through fixed I_{REF} measurement a) V_{BE} versus temperature calibration; b) Junction temperature versus output power

B. Constant Voltage R12 Extraction

In the second measurement, both the base and the reference in Fig. 2 are biased at a fixed voltage of 0.78 V and the output voltage is swept from 1 to 5 V. The current at the output are recorded and shown in Fig. 5a during the output voltage sweep. As the dissipated power in Q1 increases with V_{OUT}, the junction temperature of Q1 increases as a result of self-heating. At constant base voltage bias the collector current of Q1 increases exponentially with junction temperature. In addition to the self-heating in Q0, the mutual heating from Q1 leads to the further junction temperature rise in Q0. Thus the I_{REF} increases with V_{OUT}, as indicated in Fig. 5b.

To quantify the junction temperature at various powers, the I_{REF} at constant base bias of 0.78 V is measured from 25 °C to 65 °C. It is well known that the transfer current of a hetero-junction bipolar transistor can be described by

$$I_T = \frac{c_{10}}{Qp,T}\left[\exp\left(\frac{v_{BE}}{v_T} - \exp\left(\frac{v_{BC}}{v_T}\right)\right)\right] \quad (1)$$

where c10 and Qp,T are process-related constants [8]. When the transistor is operating under forward-active bias condition the eq. (1) can be further approximated as

$$I_T = \frac{c_{10}}{Qp,T} \exp\left(\frac{v_{BE}}{v_T} \right) \quad (2)$$

The measured I_{REF}, when plotted in log mode versus V_{BE}, has shown in Fig. 6a the perfect linear relationship to the V_{BE} bias as expected. The junction temperature of Q0 in this measurement can be calculated from Fig. 5a data based on the equation 2. In Fig. 6b the junction temperature of Q0 is plotted against the power dissipation in Q1, which is $V_{OUT}*I_{OUT}$ to the first order. The slope of this curve is calculated as R12, which is 61.9 °C/W.

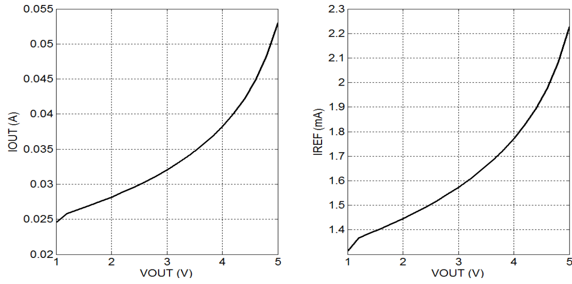


Fig. 5 Fixed V_{BE} measurement with Vout swept from 1 to 5 V a)I_{OUT} versus V_{OUT}; b)I_{REF} versus V_{OUT}

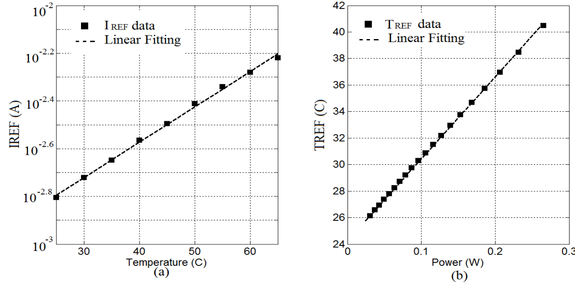


Fig. 6 The thermal coupling resistance extraction through fixed V_{BE} measurement a) I_{REF} versus temperature calibration; b) Junction temperature versus output power

C. Discussion

Both constant current and constant voltage measurement methods give very consistent R12 data. This demonstrates the validity of the experimental data. In the constant current measurements the base currents of Q0 and Q1 are changing as their junction temperatures change during the power sweep. The junction temperature of Q2 might change, too, due to finite thermal coupling from the output transistor. The base current of Q2, which is also a small part of I_{REF}, is thus changing during the power sweep. This has some minor impact on the accuracy of the temperature calibration. It can also help to explain the subtle R12 differences when I_{REF} is biased at 3 different currents. In the constant voltage measurement Q2 can be considered as an effective open since its BE junction is biased at 0. The Q0 is a diode-connected transistor in the proximity of Q1. During the power sweep of Q1 the relative change of collector current of Q0 can be used to calculate its junction temperature change. This is actually the same principle that has been used in bandgap reference circuit design [9]. The constant voltage method here assumes negligible junction temperature rise due to the self-heating in Q0, which is the case when the mirror ratio is large. However, further temperature calibration is needed to consider Q0 self-heating. When the two methods are compared, the constant voltage method is considered more physical hence more accurate.

Q0 and Q1 share the same V_{BE} bias in Fig. 2, so the current mirror ratio, which is defined as I_{OUT}/I_{REF}, is mostly sensitive to the junction temperature difference between the two transistors according to equation 2. To study the junction temperature difference, the temperature dependences of output current at fixed V_{BE} are shown in Fig. 7a for both Q0 and Q1. Both transistors have the same temperature slope on the output currents. After using the temperature data in Fig. 7a, the calculated junction temperatures for both Q0 and Q1 during fixed V_{BE} measurement are plotted in Fig. 7b. The slope of the top curve provides a good estimate of the thermal resistance of Q1, with the assumption that both the early effect and the avalanche current are insignificant in Q1 during the fixed V_{BE} measurement. The calculated R_{TH} on Q1 is in agreement with previous R_{TH} extraction using constant IE measurement [5]. The temperature difference between Q0 and Q1 shown in Fig. 7b is used to calculate the mirror ratio change at various powers. The calculated mirror ratio is compared against data in Fig. 8. They are in good agreement. This suggests that in order to simulate the mirror ratio right it is important to simulate the junction temperature right for both Q0 and Q1. A similar conclusion has been drawn in [6] that for the constant I_{REF} drive the output current is proportional to the temperature difference between the reference and the output transistors.

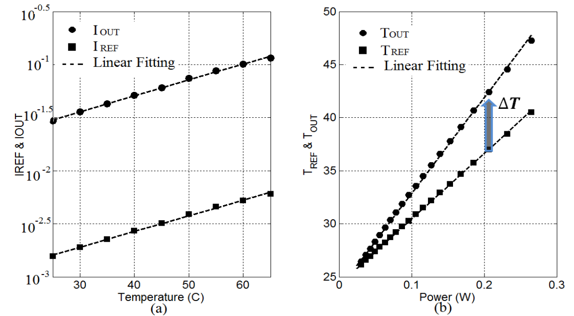


Fig. 7 The junction temperature during fixed V_{BE} measurement a) I_{REF} & I_{OUT} versus temperature calibration; b) Junction temperature versus output power

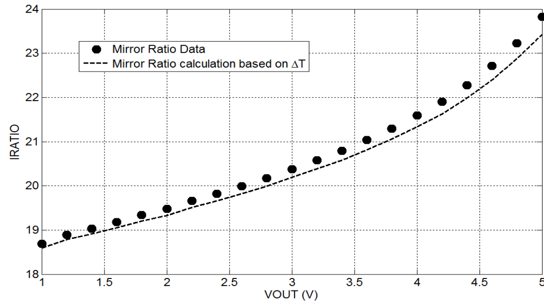


Fig. 8 The measured current mirror ratio versus calculation

IV. TCAD Simulation

During the electro-thermal measurement, we are treating the junction temperature as the electro-average of the selected transistors. In the actual applications, the heat generation and the heat transfer of transistors are distributed in nature. To further study the heat flow in the current mirror test structure, TCAD thermal simulation is performed using ANSY Mechanical. The reference transistor and the output transistor are biased at the similar power level as that used in actual measurements. The simulated temperature map is shown in Fig. 9. It clearly suggests higher junction temperature in the output transistor than in the reference device. The temperature distribution on a line from point A to point B in Fig. 9 is shown in Fig. 10. It can be seen that the junction temperature in output transistor is 1-2 ^{0}C higher than that in the reference device. N. Rinaldi developed an analytical model to calculate the temperature distribution in integrated circuit [10]. The geometric and layout information of the current mirror is implemented into the analytical model and calculated temperature distribution matches the TCAD thermal simulation results very well.

The TCAD is also very helpful in simulating the R12. In this simulation the output transistor is biased at selected power while the reference device is in off condition. The R12 is calculated as the junction temperature rise in the reference device divided by the power dissipation in the output transistor. The calculated R12 in TCAD is 61.9 $^{\circ}$C/W, agrees well with the measurement data. With proper TCAD calibration, this makes it possible to do predictive thermal modeling in an actual current mirror design.

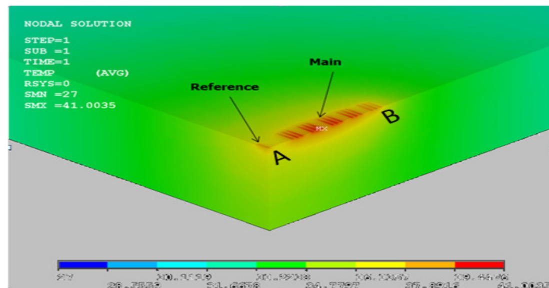


Fig. 9 The thermal simulation on the current mirror

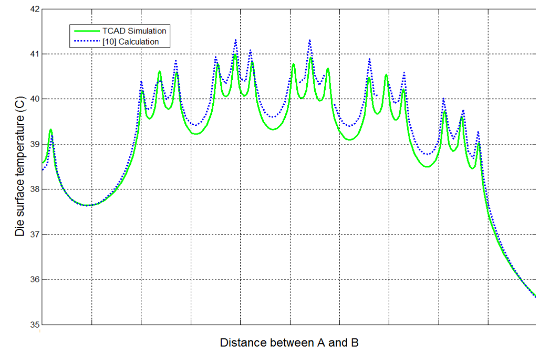


Fig. 10 The temperature mapping from A to B in Fig. 9

V. Summary

This paper investigates the thermal coupling resistance between the reference and the output transistors in a current mirror. First the importance of understanding the R12 in the current mirror is demonstrated through Cadence simulations. Two R12 extraction methods, the constant current and the constant voltage methods, are explained. Lastly, the extracted R12 data are validated through TCAD simulation.

References

[1] M. Heimlich, B. Schwitter, G. Ritchie, J. Fiala, and S. Mahon, “An integrated electrothermal design primer using an SiGe HBT PA.,” IEEE microwave magazine, 2012, pp. 70–80.

[2] M. Heimlich, “An electrical-thermal coupled solution for SiGe designs,” High Frequency Electronics, Sept. 2013, pp.22–28.

[3] A. Joel, “Design for SiGe HBT power amplifiers for microwave radar applications,” PhD thesis, Georgia Institute of Technology, May 2009.

[4] J.-S. Rieh, D. Greenberg, B. Jagannathan, G. Freeman, and S. Subbanna, “Measurement and modeling of thermal resistance of high speed SiGe heterojunction bipolar transistors,” Proc. Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2001, pp. 98-101.

[5] T. Chen, T-Y. Lee, J. Allum, and M. McPartlin, “The thermal scaling: from transistor to array,” IEEE Radio frequency integrated circuits symposium, Proceedings of 2014, pp. 123-126.

[6] M.T. Ozalas, “The impact of electro-thermal coupling on HBT power amplifiers,” IEEE compound semiconductor integrated circuit symposium, Proceedings of 2014, pp. 1–4.

[7] Introduction to ANSYS Mechanical, http://www.ansys.com/Support/ Training+Center/Courses/.

[8] M. Schroter, “A scalable physics-based compact bipolar transistor model”, http://www.iee.et.tu-resden.de/iee/eb/comp_mod.html

[9] Y. P. Tsividis, “Accurate analysis of temperature effects in Ic-Vbe characteristics with application to bandgap reference sources,” IEEE J. Solid-State Circuits, vol. 15, no. 6, pp. 1076-1084.

[10] N. Rinaldi, “Thermal analysis of solid-state devices and circuits: an analytical approach,” Solid-State Electronics, 2000, vol. 44, pp. 1789-1798