Large-Signal Characterization and Modeling of MOSFET for PA Applications

Sunyoung Lee and Tzung-Yin Lee
Skyworks Solutions, Inc.
5221 California Avenue, Irvine, CA 92617

***Abstract* — This paper presents the large-signal model requirements and generation as well as the 1- and 2-tone large-signal characterization for CMOS PA applications. The sensitivity of important parameters to the large-signal prediction for a transistor is discussed. It is demonstrated that an accurate modeling of G_m as a function of bias, as well as other important extrinsic transistor parameters, enables proper prediction of the 1-tone distortion behavior for a transistor, which in turn determines the quality of prediction for the 2-tone inter-modulation product up to the 5th order.**

***Index Terms* — MOSFET model, PSP model, large-signal modeling, non-linearity modeling**

I. Introduction

The CMOS PA has attracted many research efforts in the past 10 years with successful commercialization of a single-chip CMOS GSM/GPRS quad-band PA in 2008 [1]. The main challenge in CMOS PA design is to deliver sufficient power, and achieve high PAE, while maintaining its linearity, reliability and surviving the ruggedness test. The technologies used for CMOS PA design usually have relatively low reliable operating voltages of ~2.5 or 3.3V, when compared with the GaAs or Si Bipolar counterparts at 6~8V. Efficiency loss on a ~2-4 Ω-cm lossy Si substrate is also an issue.

Due to the phenomenal proliferation of CMOS RFICs in the consumer electronics, there have been many modeling papers published in the past decades. However, most of them focus on the small-signal and noise behavior of the transistors [2][3][4][5]. Only a few papers discussed the MOSFET non-linear behavior at high frequencies, but their approach is either based on 1-tone distortion analysis [6] or with a non-standard model [7][8].

To support the design and top-level simulation of a single-chip CMOS PA with integrated passives and power control functions, it is desirable to use a compact model that is computationally efficient, numerically robust, and widely available in most popular commercial simulators. This paper describes the model requirements and generation with a standard compact model for a CMOS PA application. The paper is organized as follows. Section II describes the critical requirements for a model to be used for CMOS PA design. The modeling methodology and measurement results are presented in Section III. Finally the paper is concluded with a summary and discussion in Section IV.

II. Model Requirement

A conventional way to study the non-linear behavior of a device or a circuit is to use the Volterra series [9]. While providing insight on the sensitivity of each non-linear component within a transistor to the overall system distortion, the Volterra series is practical only for analysis of the weak non-linear behavior for a system operating at low power levels. Moreover its application relies heavily on an accurate compact model to provide good estimates of the transistor parameters, such as G_m, C_{gs}, and C_{gd}, at the bias point where the non-linearity is calculated. However, as a handset PA often operates at very high or even at saturated power, the Volterra series is not suitable for its analysis. The model used for PA design must be accurate from low to very high power levels.

Design of a handset PA focuses mostly on delivering sufficient power output (Pout) and maintaining high linearity, while maximizing the power added efficiency (PAE). Recent emphasis for extended battery life in a metropolitan area requires a PA having high PAE, not just at the maximum Pout, but also at the low and medium power level. To optimize the PA for this wide range of Pout, the large-signal behavior of the transistor has to be accurately predicted over a wide range of bias as well as input power.

While the primary functionality of a PA is to deliver high power, the noise generated by the PA has to be maintained below a certain level. A typical requirement for a GSM/GPRS PA is that the noise at 20MHz offset, i.e. RX band noise, has to be below -160dBc/Hz. To support simulation of the RX band noise at the product level, the model needs to accurately predict the noise behavior of a transistor under a modulation, i.e the up-conversion noise. Therefore, some of the proprietary implementation with specific emphasis on the transistor non-linearity, e.g. [7][8], while predicting well the large-signal behavior for a transistor, is not entirely

suitable for the single-chip PA design due to the insufficient noise modeling.

Computational efficiency and numerical robustness is also an important concern for CMOS PA design. Compared with a discrete solution or a GaAs counterpart, a CMOS PA is often relatively complex with the integrated power control functions. Moreover the simulation time can grow rapidly with advanced simulation like the envelop analysis or with the corner or statistical simulation, which is very typical for CMOS design as the mask re-spin is often much more costly than a GaAs counterpart.

Considering the key model requirements for a CMOS PA design, it is straightforward to employ a mature compact model that has been implemented in the major simulators like Agilent ADS or Cadence Spectre®. Here we selected the surface potential PSP model [10] for its symmetrical implementation with respect to the body. While the advantage of the PSP model is not quite obvious for the PA simulation over other alternative source-referenced models like BSIM, it enables accurate co-simulation with an on-chip integrated switch for by-pass or other purposes. Being a body-referenced model, PSP does exhibits a significant advantage over BSIM for a common-gate type of application like an RF switch [11]. Besides, as the development of PSP or BSIM is mostly driven by the advanced CMOS technology, use of these industrial standard compact models, in contrast with those non-standard models, provides an easy way of modeling the layout-dependent effects and enables an accurate modeling of the PA unit cell with a relative large and custom layout.

III. MODEL AND MEASUREMENT RESULTS

The technology used for the CMOS PA design is a typical digital 0.13µm technology with dual threshold voltages (V_T) and ultra-thick dual top metal (UTDM) for on-chip passive integration. Both the driver and final PA use a cascode topology with the core FET at the bottom as the G_m stage and the IO FET at the top as the cascode stage to withstand high voltage swing.

For an example GSM/GPRS PA as described in [1], the small-signal power gain of the transistor, while being very important to the overall predictability, is not directly related to the power gain of the PA, as it is overdriven by at least 10dB to achieve high efficiency for a saturation-type of PA. The main sources of the efficiency loss include 1) R_{on} of the transistor when it is hard turned on; 2) the loss through the on-chip passive matching network; and 3) the loss into the substrate at the cascode output.

While the harmonic components of the PA at the antenna are significantly suppressed by the matching network and the duplexer, their magnitudes are largely proportion to on the transistor distortion. The transistors are the primary source for the non-linearity generated by PA. According to [6], the distortion behavior of a MOSFET changes marginally, when the operating frequency is still significantly below the unity gain frequency (f_T) at the bias point. In other words, the non-linear behavior of a MOSFET of an advanced technology of 0.18um or below is mostly dependent on the quasi-static characteristics of the transistor. Therefore, the distortion can be properly predicted by a model with a typical quasi-static extraction methodology, i.e. with a DC IV measurement on simple transistor test structures and low-frequency CV measurement on large-area capacitance structures [6].

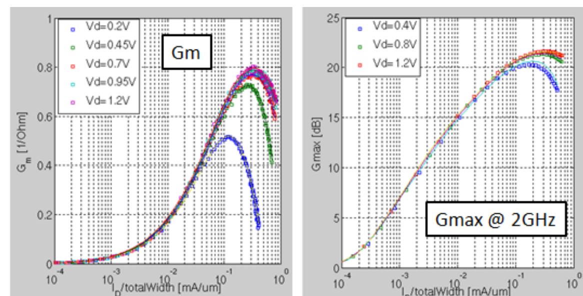

Fig. 1. Model playback versus measurement on (a) DC G_m and (2) RF power gain G_{max} at 2GHz for a 16x6.12umx0.13um NFET. Symbols represent data and lines represent the model.

The model was extracted with a RF based extraction methodology [2][3]. According discussion in the previous paragraph, to ensure the model predicts the distortion behavior of a transistor up to a very high power level, the model has to accurately predict the transistor G_m as a function of V_G or I_D as well. 0 shows the Model playback versus measurement on (a) DC G_m and (2) RF power gain G_{max} at 2GHz for a 16x6.2µmx0.13µm NFET.

0 shows the 1-tone distortion characteristics and power gain (Gp) as a function of the input power (P_{in}) for the same transistor as in 0. As shown in the figure, the model, when it is fitted well to very high current (c.f. 0), can properly predict the gain compression and the large-signal distortion behavior of the transistor up to 10dB above the 1dB compression point (P_{1dB}).

0 shows the large-signal behavior as a function of the drain current I_{ds} for a transistor operating around its P_{1dB} point. When cross referenced with the G_m characteristics shown in 0, it is not surprising to notice that the fundamental tone just tracks the DC transistor G_m even at 1.8GHz. This is because the transistor still operates in its quasi-static region, as the f_T of the

transistor is about 10~50 times higher than the operating frequency across the bias range. It is also obvious in 0 that the 2nd harmonic correlates closely with the 1st order directive of the fundamental tone characteristics and the 3rd harmonic with the 2nd order derivative (or the 1st order derivative of the 2nd tone). Therefore, accurate fitting of G_m as a function of the bias, i.e. V_{gs} or I_{ds}, is most important to the large-signal behavior prediction for a transistor.

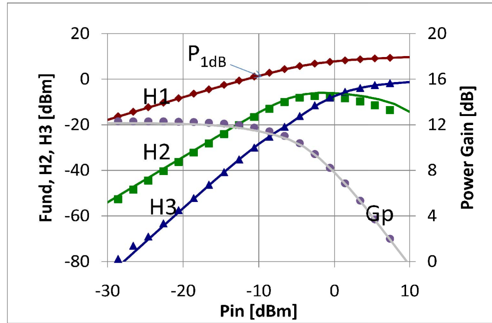

Fig. 2. 1-tone distortion behavior of a 16x6.12µmx0.13µm NFET as a function of Pin at 1.8GHz. The symbols represent the measured data and the solid lines are the distortion prediction results of the full-blown model.

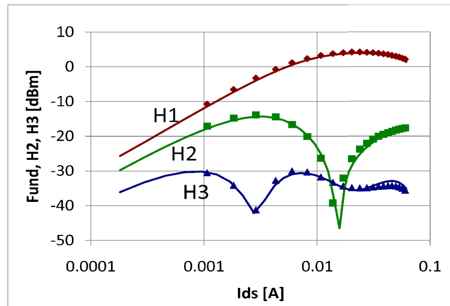

Fig. 3. 1-tone distortion behavior of a 16x6.12µmx0.13µm NFET as a function of Ids at P_{in}=-10.6dBm and frequency=1.8GHz. The symbols represent the measured data and the solid lines are the distortion prediction results of the full-blown model.

In addition to G_m, whose characteristic is mostly determined by the intrinsic portion of the transistor, (i.e. the charge inversion), mobility and velocity saturation, the extrinsic portion of the transistor, (i.e. the drain and source resistance R_d and R_s), can also influence the large-signal behavior of the transistor. While R_d and R_s both introduce negative feedback and reduce the gain of the transistor, their impact to the transistor large-signal behavior is quite different. The source resistance (R_s) improves the linearity, but the drain resistance (R_d) exacerbates the gain compression. Fortunately, unlike those in the LDMOS, they are mostly symmetrical to each other for a transistor with many fingers, which is typical for PA design, and their values can be extracted with the method described in [2].

Modern cellular standards like WCDMA or LTE demand very linear PAs to support complex modulation. Unlike GSM PA, where only harmonic components are concerned, the WCDMA PA requires the power leakage into the adjacent channel to be contained under a certain level, which is the direct result of the inter-modulation. 0 shows a model that is capable of accurately predicting the 1-tone characteristic can also predict the 3rd and 5th order inter-modulation products very well over a wide range of biases and at a relatively high power level (~3dB above its P_{1dB} point). While P_{in} of each tone is about 3dB lower than the P_{1dB} point, the peak instantaneous power of the two tone signal combined together can drive the transistor 3dB above its P_{1dB} point. Directly related to the blocker generation, the high- and low-side 2nd order inter-modulation products are shown in 0.

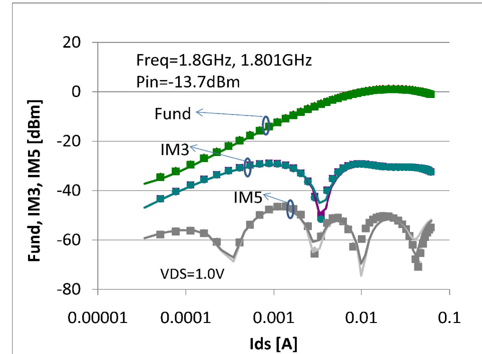

Fig. 4. The 3rd and 5th order inter-modulation products of a 16x6.12µmx0.13µm NFET as a function of Ids at P_{in}=-13.7dBm and frequency=1.8GHz and 1.801GHz.

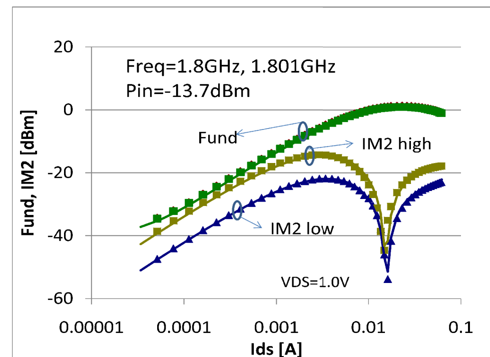

Fig. 5. The high- and low-side 2nd order inter-modulation products of a 16x6.12µmx0.13µm NFET as a function of Ids at P_{in}=-13.7dBm and frequency=1.8GHz and 1.801GHz.

0 shows the power gain (G_p), harmonic distortion characteristics (H2 and H3), and the DC current consumption as a function of the output power (P_{out}) for a cascode amplifier, which is the building block for the cell array used in the final stage PA. The cascode stage

uses 1.2V low V_T devices at the bottom as the G_m stage and 2.5V IO devices at the top to sustain the possible high-voltage swing at high P_{out} or under mismatch VSWR. As shown in the figure, the combined model predicts well the non-linear characteristics and the DC current consumption, which in turn determines the efficiency of the PA, for the basic building block of the PA.

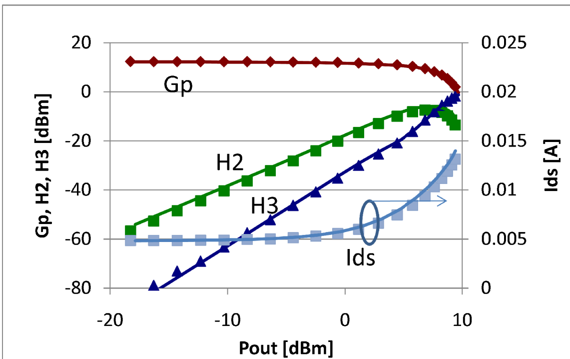

Fig. 6. The power gain (G_p), harmonic distortion characteristics (H2 and H3), and the DC current consumption as a function of the output power (P_{out}) for a cascode amplifier. V_{G1} (the gate voltage of the lower G_m stage) = 0.4V, V_{G2} (the gate voltage of the cascode stage) = V_{D2} (drain voltage) = 2.5V, Frequency=1.8GHz.

IV. Conclusion

Large-signal model requirements were discussed for CMOS PA applications. 1- and 2-tone large-signal characterization results for a 0.13µm core transistor were presented. While a model generated with a typical quasi-static approach is sufficient, additional effort on fitting the G_m as a function of bias is needed to ensure a proper prediction of the large-signal behavior, which requires accurate extraction of the physical parameters for the core transistor. It was shown that the fundamental, 2nd, and 3rd harmonic characteristics as a function of bias just track the G_m and its 1st and 2nd order derivatives. In addition to G_m, the extrinsic drain and source resistance influences significantly the gain compression characteristics and needs to be extracted carefully as well. Finally the model extracted with the proposed additional considerations was demonstrated to be capable of predicting the distortion behavior of a transistor as well as its inter-modulation products up to the 5th order.

References

[1] I. Aoki, S. Kee, R. Magoon, R. Aparicio, F. Bohn, J. Zachan, G. Hatcher, D. McClymont, and A. Hajimiri, "A Fully Integrated Quad-Band GSM/GPRS CMOS Power Amplifier," IEEE International Solid-State Circuits Conference ISSCC 2008, pp. 570 – 636, Feb. 2008, San Francisco, CA.

[2] S. F. Tin, A. A. Osman, K. Mayaram, and C. Hu, "A simple subcircuit extension of the BSIM3v3 model for CMOS RF design," IEEE Journal of Solid-State Circuits, Vol. 35, Issuse 4, 2000, pp. 612 - 624

[3] Y. Cheng, M.J. Deen, and C.-H. Chen, "MOSFET modeling for RF IC design," IEEE Transactions on Electron Devices, Volume 52 , Issue 7, 2005 , pp. 1286 - 1303

[4] A. F. Tong, W. M. Lim, K. S. Yeo, C. B. Sia, and W. C. Zhou, "A Scalable RFCMOS Noise Model," IEEE Transactions on Microwave Theory and Techniques, Volume 57, Issue 5, Part 1, 2009 , pp. 1009 - 1019

[5] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements", IEEE Transactions on Electron Devices, Volume 48, Issue 12, 2001, pp. 2884 - 2892

[6] T.-Y. Lee and Y. Cheng, "High-frequency characterization and modeling of distortion behavior of MOSFETs for RF IC design," IEEE Journal of Solid-State Circuits, Volume 39, Issue 9, 2004, pp. 1407 – 1414.

[7] A. E. Parker and G. Qu, "Intermodulation Distortion Simulation with a New MOSFET Model," 30th European Microwave Conference, 2000, pp. 1 – 4

[8] B. O hAnnaidh and T.J. Brazil, "An accurate nonlinear MOSFET model for intermodulation distortion analysis", IEEE Microwave and Wireless Components Letters, Volume 14, Issue 7, 2004 , pp. 352 - 354

[9] Piet Wambacq and Willy M.C. Sansen, "Distortion Analysis of Analog Integrated Circuits," Kluwer Academic Publishers, 1998.

[10] W. Wu, X. Li, G. Gildenblat, G. Workman, S. Veeraraghavan, C. McAndrew, R. van Langevelde, G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen and J. Watts, "PSP-SOI: A Surface Potential Based Compact Model of Partially Depleted SOI MOSFETs," IEEE Custom Integrated Circuits Conference, 2007.

[11] P. Bendix, P. Rakers, P. Wagh, L. Lemaitre, W. Grabinski, C. C. McAndrew, X. Gu, and G. Gildenblat, "RF distortion analysis with compact MOSFET models," Proceedings of the 2004 IEEE Custom Integrated Circuits Conference, 2004 , pp. 9 – 12.