APPLICATION NOTE

Wafer Level Chip Scale Packages: SMT Process Guidelines and Handling Considerations

Introduction

The Skyworks Wafer Level Chip Scale Package (WLCSP) is a bumped die solution that can be used for in-module and/or standalone applications. WLCSP packaging technology is applied to Skyworks GaAs and/or Si device technologies for various applications.

This Application Note provides mechanical background information, specific guidelines for Printed Circuit Board (PCB) layout design, Surface Mount Technology (SMT) assembly processes, and other related issues to effectively mount Skyworks WLCSP device packages.

WLCSPs

WLCSP technology consists of bumping and backend processes. In the bumping process, various bump technologies are used to convert wafer I/Os to solderable bump I/Os that can be connected to system boards using Surface Mount Technology (SMT).

The backend process includes testing, wafer thinning, singulation, and tape reels, all of which provides the format needed for SMT work.

A representative WLCSP package is shown in Figure 1. The WLCSP solution offers several advantages compared to conventional solutions that use wire-bond does and standard I/C packages:

- Optimal RF performance with reduced inductance from the wire bonds
- High density interconnects to achieve small package footprints
- SMT capable assembly process

Typical Package Dimensions

Figure 2 shows a package dimension drawing for a typical WLCSP. Using different bump pitch, size, and height designs, Skyworks provides customers with devices that can be used for a variety of in-module and standalone applications. Our family of WLCSP modules are available in a range of body sizes and functions.

As a guideline, when a WLCSP is assembled on to a module substrate or PCB, the flux dip process method is used for fine pitch applications (when bump pitch is less than 0.3 mm). For coarse pitch applications, a solder paste print process can be used.

Figure 1. Typical Skyworks WLCSP Package
Substrate Design Guidelines

Substrate Terminal Pads

The substrate pads of a WLCSP should be metal defined or non-solder mask defined (NSMD) pads. Figure 3 shows a typical or representative substrate drawing for an 0.25 mm pitch WLCSP with the following dimensions for an in-module application:

Metal Defined Pad:
- Metal pad diameter (a) = 100 μm
- Metal trace width (b) = 80 μm

Substrate solder mask design (solder mask patch):
- Solder mask width (c) = 160 μm
- Solder mask pull-back from die edge (d) = 100 μm
- Solder mask pull-back from metal pad edge (e) = 30 μm

To achieve adequate underfill after the WLCSP attachment, the solder mask at the edge of the module should be pulled back 100 microns to provide more space for the underfill material (epoxy or mold compound) to flow under the module. This creates an underfill with minimal voids.
SMT Assembly Guidelines

Stencil Design
For a WLCSP with a bump pitch of 0.25 mm and a metal pad diameter of 0.1 mm, the flux dip assembly method is used. In the case of flux printing assembly, a flux stencil is required. The stencil design should be a 1:1 match for the dimensions and locations that are used in substrate metal pad designs. Stencil design guidelines vary according to the WLCSP configuration. Specific stencil design requirements are provided in Skyworks product Data Sheets.

SMT Pick and Place
The WLCSP package is a small package relative to a typical SMT package. For better accuracy, it is recommended to use automated fine-pitch placement machines with vision alignment to place the parts. Local fiducials are required on the board to support the vision systems and achieve placement accuracy.

“Pick and place” systems using mechanical centering are not recommended due to the high potential for mechanical damage to the WLCSP device. Ensure minimal pick and place force (typically < 0.5 N) is used to avoid damage, with all vertical compression forces controlled and monitored. Z-height control methods are recommended over force control.

Skyworks highly recommends the use of low-force nozzle options and compliant materials (e.g., rubber tipped) to further avoid any physical damage to the WLCSP device. Use only vacuum pencils with soft tip materials whenever manual handling is required.

All assemblers of WLCSP components are encouraged to conduct placement accuracy studies to ensure adequate compensation is provided for achieving high accuracy placement.

Due to the wide range of equipment and process parameters available including nozzle selection, and pick and place forces, Skyworks cannot provide specific SMT process parameters for each application. Skyworks recommends the assembler perform an adequate validation of the SMT pick and place process to ensure WLCSP die integrity is not compromised.

SMT Reflow Profile
Common infrared or convection reflow SMT processes are used for the assembly. Since most WLCSP modules are rated at a Moisture Sensitivity Level (MSL) of 1, no pre-baking is required before the assembly. Standard SMT reflow profiles, as shown in Figures 4 and 5, can be used to surface-mount the WLCSP modules on to the substrate. Ranges of recommended parameters for the SMT reflow profiles shown in Figures 4 and 5 are listed in Tables 1 and 2. Solder paste manufacturer’s recommendations should also be considered to determine the proper reflow profile.

NOTE: The maximum peak reflow temperature for a specific part is found in the device Data Sheet.

In all cases, a temperature gradient of 3 °C/sec or less should be maintained to prevent warpage of the package and to ensure that all joints reflow properly. Additional soak time and slower preheating time may be required to improve the out-gassing of solder paste.

The reflow profile also depends on the PCB density and the type of solder paste used. Final adjustments of the reflow profile should be made according to the device’s application requirements. Standard no-clean solder paste is generally recommended. If another type of flux is used, removal of flux residual may be necessary.

If solder balling occurs during reflow, the paste aperture may be decreased to reduce the amount of paste deposited to the PCB. Nitrogen may also be used to help counteract the tendency of the paste to form solder balls.

During the assembly process, the PCB must be supported properly to ensure board flatness. Typically, supports under the board are provided at each workstation but are not always available in a conveyor system. When thin or large boards are populated with components, the weight of the board, itself, plus the weight of the components may deform the PCB in reflow operation and cause the board to sag. This effect may shift a component from a designated location on the board after placement. Consequently, there is a large variation in solder joint height, which increases the potential for solder joint defects such as “bridging” and “opens.” Generally, carriers need to be designed and used for large or thin boards to ensure proper board flatness.

Although a certain amount of voids do occur in the solder joints, a 20 percent voiding distributed across the solder joints as small voids should be acceptable.

Assembly Considerations
WLCSPs are more susceptible to mishandling and processing-related Mechanical-Over-Stress (MOS) issues than conventional molded chip and wire packages. Care must be exercised throughout the transportation, inventory, staging, and manufacturing operations to ensure that the parts are not damaged. Experience has shown that all persons involved and associated with material handling and manufacturing should be trained in the proper methods and techniques of handling WLCSPs to avoid incidental damage.

All semiconductor devices, whether packaged or unpackaged, may be inadvertently damaged by static discharges. These charges can build up on any insulating surface, including the operator’s hair and clothing, and are measured in tens of thousands of volts. Just touching any of the connections on an grounded component can induce tunneling defects in the internal dielectric layers. The best way to avoid this is to ensure that all operators, tools, and equipment are suitably grounded before any contact is made.
Figure 4. Typical SMT Reflow Profile for Maximum Temperature of 250 °C

Table 1. Typical 250 °C SMT Reflow Profile Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Convection or Infrared/Convection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average ramp-up rate</td>
<td>3 °C/sec maximum</td>
</tr>
<tr>
<td>Preheat temperature = 175 ± 25 °C</td>
<td>60 to 180 seconds</td>
</tr>
<tr>
<td>Temperature maintained above 217 °C</td>
<td>60 to 150 seconds</td>
</tr>
<tr>
<td>Time between 245 °C and 250 °C (peak temperature)</td>
<td>10 to 20 seconds</td>
</tr>
<tr>
<td>Peak temperature range</td>
<td>250 (+0/−5) °C or 245 (+5/−0) °C</td>
</tr>
<tr>
<td>Ramp-down rate</td>
<td>6 °C/sec maximum</td>
</tr>
<tr>
<td>Time from 25 °C to peak temperature</td>
<td>480 seconds maximum</td>
</tr>
</tbody>
</table>
Figure 5. Typical SMT Reflow Profile for Maximum Temperature of 260 °C

Table 2. Typical 260 °C SMT Reflow Profile Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Convection or Infrared/Convection</th>
</tr>
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<tr>
<td>Average ramp-up rate</td>
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<td>60 to 150 seconds</td>
</tr>
<tr>
<td>Time between 255 °C and 260 °C (peak temperature)</td>
<td>10 to 20 seconds</td>
</tr>
<tr>
<td>Peak temperature range</td>
<td>260 (+0/-5) °C or 255 (+5/-0) °C</td>
</tr>
<tr>
<td>Ramp-down rate</td>
<td>6 °C/sec maximum</td>
</tr>
<tr>
<td>Time from 25 °C to peak temperature</td>
<td>480 seconds maximum</td>
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I/Cs are also vulnerable to oxidation, contamination, and mechanical damage. Wafer clam shells should only be opened and handled in approved work stations that are ESD compliant. Loose units outside of the original packing should be considered compromised and should be scrapped. The original packing materials have been selected to provide adequate protection for WLCSP packages through a normal distribution and manufacturing process.

Repacking of Skyworks products into other packaging or into other intermediate containers is not recommended and can potentially void Skyworks product warranty. Skyworks factory packing does not protect the WLCSPs from damage in extreme or excessive cases. Boxes and ring frames & hoop rings should not be dropped, impacted or exposed to crushing forces.

**Susceptibility to Mechanical Over Stress**

Due to the properties of silicon, GaAs and other semiconductor materials used in WLCSP packages are are brittle and subject to MOS damage during handling and assembly processes.

Unlike conventionally packaged parts, WLCSPs could be rendered nonfunctional or unreliable by even moderate MOS damage. Care must be taken in design, handling, and manufacturing to ensure that WLCSPs are adequately protected against impacts and mechanical stresses. Typical mechanical stress and its effects on die integrity are highlighted in Table 3.

**Underfill**

Although underfilling WLCSPs is often considered to be undesirable due to the added process complexity and cost, it has been demonstrated to be beneficial in board level reliability testing that includes thermal cycling, drop testing, and board bending performance.

As a result, underfills have been effectively used to improve solder joint reliability. Underfills enhance WLCSP board level reliability with the impact conditions associated with mobile electronics. A number of applications demand high reliability, which include medical, automotive, industrial, and military electronics. The decision to select and use a specific underfill should be carefully considered and the effectiveness of the desired underfill should be evaluated by the customer.

**Packing:** The WLCSP devices used in high volume SMT applications are generally supplied on film frame on a UV dicing tape. WLCSPs are provided in a bump-up configuration. Adequate steps should be taken to ensure proper UV exposure is performed before the die pick application.

**Table 3. Typical Mechanical Stresses and Effects on Die Integrity**

<table>
<thead>
<tr>
<th>Force Moments</th>
<th>Force Representation</th>
<th>Potential Sources</th>
<th>Prevention/Mitigation for Decreasing Force Movement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compressive forces</td>
<td></td>
<td>Mishandling in tape, Mishandling during and after SMT, Excessive placement force</td>
<td>Observe proper handling protocols, Backside tape lamination underfill, Optimization of SMT process</td>
</tr>
<tr>
<td>Flexure</td>
<td></td>
<td>Board flexing during and after SMT, Drop and vibration forces, Excessive Coefficient of Thermal Expansion (CTE) mismatch</td>
<td>Observe proper handling protocols, Backside tape lamination, Optimize fixturing, Optimization of SMT process</td>
</tr>
<tr>
<td>Impact</td>
<td></td>
<td>Mishandling in tape, Pick and place process errors, Mishandling during and after SMT</td>
<td>Observe proper handling, Underfill, Backside tape lamination</td>
</tr>
</tbody>
</table>