Features of the AAT4910 28V Half-Bridge, Dual N-Channel MOSFET Driver

Introduction

The AAT4910 FastSwitch™ is a member of Skyworks Application Specific Power MOSFET (ASPM™) product family. It is a half bridge buffered power stage that operates with an input voltage range of 2.7V to 5.5V. The device is designed to operate with a switching frequency of up to 2MHz, minimizing the cost and size of external components. The AAT4910 is protected from shoot-through current by integrated break-before-make circuitry. The drivers are offered with a single input control and a typical 50ns propagation delay from input to output.

Other features include low $R_{DS(on)}$ and low quiescent current which allows high efficiency performance. The AAT4910 also includes thermal protection to safeguard the device under extreme operating conditions.

These features allow the device to be used in many applications including multiphase DC/DC converter output power stages, DC motor drives, and Class D audio power amplifiers.

The AAT4910 is available in the space saving, Pb-free 8-pin SC70JW package and is rated over the -40 to 85°C temperature range.

Functional Block Diagram and Description

The AAT4910 is a dual MOSFET driver that takes a logic input (IN) and drives external high and low-side N-channel MOSFETs. It can be used to drive the power section of DC/DC converters, Class D audio power amplifiers, or other high-power devices requiring switched voltage. It is powered from a 5V rail and includes circuitry to drive the high-side N-channel MOSFET with up to a 28V power input. The enable input (EN), when driven low, turns off the driver and reduces the operating current to less than 1μA. Over-temperature shutdown protects the AAT4910 in case of a short circuit or defective MOSFET. High-side driver under-voltage lockout (UVLO) turns off the high-side MOSFET when there is insufficient voltage to drive the MOSFET, preventing damage at startup or if the IN input is held continuously high.

High-Side/Low-Side MOSFET Driver

The AAT4910 turns on the high-side external MOSFET when IN is driven high, and turns on the low-side MOSFET when IN is driven low. The low 0.5Ω pull-up and 1.7Ω pull-down resistance allow fast turn-on and turn-off times as well as the capability to drive multiple large MOSFETs. The lower pull-down resistance insures that the MOSFETs remain off during fast drain-voltage switching transients.
**Shoot Through Protection**

The high-side and low-side MOSFETs of the AAT4910 can not conduct at the same time to prevent shoot-through current. When the IN pulse rises, DL is first pulled down. The shoot-through protection circuit waits for 20ns before pulling up DH. Similarly, when IN goes low, DH is pulled down first, and the circuit pulls up DL after about 40ns. In this way, the high-side and low-side MOSFETs are never on at the same time, preventing supply voltage shorts to ground. The dead time between the DH and DL pulses should be kept as small as possible to minimize the current flows through the body diode of the low-side MOSFET(s). The break-before-make shoot-through protection significantly reduces the losses associated with the driver at high frequency.

![Figure 2: AAT4910 Timing Diagram.](image)

**Boost Strap Capacitor**

In order to fully turn on the high-side power MOSFET, the gate voltage must be 5V to 10V higher than its source voltage. The boost strap circuit includes a diode and a boost strap capacitor which are used to power the gate of the high side MOSFET to a voltage greater than the supply voltage without a separate power supply rail. The high-side driver boost capacitor between SW and BST is charged when the low-side MOSFET is on through the 5V power source and the external rectifier (see Figure 3). Once the capacitor is charged, the DH MOSFET gate driver output is powered from BST allowing sufficient MOSFET gate voltage for full enhancement. An under-voltage lockout feature on the BST-to-SW voltage turns off the DH output if the voltage falls below the under-voltage threshold. This ensures that if the boost capacitor discharges excessively or is unable to fully charge, the MOSFET will not be driven to an intermediate state that would result in excessive power dissipation and could cause the MOSFET to fail.
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The boost strap capacitor voltage rating should be able to withstand at least twice the maximum voltage supply, and its value should be approximately ten times larger than the gate capacitor value (rule of thumb):

**Eq. 1:**

$$C_{BS} = 10 \cdot \frac{Q_G}{V_{CC} - V_{DIODE}}$$

For example, a Si4908DY dual N-channel MOSFET has a total gate charge of 8nC. If the input supply is 5V and the voltage drop on the BST diode is 1V, then:

$$C_{BS} = 10 \cdot \frac{8\text{nC}}{5\text{V} - 1\text{V}} = 20\text{nF}$$

**Power MOSFET Selection**

Matching a MOSFET driver to a MOSFET is very difficult due to the variety of MOSFET technologies and silicon processes. Choosing the right MOSFET for a MOSFET driver depends on the application and on MOSFET parameters such as quiescent current, peak drive current rating, input–to–output propagation delay, latch-up immunity, package, and power dissipation.

**Power Dissipation**

The high side and low side conduction losses are associated with the $R_{DS(ON)}$ characteristics of the output switching devices. They can be derived from the following equation:

**Eq. 2:**

$$P_C = I_O^2 \cdot R_{DS(ON)H} \cdot D + I_O^2 \cdot R_{DS(ON)L} \cdot (1 - D)$$

$$= I_O^2 \cdot R_{DS(ON)H} \cdot \frac{V_{OUT}}{V_{IN}} + I_O^2 \cdot R_{DS(ON)L} \cdot \frac{V_{IN} - V_{OUT}}{V_{IN}}$$
The switching loss due to charging and discharging the gate capacitance of the MOSFET is given by:

\[ P_{SW} = C_{GATE} \cdot V_{IN}^2 \cdot F_{SW} \]

\[ = t_{SW} \cdot I_o \cdot V_{IN} \cdot F_{SW} \]

Where \( t_{SW} \) is the rise time of the gate voltage.

Power dissipation due to the quiescent current of the MOSFET driver is given by:

\[ P_{Q} = I_o \cdot V_{IN} \]

The total power dissipation is the sum of \( P_C \), \( P_S \), and \( P_Q \) equations:

\[ P_{TOTAL} = \frac{I_o^2 (R_{DS(ON)H} \cdot V_o + I_o^2 \cdot R_{DS(ON)L} \cdot [V_{IN} - V_o])}{V_{IN}} + (t_{SW} \cdot F_{SW} \cdot I_o + I_o) \cdot V_{IN} \]

The high-side MOSFET is usually selected to minimize switching losses and conduction losses. This typically implies a low gate resistance and low gate charge device. The low-side MOSFET is selected to have a low on resistance and large input gate capacitance to minimize conduction losses.

Gate Drive Current Ratings

Choosing the MOSFET for the MOSFET driver is based on the speed required to turn the power MOSFET on and off. The speed at which a MOSFET can be turned on and off is related to how quickly the gate capacitance of the MOSFET can be charged and discharged. The maximum package power dissipation can be estimated by the following equation:

\[ P_{D(MAX)} = V_{CC} \cdot I_{IN} \]

\[ = \frac{T_{J(MAX)} - T_{AMB}}{\theta_{JA}} \]

\[ = I_o \cdot V_{CC} + Q_{G(HS)}F_{SW} \cdot V_{CC} + Q_{G(LS)}F_{SW} \cdot V_{CC} \]

Where:

- \( T_{J(MAX)} \) is the junction temperature of the die (°C)
- \( T_{AMB} \) is the ambient temperature (°C)
- \( \theta_{JA} \) is the thermal resistance (°C/W)
- \( I_o \) is the operating current of the driver (mA)
- \( Q_{G(HS)} \) and \( Q_{G(LS)} \) are the gate charge of high side and low side MOSFET (nC)
- \( F_{SW} \) is the switching frequency (MHz)

Assuming that the maximum gate charge of the high-side and low-side MOSFETs are equal, the maximum gate drive capability for the designed maximum junction temperature without an external series resistor can be derived from Equation 6:

\[ Q_{G(MAX)} = \frac{1}{2F_{SW}} \left( \frac{T_{J(MAX)} - T_{AMB}}{\theta_{JA} \cdot V_{IN} - I_o} \right) \]
The relationship between gate capacitance, turn-on/turn-off time and the MOSFET driver current rating can be determined by:

**Eq. 8:**
$$I_{G(\text{MAX})} = C_{G(\text{MAX})} \cdot \frac{dV}{dt}$$

Where:
- $I_{G(\text{MAX})}$ is peak drive current for a given applied voltage
- $C_{G(\text{MAX})}$ is maximum gate capacitance
- $dV$ is gate voltage
- $dt$ is rise time of the MOSFET gate voltage

The relationship between $C_{G(\text{MAX})}$, $Q_{G(\text{MAX})}$, and $V_{\text{GATE}}$ is given by:

**Eq. 9:**
$$C_{G(\text{MAX})} = \frac{Q_{G(\text{MAX})}}{V_{\text{GATE}}}$$

The peak current drive requirements for a given MOSFET gate voltage can be derived from Equation 8 and Equation 9:

**Eq. 10:**
$$I_{G(\text{MAX})} = \frac{Q_{G(\text{MAX})}}{dt}$$

**Design Example**

- $V_{\text{IN}} = 5\text{V}$
- $V_{\text{GATE}} = 5\text{V}$
- $F_{\text{SW}} = 700\text{KHz}$
- $\theta_{ja} = 150\text{°C/W}$
- $I_{d} = 3.2\text{mA}$
- $T_{J(\text{MAX})} = 120\text{°C}$
- $T_{\text{AMB}} = 85\text{°C}$
- $t_{\text{RISE}} = dt = 20\text{ns}$

$$Q_{G(\text{MAX})} = \frac{1}{2 \cdot 700\text{KHz}} \left[ \frac{120\text{°C} - 85\text{°C}}{150\text{°C/W} \cdot 5\text{V}} - 3.2\text{mA} \right] = 31\text{nC}$$

$$C_{G(\text{MAX})} = \frac{Q_{G(\text{MAX})}}{V_{\text{GATE}}} = \frac{31\text{nC}}{5\text{V}} = 6.2\text{nF}$$

$$I_{G(\text{MAX})} = \frac{Q_{G(\text{MAX})}}{dt} = \frac{31\text{nC}}{20\text{ns}} = 1.6\text{A}$$
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Figure 4: Maximum Gate Charge vs. Switching Frequency.

The Maximum Gate Charge vs. Frequency graph in Figure 4 shows how the maximum gate drive capability of the MOSFET driver decreases as switching frequency increases.

Multiphase Buck Converter Application

The advances in VLSI technologies impose a new challenge for delivering high quality power to modern microprocessors. A multiphase buck converter offers several advantages over a single buck converter including low supply voltage, high output current, low current ripple on the input and output capacitors, fast transient responses, and high efficiency.

Figure 5: Three-Phase CPU Power Supply for AMD Socket 939 Processor.

Today’s multiphase buck converters are almost universally based on the buck topology, where the basic buck converter circuits are placed in parallel between the input and load. The primary advantage of this type of converter is that each phase is turned on at equally-spaced intervals over the switching period, and the load current is split among the n-phases of the multiphase converter. In this way, the heat losses on each of the switches are spread across a larger area. Another advantage provided by the multiphase converter is output ripple cancellation, which results in increasing the effective output frequency without sacrificing the switching losses. The increasing effective frequency reduces component size.
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A typical AAT4910 MOSFET driver application in a two-phase buck converter is shown in Figure 6. The multiphase synchronous buck controller generates PWM1 and PWM2 180° out-of-phase. These PWM signals are fed into the IN terminals of the AAT4910s to drive the dual N-channel power MOSFETs. The switching node voltages, inductor currents of channel 1 and channel 2, and output ripple cancellation are monitored on the oscilloscope (Figure 7). The output ripple is reduced by a factor of 2, while the load experiences a ripple frequency which is 2 times the switching frequency.

Figure 6: Two-Phase Buck Converter Using Two AAT4910 MOSFET Drivers.

Figure 7: Switching Waveforms of a Two-Phase Buck Converter Using Two AAT4910 MOSFET Drivers:
- CH1 (blue): Switching node of the upper driver;
- CH2 (light blue): Switching node of the lower driver;
- CH3 (pink): Inductor current of the upper driver;
- CH4 (green): Inductor current of the lower driver;
- Math (Red): Output ripple current (500mA/div).
**Motor Drive Application**

The AAT4910 is also ideally suited for use as an efficient output driver for DC brushless motor control. A motor control circuit is illustrated in Figures 8 and 9.

In half bridge motor control, one end of the motor is connected to the SW node of the driver, and the other end is connected to the power supply or ground. The speed of the motor is controlled by the duty cycle of the PWM at the IN terminal of the AAT4910. When the high side MOSFET turns OFF and the low side MOSFET turns ON, the current flows through the motor to ground from the supply voltage (blue arrow). During the ON time, the low side turns OFF and high side turns ON. The winding current keeps the induced current flowing in the same direction but exponentially decays toward zero.

*Figure 8: Half-Bridge Motor Drive Using the AAT4910 MOSFET Driver.*

*Figure 9: H-Bridge Motor Drive Using Two AAT4910 MOSFET Drivers.*
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The H-bridge (full-bridge) motor control power stage consists of two AAT4910 drivers and four DMOS power switches as shown in Figure 9. This configuration allows the motor to operate in both directions. For forward drive, the Hi1 switch and Lo2 switch in opposite halves of the bridge are turned ON, allowing current to flow in the direction of the solid blue arrow. Turning the Lo2 switch OFF causes a voltage transient that forward biases the body diode of the Hi2 switch. This body diode provides an alternative path for the winding current to flow (dashed blue arrow), and clamps the transient voltage one diode drop above the supply voltage.

The reverse drive is similar; the Hi2 and Lo1 switches are turned ON, and then the Lo1 is turned OFF, allowing current flow to continue in the reverse direction.

Power Stage Driver in Class D Audio Application

The Class D audio amplifier has quickly risen to replace the traditional Class A, B, and AB in consumer audio applications, including handheld devices such as mobile phone handsets, MP3 players, game consoles, LCD TVs, and home theater systems. In this type of amplifier, the switches are either fully ON or fully OFF, significantly reducing the power losses in the power devices. In this way, Class D audio offers a superior efficiency over 90%, which can not be achieved in a traditional class-AB audio.

The superior efficiency of Class D offers the best solution in handheld device applications, where battery life is the most important factor. In high-powered amplifier applications, such as audio-visual products, LCD TVs, and home theater systems, the high power efficiency of Class D provides the advantages of smaller power supplies, smaller circuit board area, and reduced heat dissipation.

In handheld applications, where size and cost are critical factors, a single chip solution is essential. However, in very high output power products, a Class D modulator IC is used to control the switching power stage, including MOSFET driver and power MOSFETs.

Half-Bridge Class D Audio Topology

In half-bridge Class D audio topology (Figure 10), the power stage, including an AAT4910 MOSFET driver and two synchronous power MOSFETs, is controlled by a pulse width modulator (PWM). In the single supply application, the driver is normally biased at a DC level that equals half-supply voltage. Typically, a 1000µF DC blocking capacitor (C2) is used at the output to provide DC short-circuit protection.

Figure 10: Half-Bridge Class D Audio Amplifier Using the AAT4910 MOSFET Driver.
Selecting a Output Power MOSFET for Class D Audio

The voltage rating of the output switching MOSFET is based on the output voltage swing and power required to achieve 1% total harmonic distortion (THD). The output voltage swing at full load is determined by the following equation:

\[ \text{Eq. 11: } V_{\text{SWING}} = 2 \cdot \frac{M}{100\%} \cdot \sqrt{2 \cdot P_{1\%\text{THD}}} \cdot R_{\text{SPEAKER}} \]

Where:

- \( M \) is the modulation index of 100%.
- \( P_{1\%\text{THD}} \) is the power at 1% total harmonic distortion (THD).
- \( R_{\text{SPEAKER}} \) is speaker impedance.

The voltage rating of the output switching MOSFET should be 50% higher than the peak-to-peak voltage swing. The peak switching device current is given by:

\[ \text{Eq. 12: } I_{\text{PEAK}} = \frac{2 \cdot P_{1\%\text{THD}}}{R_{\text{SPEAKER}}} \]

**Design Example**

- \( M = 100\% \text{ or } 1 \)
- \( P_{1\%\text{THD}} = 25W \)
- \( R_{\text{SPEAKER}} = 4\Omega \)

Hence,

\[ V_{\text{SWING}} = \frac{2}{100\%} \cdot \sqrt{2 \cdot 25W \cdot 4} = 20V \]

\[ I_{\text{PEAK}} = \frac{2 \cdot P_{1\%\text{THD}}}{R_{\text{SPEAKER}}} = \frac{2 \cdot 25W}{4W} = 3.5A \]

The MOSFET size is a trade-off between minimizing conduction losses and minimizing switching losses. Conductive losses (\( R_{\text{DS(ON)}} \cdot I_{\text{DS}} \)) dominate power dissipation and efficiency at high output power levels, while switching losses (\( C_{\text{GATE}} \cdot V_{\text{IN}} \cdot F_{\text{SW}} \)) dominate power dissipation at low output levels. Choosing a low \( R_{\text{DS(ON)}} \) MOSFET to minimize conduction losses at the high level output will increase the switching loss at low level output due to a significant increase in gate capacitance (\( C_{\text{GATE}} \)). Therefore, the power output device size is chosen to optimize power dissipation over a wide range of signal conditions.

**Gate Drive Choice and Propagation Delay Variation**

The mismatch in signal propagation delay between the low side and the high side device causes the most significant contribution of nonlinearity in a Class D audio amplifier. The switching time error in the gate drive results in variation in the dead time and increased THD. If the dead time is decreased beyond a certain point (depending on the switching speed of the MOSFETS), then both devices are conducting at the same time, which leads to large shoot-through currents that can reduce efficiency and may result in device destruction. However, increasing dead time results in increased THD. The maximum propagation delays between DH and DL signals from the point where the control signal splits should be set within 15ns.
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The AAT4910 dual MOSFET driver features a shoot-through protection circuit with a delay matching of DH and DL to within 15ns. The driver is also capable of providing 1.6A peak current drive requirements for a 5V gate voltage to charge and discharge up to 6.2nF MOSFET gate capacitance during the switching interval of 20ns to 50ns rise/fall times.

Output Filter Design and Feedback Network

Typically, a 22µH inductor core type, a 470nF polypropylene capacitor, and a 4Ω speaker are chosen to provide a cut-off frequency above the audio band (30 to 60KHz). The LC low-pass filter is capable of attenuating the carrier frequency (F_{SW}) as much as 31dB at 300KHz to prevent electro-magnetic interference (EMF) caused by harmonics.

A feedback network that includes a passive RC low pass filter may be connected from both the switching node and the filter output, and fed to the input of the error amplifier to minimize distortion and noise.

Full-Bridge Class D Audio Topology

Another well-known Class D topology is full-bridge (H-bridge), which uses four switching MOSFETs and Two AAT4910 drivers (Figure 11). Half-bridge topology is obviously simpler compared to H-bridge topology. However, it suffers from “bus pumping,” which can be observed when the half-bridge topology is powering a low frequency output to the load. The majority of the energy that is stored in the inductor of the low-pass filter flows back to the power supply, causing bus fluctuation. The voltage fluctuation in the power supply creates distortion.

Although the H-bridge design is more complicated, it does not suffer from bus pumping. In the H-bridge topology, the energy kicked back to the power supply from one side of the switching leg will be consumed in the other side of the switching leg.

![Figure 11: Full-Bridge Class D Audio Amplifier Using Two AAT4910 MOSFET Drivers.](image-url)
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Conclusion

The AAT4910 is a 28V half-bridge MOSFET driver optimized for driving two N-channel MOSFETs. Each driver can drive up to a 6.2nF gate capacitor or 31nC total gate charge at 700KHz during the 20ns transition time with a matching delay for DH and DL to within 15ns. The AAT4910 also features shoot-through protection and achieves high efficiency to suit multiphase buck converter, motor drive, and Class D audio applications.