

**Introduction**

The AAT2430A, 16-Channel White LED Driver, uses the SPI interface to control the PWM duty cycle and delay timing. The PWM duty cycle is set by the GS registers, and the delay timing is set by the DLY registers. Data to the GS and DLY registers is sent to the device via the SPI interface. The GS and DLY registers are latched with the new data either on the falling edge or the rising edge of PWM. The GS and DLY latch settings are selected by bits<3:2> and bits<1:0> in CTRL3 register for the AAT2430A as shown in Figure 1.

**CTRL3: Control 3 Register (Address C4h)**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>3DMODE</td>
<td>DOTR</td>
<td>INVERT</td>
<td>100DC</td>
<td>GSL2</td>
<td>GSL1</td>
<td>DLYL2</td>
<td>DLYL1</td>
</tr>
</tbody>
</table>

- **bit 7**
  - **3DMODE**: 3D Mode regulation point enable bit
    - 0: Disable 3D Mode. Regulation point is approximately 0.6V for $I_{csx} = 150mA$
    - 1: Enable 3D Mode. Regulation point is approximately 1.1V for $I_{csx} = 150mA$

- **bit 6**
  - **DOTR**: DOT function current sense feedback reference enable bit
    - 0: Enable DOT Reference
    - 1: Disable DOT Reference

- **bit 5**
  - **INVERT**: PWM inverting enable bit
    - 0: Disables inversion. Normal PWM duty cycle from grayscale settings
    - 1: Enables inversion. Inverting all PWM duty cycle from the grayscale settings

- **bit 4**
  - **100DC**: 100% PWM duty cycle enable bit
    - 0: Disables 100% PWM duty cycle. Use normal PWM control on all current sinks.
    - 1: Enables 100% PWM duty cycle. DLY and GS registers are overridden. All current sinks go to 100% duty cycle

- **bit 3-2**
  - **GSL<2:1>**: Grayscale Latch select bits
    - 00: GS Registers latched on falling edge of PWM
    - 01: GS Registers latched on rising edge of PWM
    - 10: Not defined for use in normal operation
    - 11: Not defined for use in normal operation

- **bit 1-0**
  - **DLYL<2:1>**: Delay Latch select bits
    - 00: DLY Registers latched on falling edge of PWM
    - 01: DLY Registers latched on rising edge of PWM
    - 10: Not defined for use in normal operation
    - 11: Not defined for use in normal operation

**Legend:**

- **R** = Readable bit
- **W** = Writeable bit
- **U** = Unimplemented
- **n** = Current Sink number
- **v** = Default value
- ’1’ = Bit is set
- ’0’ = Bit is cleared
- ‘x’ = Bit is unknown, don’t care

**Figure 1: CTRL3 Register.**
The AAT2430A has two GS and DLY data latch settings not defined for use in normal operation. These two data latch settings are on the rising edge of VSYNC and asynchronously through the SPI interface. Setting bits<3:2> and bits<1:0> to '10' will set the data latch on the rising edge of VSYNC. Setting bits<3:2> and bits<1:0> to '11' will set the data latch to occur asynchronously through the SPI interface. Under some conditions, these two data latch settings will lead to flicker on the LED channels. To avoid flicker, these two data latch settings are not recommended for use in normal operation. This application note will list the settings to avoid flicker when latching on the rising edge of VSYNC and asynchronously through the SPI interface.

Latching on the rising edge of VSYNC will lead to flicker when a previous PWM setting “GS+DLY_1” is changed to a new PWM setting “GS+DLY_2” under either of the following two conditions:

1. GS+DLY_1 > 4096 is changed to GS+DLY_2 < 4096 with DLY_1 = DLY_2.
2. GS+DLY_1 > 4096 is changed to 4096 < GS+DLY_2 < GS+DLY_1 with GS_1 ≠ GS_2, DLY_1 ≠ DLY_2

Note: 4096 is the full scale resolution for GS and DLY registers.

In condition 1, a previous PWM setting has the combined GS+DLY register value greater than 4096. A new PWM setting has the combined GS+DLY register value less than 4096 with DLY setting remaining the same. When the previous PWM setting is changed to the new PWM setting under these conditions, the internal counter of AAT2430A is not able to reset and apply the new setting. After the new setting is latched, the PWM stays on at 100% duty cycle for one VSYNC cycle before the new setting is applied to the PWM.

For example, a PWM with a GS_1 setting of 2867 and DLY_1 setting of 2048 has the combined GS+DLY value of 4915, greater than 4096. The new GS_2 setting is going to be 1638 with the DLY setting remaining the same. The combined GS+DLY value for the new setting is 3686, less than 4096. Now the PWM is updated to the new GS_2 setting from GS_1, and the combined GS+DLY value is changed from being greater than 4096 to being less than 4096. The PWM becomes 100% duty cycle for one VSYNC cycle starting from the VSYNC that latches in the new setting. After the VSYNC cycle completes, the PWM is set to the new setting. Figure 2 shows a graphical representation of this example.

![Figure 2: Changing the Combined GS+DLY Setting of PWM from Being Greater than 4096 to Being Less than 4096.](image-url)
Using the VSYNC and SPI Latches in the AAT2430A 16-Channel White LED Driver

In condition 2, a previous PWM setting has the combined GS+DLY register value greater than 4096. A new PWM setting has the combined GS+DLY register value greater than 4096 but less than the previous setting. Both the GS and DLY settings are different from the previous values. When the previous PWM setting is changed to the new PWM setting under these conditions, the internal counter of AAT2430A is not able to reset and apply the new setting. After the new setting is latched, the PWM stays on at 100% duty cycle for one VSYNC cycles before the new setting is applied to the PWM.

To avoid flicker, set the DLY register value to 0 when using the rising edge of VSYNC to latch. Since flicker only happens when the combined GS+DLY setting is greater than 4096, setting DLY to 0 will limit the combined GS+DLY setting to be always less than 4096 for all GS register settings.

When PWM is on and GS setting changes from high to low duty cycle, latching asynchronously through the SPI interface will lead to flicker whenever the latching occurs. The flicker is the same as when latching on the rising edge of VSYNC where PWM will stay on for 100% duty cycle for one VSYNC cycle. Figure 3 shows a case where the new setting is latched in when PWM is on, and Figure 4 shows a case where the new setting is latched in when PWM is off. Both Figure 3 and Figure 4 have exactly same setup with GS setting changing from a high value to a low value and DLY setting remaining the same.

![Diagram](image_url)

**Figure 3: Latching New Data when PWM is ON.**

![Diagram](image_url)

**Figure 4: Latching New Data when PWM is OFF.**
Using the VSYNC and SPI Latches in the AAT2430A 16-Channel White LED Driver

The only solution to avoid flicker is to apply the SPI signal when PWM is off. It may be feasible, but it will involve a large amount of detection and coding to implement this function. On top of the coding issue, latching asynchronously through the SPI interface will lead to synchronization between the LED and the video. So, it is not recommended to use latching asynchronously through the SPI interface.

In some applications, latching on the rising edge of VSYNC is the best approach. Due to the logic limitations, care is needed to have the system perform flawlessly. In the case of latching on the rising edge of VSYNC, the DLY setting is recommended to be 0 to avoid any possible flicker.