Output Capacitor Selection for the AAT115X Series Buck Converter

Introduction
Regardless of the application—from cell phones to wireless LAN cards—height, size, and efficiency are important features for components used with AAT115X converters. With this in mind, the recommended output capacitor for the AAT115X family of buck converters is presented in this Application Note. The design procedure for determining the capacitor value and calculating stresses is also examined.

Figure 1: Buck Converter.

Capacitor Type
Surface mount ceramic X5R or X7R capacitors are ideally suited for AnalogicTech's buck converter (Figure 1). X5R ceramic capacitors have a CV product with a temperature and voltage coefficient that is ideal for low voltage, high frequency, and high density switching regulators. Figure 2 shows the voltage and temperature characteristics for a 22µF, 6.3V, 0805, X5R ceramic capacitor. The graph illustrates the strong voltage coefficient typical of an X5R capacitor. From the graph, it can be seen that the applied voltage must be considered when determining the actual capacitor value. The impedance and equivalent series resistance (ESR) characteristics shown in Figure 3 are both typical of an X5R ceramic capacitor and ideal for achieving low output ripple at a high switching frequency.

Figure 2: Capacitance vs. Voltage Bias and Temperature (22µF, 6.3V, 0805, X5R).
Output Capacitor Value

Voltage loop stability is the main consideration when selecting an output capacitor for the AAT115X family of DC/DC converters. A simplified schematic of the AAT115X feedback control loop is shown in Figure 4. The inner peak current mode loop is modeled as a current-controlled current source which is programmed by an output voltage error amplifier. The crossover frequency, phase, and gain margin of the voltage loop vary with the output capacitor size. As the output capacitor is increased, the voltage loop crossover frequency decreases and the phase and gain margin increases. Appendix A (page 7) displays a table and Bode plots with the suggested ceramic output capacitor for various AAT1156 output voltages.

The X5R ceramic capacitor has a sufficiently low ESR that the capacitor does not present an ESR zero to the voltage loop. It simply adds a single pole roll off. The use of an alternate high-ESR capacitor, such as a tantalum or organic electrolyte, will not produce the same phase and gain margin results given the same capacitor value. For these types of capacitors, the ESR zero will occur before the loop crossover frequency. Therefore, it must not be assumed that the ceramic output capacitor can be substituted with another type without affecting stability, crossover frequency, phase, and gain margin.

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**Figure 3: ESR and Impedance vs. Frequency**

* (22µF, 6.3V, 0805, X5R).

**Figure 4: AAT115X Feedback Control Loop.**
After selecting a ceramic capacitor which provides the desired phase and gain margin, the output capacitor value must be examined to insure that it meets the load transient demands. For applications with large instantaneous load transitions, the output capacitor size must be sufficient to limit the output voltage excursion during load transient recovery. For a step increase in load current, the output capacitor supplies the change in load current while the converter recovers and responds to the new load level. The feedback control loop typically requires three switching cycles to increase the inductor current to match the increased load demand. The capacity required to limit the output voltage droop to a specific level ($V_{\text{DROOP}}$) is:

$$C = \frac{3 \cdot (\Delta I_o)}{F_{\text{SW}} \cdot V_{\text{DROOP}}}$$

For an instantaneous step decrease in load current, the output capacity required to limit the output voltage overshoot ($V_{\text{OS}}$) during a full load to no load transient must be determined. This transient requires the excess energy stored in the output inductor to be absorbed by the output capacitor with a limited overshoot in the output voltage.

$$C = \frac{L \cdot I_o^2}{(V_o + V_{\text{OS}})^2 - V_o^2}$$

If necessary, the capacitor size should be increased beyond that selected for stability to meet the load transient requirement.

**Output Capacitor Ripple Current**

Because the ESR of ceramic capacitors is low, the capacitor temperature rise due to ripple current dissipation is usually negligible. Good design practice dictates that we always confirm this and verify that the output capacitor RMS current and temperature rise are within the manufacturer's suggested limit. The maximum RMS ripple current seen by the output capacitor occurs at the maximum input voltage. The capacitor ripple current consists of the AC portion of the inductor current. The DC component of the inductor current is passed on to the load as shown in Figure 5. The typical ceramic X5R ripple current rating corresponds to the amount of ripple sufficient to raise the capacitor temperature by 20°C above the ambient temperature. Figure 6 graphs the temperature rise vs. the applied ripple current for the recommended capacitor. It shows that the current required to reach a 20°C rise above ambient is in excess of 1A RMS, much higher than the ripple current seen in any AAT115X application.
If the ESR and thermal resistance specifications are available, the power dissipation and temperature rise can also be calculated. The thermal resistance ($\Theta$) for the 0805 size capacitor is 207°C/W. The power dissipated in the output capacitor is the RMS current squared multiplied by the capacitor ESR (2.2mΩ @ 1MHz from the plot in Figure 3). As seen in Figure 3, the capacitor ESR varies with frequency and must be evaluated at the converter switching frequency. The temperature rise is calculated by multiplying the power dissipated ($P_{CAP}$) by the thermal resistance ($\Theta$).
Output Ripple Voltage

The ceramic capacitor can be modeled as an ideal capacitor in series with a resistor and inductor, with all three components contributing to the effective output voltage ripple. The capacitor resonant frequency is the frequency at which the capacitor impedance is equal to the series resistance. Above this frequency, the inductive reactance dominates over the capacitive reactance, and the impedance vs. frequency has a positive slope. It is desirable to select a ceramic capacitor whose resonant frequency is close to the converter switching frequency. X5R and X7R ceramic capacitors have extremely low ESR with typical values less than 5mΩ. Consequently, the output voltage ripple due to ESR is small.

A simulation which includes the parasitic elements of the suggested capacitor is shown in Figure 7. For this simulation, the input to the output filter (LX node) is replaced with an ideal square wave with an amplitude equal to the maximum input voltage. The extremely low ripple associated with a low ESR/ESL ceramic output capacitor can be seen.

\[
P_{\text{CAP}} = I_{\text{RMS}}^2 \cdot \text{ESR}
\]

\[
\Delta T = P_{\text{CAP}} \cdot \Theta
\]

Summary

X5R or X7R surface mount ceramic capacitors are ideal output capacitor solutions for the AAT115X series buck converters. They are available with voltage, ESR, and capacity characteristics that are ideal for high frequency, high density, switch mode power supplies. The control loop stability (gain and phase margin) generally dictates the capacity required, while applications with large instantaneous load transitions may require increased capacity. Once the correct value of X5R capacitor has been selected, the ripple current, temperature rise, and output voltage ripple can be examined.
Design Example

Specifications:

\( V_O = 1.0V \)
\( I_O = 700mA \)
\( V_{IN} = 2.7V \) to 3.6V
\( L_O = 2.2\mu H \)
\( V_{DROOP} = V_{OS} = 50mV \) for Load Transient

1. Determine capacitance from Appendix A, Table 1.

\[ C_O = 2 \times 22\mu F \] for a 41° phase margin and 11 dB gain margin.

2. Calculate the minimum capacitance needed to meet the transient response requirements.

The capacitance selected for stability is larger than that required for the transient response; therefore, the capacity need not be increased.

\[ C = \frac{3 \cdot (\Delta I_O)}{F_{SW} \cdot V_{DROOP}} = \frac{3 \cdot 0.7A}{1.0MHz \cdot 50mV} = 42\mu F \]

\[ C = \frac{L \cdot I_O^2}{(V_O + V_{OS})^2 - V_O^2} = \frac{2.2\mu H \cdot 0.7A^2}{1.05V^2 - 1V^2} = 10\mu F \]

3. Calculate ripple current and temperature rise.

\[ I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}} = \frac{1}{3.5} \cdot \frac{1.0V \cdot (4.2V - 1.0V)}{2.2\mu H \cdot 1MHz \cdot 4.2V} = 98mA \]

\[ P_{CAP} = I_{RMS}^2 \cdot ESR = 100mA^2 \cdot 2.2m\Omega = 22\mu W \]

\[ \Delta T = P_{CAP} \cdot \Theta = 22\mu W \cdot 207^\circ C/W << 1^\circ C \]
Appendix A

Table 1: AAT1156 Output Filter Values and Loop Characteristics

<table>
<thead>
<tr>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$L_{\text{OUT}}$ (µH)</th>
<th>$C_{\text{OUT}}$ (µF)</th>
<th>Crossover Frequency (kHz)</th>
<th>Phase Margin (°)</th>
<th>Gain Margin (dB)</th>
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<tr>
<td>0.8</td>
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<td>3 x 22</td>
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<td>45</td>
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Frequency (MHz) vs. Gain and Phase for different bias conditions.

- **1.0V; 0.7A; 1.5μH; 2 x 22μF**
  - \( F_c = 168 \text{ kHz} \)
  - \( \Phi_m = 46^\circ \)
  - \( G_m = 12 \text{ dB} \)

- **1.0V; 0.7A; 1.5μH; 2 x 22μF**
  - \( F_c = 168 \text{ kHz} \)
  - \( \Phi_m = 46^\circ \)
  - \( G_m = 12 \text{ dB} \)

- **1.0V; 0.7A; 3.3μH; 2 x 22μF**
  - \( F_c = 168 \text{ kHz} \)
  - \( \Phi_m = 33^\circ \)
  - \( G_m = 9 \text{ dB} \)

- **1.2V; 0.7A; 2.2μH; 2 x 22μF**
  - \( F_c = 179 \text{ kHz} \)
  - \( \Phi_m = 38^\circ \)
  - \( G_m = 8 \text{ dB} \)

- **1.2V; 0.7A; 3.3μH; 2 x 22μF**
  - \( F_c = 179 \text{ kHz} \)
  - \( \Phi_m = 33^\circ \)
  - \( G_m = 9 \text{ dB} \)

- **1.5V; 0.7A; 2.2μH; 2 x 22μF**
  - \( F_c = 157 \text{ kHz} \)
  - \( \Phi_m = 54^\circ \)
  - \( G_m = 11 \text{ dB} \)
Bode Plot Measurement Method

In order to measure the loop gain, the feedback loop must be broken and an AC source inserted. The schematic shown in Figure A-1 illustrates the method used for measuring the loop gain and phase for the AAT115X series converters. When measuring the loop gain, monitor the switching waveform and the output ripple to verify that the injected signal magnitude is appropriate. Excessive signal injection can cause the loop to enter into a non-linear region due to clipping at a supply rail or exceeding the dynamic range of a stage within the loop. A non-sinusoidal output, clipped signal, or erratic switching waveforms is an indication of excessive injected source magnitude. Insufficient injected signal magnitude reduces the measured signal below the noise floor and can cause errors in measurement. In order to avoid this, it may be necessary to narrow the frequency sweep range so that the injected signal is never either too large or too small. Of course, the area of greatest concern is near the crossover frequency.

Operational amplifiers U2A and U2B are inserted into the loop in order to guarantee that the impedance requirements at each side of Rs are met. Receiver Channel A side of Rs must be high impedance, while the Channel B side Rs should be low impedance for accurate results. The opamps must be unity gain with no phase delay across all frequencies of interest.

Figure A-1: Test Circuit for Loop Gain and Phase.
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