



SKYWORKS®

Application Note Switch Time Reduction

RELEVANT PRODUCTS

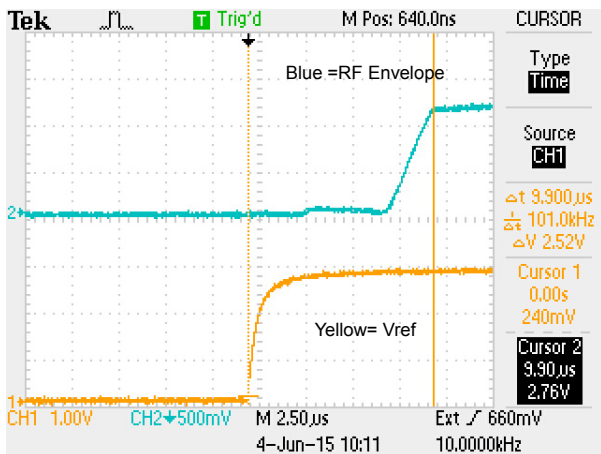
- AWB71XX and AWB72XX series PAM's

OVERVIEW

The AWB7XXX is a highly linear, fully matched, power amplifier module designed for picocell, femtocell, and customer premises equipment (CPE) applications. Its high power efficiency and low adjacent channel power levels meet the extremely demanding needs of small cell infrastructure architectures. Designed for LTE, WCDMA, HSDPA air interfaces and meets 3GPP specification TS36-104 section 6.4.2 for transmitter On/Off period of 17uS, see Figure 1. This application note describes a simple circuit that can be used to further reduce the turn-on of the PAM if required.

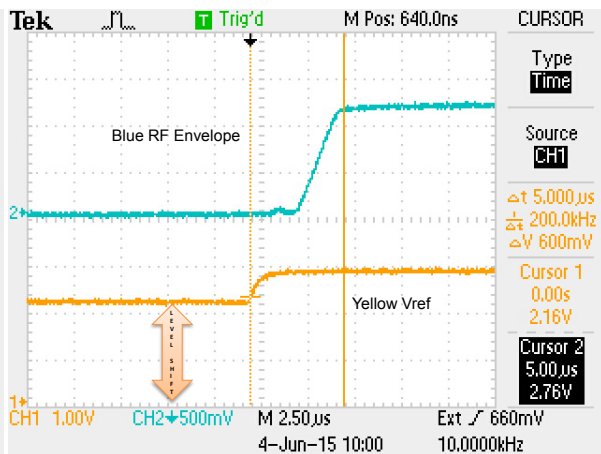
REDUCED TURN ON TIME

The turn-on time for the AWB7XXX series PAM's is dominated by an internal RC network that is tied directly to the VREF pin. Therefore, the turn-on time can be reduced by reducing the voltage swing on VREF. Applying a voltage greater than 0 V to the VREF pin in the off state will reduce the time necessary to charge the internal capacitors, while keeping the RF amplifier portion shut down. As a result, the voltage ramp to 2.85 V decreases and the turn-on time of the PA is significantly reduced. Because many systems do not have the ability to directly supply 1-2 V (Low Level) and 2.85 V (High Level), a simple resistive divider circuit can be used to level shift the standard 0 V low logic level. See Figure 2.



Note:
Low Level = 0 V, High Level = 2.85 V

Figure 1: Nominal RF ON time < 10 µS



Note:
Low Level = ~ 2 V, High Level = 2.85 V

Figure 2: RF ON time < 2 µS

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LEVEL SHIFTER

Figure 3 shows a simple level shifter circuit for AWB71XX family of PAM, that uses a 3.3 V regulated supply (commonly available in chipset LDO's) in addition to the standard 2.85 VREF⁽¹⁾ control. R1 sets up the high level in union with the effective bias ON current (IREF⁽¹⁾).

R2 will determine the low level "OFF" value. This should not exceed 2.2 V.

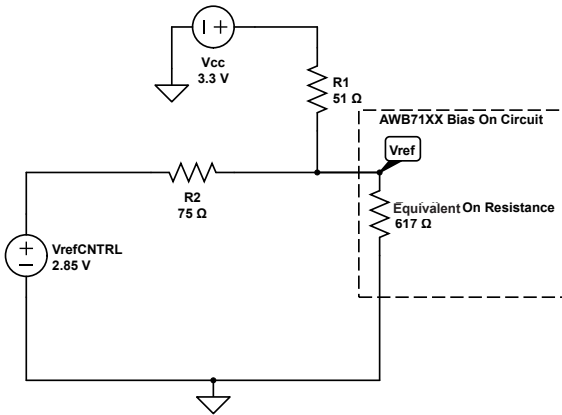


Figure 3: Level Shifter AWB71XX

BIAS ON CURRENT

VREF pin ON current for AWB72XX current will require approximately 2x the current of an AWB71xx device. As a result, R1 for AWB72XX is lowered. See Figure 4.

Note 1: More detailed VREF control can be developed per part by Skyworks Applications based on specific part and LDO used. Specific values will be recommended that window Vref within operational range. Low/High level set by function generator

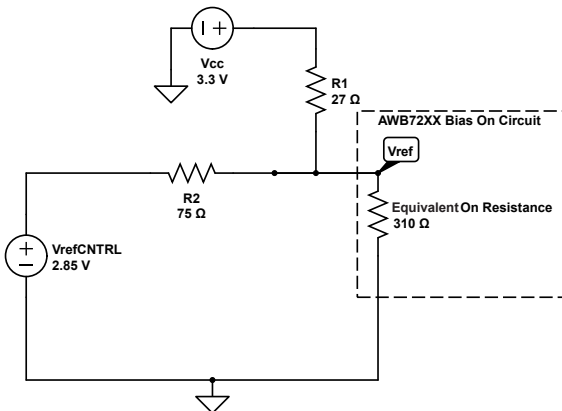


Figure 4: Level Shifter AWB72XX

VALIDATION TESTING

Figure 5 is a block diagram showing test configuration used to measure Figures 1 and 2 Low/High level set by function generator.

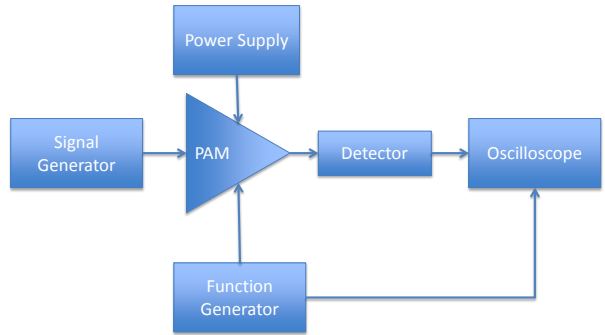


Figure 5: Test Block Diagram

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